AN4904
Application note

Migration of microcontroller applications from STM32F1 Series to STM32F4 Access lines

Introduction

For more and more applications using STM32 products, it is important to migrate a project easily to a different microcontroller in the same product family.

Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. On the other hand, cost reduction objectives may force you to switch to smaller components and shrink the PCB area.

This application note is intended to help analyze the steps you need to migrate from an existing STM32F1 Series based design to STM32F4 Access lines. It groups together all the most important information and lists the vital aspects that you need to address.

The current document lists the ‘full set’ of features for STM32F1 and the equivalent features of STM32F401/410/411/412/413/423 (Access lines) products when available. To fully benefit from this application note, you should be familiar with the STM32 microcontroller documentation available from *www.st.com* with a particular focus on the documents listed below.

STM32F401/410/411/412/413/423 lines:

- STM32F401xB/C and STM32F401xD/E reference manual (RM0368)
- STM32F410 reference manual (RM0401)
- STM32F412 reference manual (RM0402)
- STM32F411xC/E reference manual (RM0383)
- STM32F413/423 reference manual(RM0430)
- All the STM32F401/410/411/412/413/423 lines’ datasheets.

STM32F1 Series:

- STM32F1xx reference manual (RM0008)
- STM32F1xx reference manual (RM0041)
- STM32F1xx datasheets
- STM32F1 Flash and EEPROM programming manuals (PM0068, PM0056, PM0075).

Table 1. Applicable products

Type	Product Series / line
Microcontrollers	STM32F1 Series STM32F401 line STM32F410 line STM32F411 line STM32F412 line STM32F413/423 line

Contents

List of figures

List of tables

1 Hardware migration

The available packages for the STM32F1 Series and STM32F401/410/411/412/413/423 lines are listed in *Table 2*.

Table 2. Package availability(1)

Package	STM32F1 Series					STM32F401/410/411/412/413/423 lines				
	F100 value line	F101	F102	F103	F105 /107	F401	F410	F411	F412	F413 /423
LQFP144	X	X	-	X	-	-	-	-	X	X
LQFP100	X	X	-	X	X	X	-	X	X	X
LQFP64	X	X	X	X	X	X	X	X	X	X
LQFP48	X	X	X	X	-	-	X	-	-	-
UFBGA144	-	-	-	-	-	-	-	-	X	X
UFBGA100	-	-	-	X	-	X	-	X	X	X
UFBGA64	-	-	-	-	-	-	X	-	-	-
LFBGA144	-	-	-	X	-	-	-	-	-	-
LFBGA100	-	-	-	X	X	-	-	-	-	-
TFBGA64	X	-	-	X	-	-	-	-	-	-
WLCSP81	-	-	-	-	-	-	-	-	-	X
WLCSP64	-	-	-	X	-	-	-	-	X	-
WLCSP49	-	-	-	-	-	X	-	X	-	-
WLCSP36	-	-	-	-	-	-	X	-	-	-
UFQFPN48	-	-	-	-	-	X	X	X	X	X
VFQFPN36	-	X	-	X	-	-	-	-	-	-

1. ‘X’ denotes available package.

The STM32F401/410/411/412/413/423 lines and STM32F1 Series present a high level of pin compatibility. Most peripherals share the same pins in the two families.

The transition from the STM32F1 Series to the STM32F401/410/411/412/413/423 lines is easy since only a few pins are impacted (refer to *Table 3* and *Table 4*).

Table 3. STM32F1 Series and STM32F401/410/411/412/413/423 lines pin out differences (QFP)(1)

Package / pin number				Signal / supply name	
QFP48	QFP64	QFP100	QFP144	STM32F1 Series	STM32F401/410/411/412/413/423 lines
5	5	12	23	PD0-OSC_IN	PH0-OSC_IN
6	6	13	24	PD1-OSC_OUT	PH1-OSC_OUT
-	-	19	30	VSSA	VDD
-	-	20	31	VREF-	VSSA
22	30	48	-	PB11	VCAP_1
-	-	-	71	VSS	VCAP_1
-	-	73	106	NC	VCAP_2
-	-	-	143	VSS	PDR_ON
-	-	-	95	VDD	VDDUSB

1. Dependence on product package availability.

Table 4. STM32F1 Series and STM32F401/410/411/412/413/423 lines ball out differences (BGA)(1)

Package / ball location		Signal / supply name	
UFBGA100	LFBGA144	STM32F1 Series	STM32F401/410/411/412/413/423 lines
-	C11	NC	VDDUSB
-	H7	VSS	VCAP_1
-	G9	VSS	VCAP_2
H3	-	VDD	PDR_ON
-	E5	VSS	PDR_ON
E3	H5	VSS	BYPASS_ REG
C11	-	NC	VCAP_2
L11	-	PB11	VCAP_1

1. Dependence on product package availability.

Note: The STM32F1 Series proposes an LFBGA100 package that has a different ball out and size than the UFBGA100. It is not compatible with the STM32F401/410/411/412/413/423 lines' UFBGA100 package.

The STM32F103 is proposed in a WLCSP64 package, which is not compatible with that of the STM32F412.

Recommendations for migration from an STM32F1 Series board to an STM32F401/410/411/412/413/423 line board

The VSSA pin (pin 19 on QFP100) is now used as VDD in the STM32F401/410/411/412/413/423 lines.

For STM32F410 LQFP64 package, there is no PD2 pin, it is replaced by PB11.

On STM32F401/410/411/412/413/423 lines there are no PD0 and PD1 pins; they are replaced by PH0 and PH1 respectively.

Figure 1 and *Figure 2* show examples of board designs that are compatible with both the STM32F1 Series and STM32F401/410/411/412/413/423 lines.

Figure 1. Compatible board design (LQFP100)

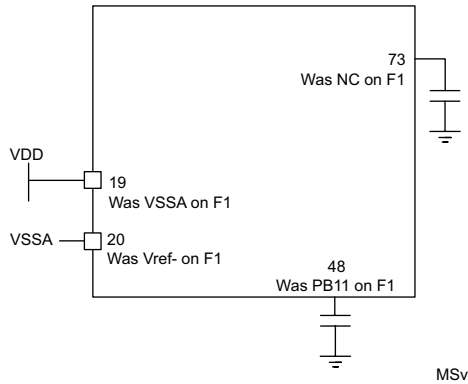
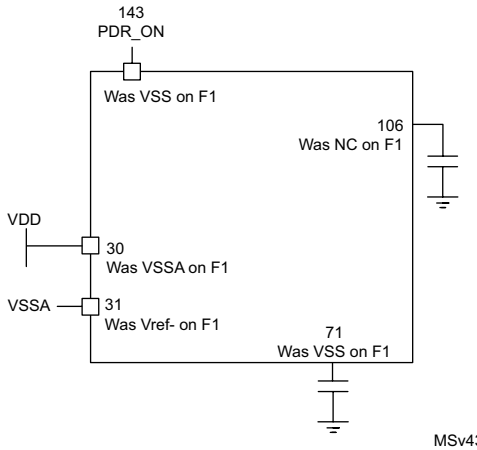


Figure 2. Compatible board design (LQFP144)



2 Boot mode selection

Both the STM32F401/410/411/412/413/423 lines and the STM32F1 Series can select between 3 boot-mode options:

- boot from main Flash memory
- boot from SRAM
- boot from system memory.

Table 5 summarizes the different configurations available for selecting the boot mode.

Table 5. Boot modes

STM32F401/410/411/412/413/423/F1 boot mode selection		Boot mode	Aliasing
BOOT1	BOOT0		
X	0	Main Flash memory	Main Flash memory is selected as the boot space
0	1	System memory	System memory is selected as the boot space
1	1	Embedded SRAM	Embedded SRAM is selected as the boot space

Embedded boot loader

The embedded boot loader is located in the system memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the serial interfaces shown in *Table 6*.

Table 6. Bootloader interfaces(1)

Peripheral	Pin	STM32F1 Series			STM32F4 lines			
		STM32 F10xxx	STM32 F105xx/ F107xx	STM32 F10xxx XL-density(2)	STM32 F401/ F411	STM32 F410	STM32 F412	STM32 F413/ F423
DFU	USB_DM (PA11) USB_DP (PA12)	X	X	X	X	-	X	X
CAN2	CAN2_RX (PB5) CAN2_TX (PB6)	-	X	-	-	-	-	-
	CAN2_RX (PB5) CAN2_TX (PB13)	-	-	-	-	-	X	X
USART1	USART1_TX (PA9) USART1_RX (PA10)	X	X	X	X	X	X	X
USART2	USART2_TX (PD5) USART2_RX (PD6)	-	X	X	X	-	X	X
	USART2_TX (PA2) USART2_RX (PA3)	-	-	-	-	X	-	-
USART3	USART3_TX (PB10) USART3_RX (PB11)	-	-	-	-	-	X	X
I2C1	I2C1_SCL (PB6) I2C1_SDA (PB7)	-	-	-	X	X	X	X
I2C2	I2C2_SCL (PB10) I2C2_SDA (PB11)	-	-	-	X	X	-	-
	I2C2_SCL (PF0) I2C2_SDA (PF1)	-	-	-	-	-	X	X
I2C3	I2C3_SCL (PA8) I2C3_SDA (PB4)	-	-	-	X	-	X	X
I2C4	I2C2_SCL (PB10) I2C2_SDA(PB3)	-	-	-	-	X(3)	-	-
	I2C2_SCL (PB15) I2C2_SDA(PB14)	-	-	-	-	X(4)	X	X
SPI1	SPI1_NSS (PA4) SPI1_SCK (PA5) SPI1_MISO (PA6) SPI1_MOSI (PA7)	-	-	-	X	X(4)	X	X
	SPI1_NSS (PA15) SPI1_SCK (PA5) SPI1_MISO (PB4) SPI1_MOSI (PB5)	-	-	-	-	X(3)	-	-

Table 6. Bootloader interfaces[1] (continued)

Peripheral	Pin	STM32F1 Series			STM32F4 lines			
		STM32 F10xxx	STM32 F105xx/ F107xx	STM32 F10xxx XL-density[2]	STM32 F401/ F411	STM32 F410	STM32 F412	STM32 F413/ F423
SPI2	SPI2_NSS (PB12) SPI2_SCK (PB13) SPI2_MISO (PB14) SPI2_MOSI (PB15)	-	-	-	X	-	-	-
	SPI2_NSS (PB12) SPI2_SCK (PB13) SPI2_MISO (PC2) SPI2_MOSI (PC3)	-	-	-	-	X	-	-
SPI3	SPI3_NSS (PA15) SPI3_SCK (PC10) SPI3_MISO (PC11) SPI3_MOSI (PC12)	-	-	-	X	-	X	X
SPI4	SPI3_NSS (PE11) SPI3_SCK (PE12) SPI3_MISO (PE13) SPI3_MOSI (PE14)	-	-	-	-	-	-	X

1. For smaller packages please verify pin and peripheral availability.
2. STM32F101xx and STM32F103xx microcontrollers where the Flash memory density ranges between 768 Kbytes and 1 Mbyte.
3. For STM32F410Tx devices.
4. For STM32F410Cx/Rx devices.

Note: Please refer to AN2606 for more details of the bootloader.

3 Peripheral migration

3.1 STM32 product cross-compatibility

The STM32 Series embeds a set of peripherals which can be classified in three categories:

- **Peripherals that are common to all products**. These peripherals are identical on all products, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- **Peripherals that present minor differences from one product to another** (usually differences due to the support of new features). Migrating from one product to another is very easy and does not require any significant new development effort.
- **Peripherals which have been considerably modified from one product to another** (new architecture, new features and so on). For this category of peripherals, migration requires new development at application level.

Table 7 gives a general overview of this classification.

Table 7. STM32 peripheral compatibility between STM32F1 Series and STM32F401/410/411/412/413/423 lines

Peripherals		Number of instances					Compatibility		
		STM32 F1 Series	STM32 F401/ F411 lines	STM32 F410 line	STM32 F412 line	STM32 F413/ F423 line	Software	Pinout	Comments
Communication interfaces	QuadSPI	0	0	0	1	1	NA	NA	New QuadSPI added for STM32F412/413/423 lines
	SPI/I2S	3/2	4/2 5/2	3/3	5/5	5/5	Full Compatibility	Partial compatibility	Full compatibility for the same feature. Some alternate functions are not mapped on the same GPIO.
	I2C	2	3	3	4	4	Full Compatibility	Partial compatibility	Full compatibility for the same feature. Some alternate functions are not mapped on the same GPIO. For STM32F410/412/413/423 lines the new I2C interface supports the Fast-mode plus (up to 1 MHz).
	USART	5	3	3	4	10	Full Compatibility	Full Compatibility	Full compatibility for the same feature
	USB OTG FS	1	1	0	1	1	Full compatibility	Full compatibility	Separate power rail for STM32F412/413/423 lines
	SDIO	1	1	1	1	1	Full Compatibility	Partial compatibility	SDIO only available for STM32F103 in STM32F1 Series
	CAN	2	0	0	2	3	Full compatibility	Full compatibility	Full compatibility for the same feature
	SAI	0	0	0	0	1	NA	NA	New SAI added for STM32F413/423 line

Table 7. STM32 peripheral compatibility between STM32F1 Series and STM32F401/410/411/412/413/423 lines (continued)

Peripherals		Number of instances					Compatibility		
		STM32 F1 Series	STM32 F401/ F411 lines	STM32 F410 line	STM32 F412 line	STM32 F413/ F423 line	Software	Pinout	Comments
Timers	GP	10	7	3	10	10	Full compatibility	Partial compatibility	Internal connections may differ. Some pins are not mapped on the same GPIO.
	Advanced	2	1	1	2	2			
	Basic	2	0	1	2	1			
	Low Power	0	0	1	0	1			
Ethernet		1	0	0	0	0	NA	NA	Ethernet peripheral not available on STM32F401/410/411/412 lines
WWDG		1	1	1	1	1	Full Compatibility	NA	-
IWDG		1	1	1	1	1	Full Compatibility	NA	-
GPIO(1)		Up to 142 IOs	Up to 81 IOs	Up to 50 IOs	Up to 114 IOs	Up to 114 IOs	Full compatibility	Full compatibility	Full compatibility for the same feature
ADC		3	1	1	1	1	Full compatibility	NA	Full compatibility for the same feature
DAC		2	0	1	0	2	Full compatibility	NA	Full compatibility for the same feature
RCC		1	1	1	1	1	Partial Compatibility	NA	-
PWR		1	1	1	1	1	Full compatibility	NA	Full compatibility for the same feature
DFSDM		0	0	0	1	2	NA	NA	New DFSDM 4 channels / 8 filters for STM32F413/423 line
AES		0	0	0	0	1	NA	NA	New AES 256 bits only for the STM32F423 device

1. Maximum number of instances.

3.2 Memory mapping

The peripheral address mapping of the STM32F401/410/411/412/413/423 lines is different to that of the STM32F1 Series.

Table 8 provides the peripheral address mapping correspondence between F1 and STM32F401/410/411/412/413/423 lines.

Table 8. Bus mapping differences between STM32F1 Series and STM32F401/410/411/412/413/423 lines

Peripheral	STM32F1 Series		STM32F401/410/411/412/413/423 lines	
	Bus	Base address	Bus	Base address
Backup registers (BKP)	APB1	0x4000 6C00	NA	
I2S2ext	NA		APB1	0x4000 3400
I2S3ext				0x4000 4000
UART8				0x4000 7C00(1)
UART7				0x4000 7800(1)
UART4	APB1	0x4000 4C00		0x4000 4C00(1)
UART5		0x4000 5000		0x4000 5000(1)
CAN1		0x4000 6400		0x4000 6400(2)
CAN2		0x4000 6800		0x4000 6800(2)
CAN3	NA			0x4000 6C00(1)
I2C2	APB1	0x4000 5C00	APB1	0x4000 5800
I2C3	NA			0x4000 5C00
I2CFMP1				0x4000 6000
DAC	APB1	0x4000 7400	APB1	0x4000 7400(3)
LPTIM1	NA			0x4000 2400(3)
TIM1	APB2	0x4001 2C00	APB2	0x4001 0000
TIM8	NA			0x4001 0400
USART1	APB2	0x4001 3800		0x4001 1000
USART6	NA			0x4001 1400
ADC1	APB2	0x4001 2400		0x4001 2000
SPI4	NA			0x4001 3400
SYSCFG				0x4001 3800
TIM9	APB2	0x4001 4C00		0x4001 4000
TIM10		0x4001 5000		0x4001 4400
TIM11		0x4001 5400		0x4001 4800

Table 8. Bus mapping differences between STM32F1 Series and STM32F401/410/411/412/413/423 lines (continued)

Peripheral	STM32F1 Series		STM32F401/410/411/412/413/423 lines	
	Bus	Base address	Bus	Base address
SPI5	NA		APB2	0x4001 5000
DFSDM1				0x4001 6000(2)
DFSDM2				0x4001 6400(1)
SAI1				0x4001 5800(1)
UART10				0x4001 1C00(1)
UART9				0x4001 1800(1)
ADC3	APB2	0x4001 3C00	NA	
ADC2		0x4001 2800		
GPIOA		0x4001 0800	AHB1	0x4002 0000
GPIOB		0x4001 0C00		0x4002 0400
GPIOC		0x4001 1000		0x4002 0800
GPIOD		0x4001 1400		0x4002 0C00
GPIOE		0x4001 1800		0x4002 1000
GPIOF		0x4001 1C00		0x4002 1400
GPIOG		0x4001 2000		0x4002 1800
GPIOH	NA			0x4002 1C00
AES			AHB2	0x5006 0000(4)
RNG				0x5006 0800(5)
SDIO/SDMMC	AHB	0x4001 8000	APB2	0x4001 2C00

1. Only available in STM32F413/423 line.
2. Only available in STM32F412/413/423 lines.
3. Only available in STM32F410/413/423 lines.
4. Only available in the STM32F423 device.
5. Only available in STM32F410/412/413/423 lines.

Note: For more details about the system memory mapping please refer to reference manual or datasheet.

3.3 DMA

The STM32F401/410/411/412/413/423 lines implement an ‘enhanced’ DMA compared to the STM32F1 Series:

- The STM32F1 Series embeds two DMA controllers, each controller has up to 7 channels. Each channel is dedicated to managing memory access requests from one or more peripherals. It has an arbiter for handling the priority between DMA requests.
- The STM32F401/410/411/412/413/423 lines embed two DMA controllers, each controller has 8 streams, and each stream is dedicated to managing memory access requests from one or more peripherals. Each stream can have up to 8 channels (requests) in total. Each has an arbiter for handling the priority between DMA requests.

Table 9 presents the correspondence between the peripheral DMA requests in the STM32F401/410/411/412/413/423 lines and in the STM32F1 Series.

Table 9. DMA request differences migrating from STM32F1 Series to STM32F401/410/411/412/413/423 lines

Peripheral	DMA request	STM32F1 Series	STM32F401/410/411/412/413/423 lines
ADC1	ADC1	DMA1_Channel1	DMA2_Stream0 DMA2_Stream4
ADC3	ADC3	DMA2_Channel5	NA
DAC	DAC1	DMA2_Channel3	DMA1_Stream5(1)(2)
	DAC2	DMA2_Channel4	DMA1_Stream6(2)
SPI1	SPI1_Rx	DMA1_Channel2	DMA2_Stream0 DMA2_Stream2
	SPI1_Tx	DMA1_Channel3	DMA2_Stream3 DMA2_Stream5 DMA2_Stream2(2)
SPI2	SPI2_Rx	DMA1_Channel4	DMA1_Stream3
	SPI2_Tx	DMA1_Channel5	DMA1_Stream4
SPI3	SPI3_Rx	DMA2_Channel1	DMA1_Stream0 DMA1_Stream2
	SPI3_Tx	DMA2_Channel2	DMA1_Stream5 DMA1_Stream7
SPI4	SPI4_Rx	NA	DMA2_Stream0(3) DMA2_Stream3(3) DMA2_Stream4(2)
	SPI4_Tx		DMA2_Stream1(3) DMA2_Stream4(3)
SPI5	SPI5_Rx	NA	DMA2_Stream5(4) DMA2_Stream3(5)
	SPI5_Tx		DMA2_Stream5(4) DMA2_Stream6(4) DMA2_Stream4(5)
USART1	USART1_Rx	DMA1_Channel5	DMA2_Stream2 DMA2_Stream5
	USART1_Tx	DMA1_Channel4	DMA2_ Stream7
USART2	USART2_Rx	DMA1_Channel6	DMA1_Stream5 DMA1_ Stream7
	USART2_Tx	DMA1_Channel7	DMA1_Stream6
USART3	USART3_Rx	DMA1_Channel3	DMA1_Stream1
	USART3_Tx	DMA1_Channel2	DMA1_Stream3 DMA1_Stream4(2)

Table 9. DMA request differences migrating from STM32F1 Series to STM32F401/410/411/412/413/423 lines (continued)

Peripheral	DMA request	STM32F1 Series	STM32F401/410/411/412/413/423 lines
UART4	UART4_Rx	DMA2_Channel3	DMA1_Stream2(2)
	UART4_Tx	DMA2_Channel5	DMA1_Stream4(2)
USART6	USART6_Rx	NA	DMA2_Stream1 DMA2_Stream2
	USART6_Tx		DMA2_ Stream6 DMA2_ Stream7
I2C1	I2C1_Rx	DMA1_Channel7	DMA1_Stream0 DMA1_Stream5
	I2C1_Tx	DMA1_Channel6	DMA1_Stream6 DMA1_Stream7 DMA1_Stream1(2)(5)
I2C2	I2C2_Rx	DMA1_Channel5	DMA1_Stream2 DMA1_Stream3
	I2C2_Tx	DMA1_Channel4	DMA1_Stream7
I2C3	I2C3_Rx	NA	DMA1_Stream1 DMA1_Stream2
	I2C3_Tx		DMA1_Stream4 DMA1_Stream5
SDIO	SDIO	DMA2_Channel4	DMA2_Stream3 DMA2_Stream6
TIM1	TIM1_UP	DMA1_Channel5	DMA2_Stream5
	TIM1_TRIG	DMA1_Channel4	DMA2_Stream0 DMA2_Stream4
	TIM1_COM	DMA1_Channel4	DMA2_Stream4
	TIM1_CH1	DMA1_Channel2 DMA1_Channel6	DMA2_Stream1 DMA2_Stream3 DMA2_Stream6
	TIM1_CH2	DMA1_Channel6	DMA2_Stream2 DMA2_Stream6
	TIM1_CH3	DMA1_Channel6	DMA2_Stream6
	TIM1_CH4	DMA1_Channel4	DMA2_Stream4

Table 9. DMA request differences migrating from STM32F1 Series to STM32F401/410/411/412/413/423 lines (continued)

Peripheral	DMA request	STM32F1 Series	STM32F401/410/411/412/413/423 lines
TIM2	TIM2_UP	DMA1_Channel2	DMA1_Stream1 DMA1_Stream7
	TIM2_CH1	DMA1_Channel5	DMA1_Stream5
	TIM2_CH2	DMA1_Channel7	DMA1_Stream6
	TIM2_CH3	DMA1_Channel1	DMA1_Stream1
	TIM2_CH4	DMA1_Channel7	DMA1_Stream6 DMA1_Stream7
TIM3	TIM3_UP	DMA1_Channel3	DMA1_Stream2
	TIM3_TRIG	DMA1_Channel6	DMA1_Stream4
	TIM3_CH1	DMA1_Channel6	DMA1_Stream4
	TIM3_CH2	NA	DMA1_Stream5
	TIM3_CH3	DMA1_Channel2	DMA1_Stream7
	TIM3_CH4	DMA1_Channel3	DMA1_Stream2
TIM4	TIM4_UP	DMA1_Channel7	DMA1_Stream6
	TIM4_CH1	DMA1_Channel1	DMA1_Stream0
	TIM4_CH2	DMA1_Channel4	DMA1_Stream3
	TIM4_CH3	DMA1_Channel5	DMA1_Stream7
TIM5	TIM5_UP	DMA2_Channel2	DMA1_Stream0 DMA1_Stream6
	TIM5_TRIG	DMA2_Channel1	DMA1_Stream1 DMA1_Stream3
	TIM5_CH1	DMA2_Channel5	DMA1_Stream2
	TIM5_CH2	DMA2_Channel4	DMA1_Stream4
	TIM5_CH3	DMA2_Channel2	DMA1_Stream0
	TIM5_CH4	DMA2_Channel1	DMA1_Stream1 DMA1_Stream3
TIM6	TIM6_UP	DMA2_Channel3	DMA1_Stream1(2)(5)
TIM7	TIM7_UP	DMA2_Channel4	DMA1_Stream2(2)(5) DMA1_Stream4(2)(5)

Table 9. DMA request differences migrating from STM32F1 Series to STM32F401/410/411/412/413/423 lines (continued)

Peripheral	DMA request	STM32F1 Series	STM32F401/410/411/412/413/423 lines
TIM8	TIM8_UP	DMA2_Channel1	DMA2_Stream1
	TIM8_COM	DMA2_Channel2	DMA2_Stream7
	TIM8_TRIG	DMA2_Channel2	DMA2_Stream7
	TIM8_CH1	DMA2_Channel3	DMA2_Stream2
	TIM8_CH2	DMA2_Channel5	DMA2_Stream2 DMA2_Stream3
	TIM8_CH3	DMA2_Channel1	DMA2_Stream2 DMA2_Stream4
	TIM8_CH4	DMA2_Channel2	DMA2_Stream7
QUADSPI(2)(5)	QUADSPI	NA	DMA2_Stream7
DFSDM(2)(5)	DFSDM1_ FLT0	NA	DMA2_Stream0 DMA2_Stream6
	DFSDM1_ FLT1		DMA2_Stream1 DMA2_Stream4
DFSDM2(2)	DFSDM2_ FLT0	NA	DMA2_Stream0 DMA2_Stream4
	DFSDM2_ FLT1		DMA2_Stream1 DMA2_Stream5
	DFSDM2_ FLT2		DMA2_Stream2 DMA2_Stream6
	DFSDM2_ FLT3		DMA2_Stream3 DMA2_Stream7
UART5(2)	UART5_Rx	NA	DMA1_Stream0
	UART5_Tx		DMA1_Stream7
UART7(2)	UART7_Rx	NA	DMA1_Stream3
	UART7_Tx		DMA1_Stream1
UART8(2)	UART8_Rx	NA	DMA1_Stream6
	UART8_Tx		DMA1_Stream0
UART9(2)	UART9_Rx	NA	DMA2_Stream7
	UART9_Tx		DMA2_Stream0
USART10(2)	USART10_RX	NA	DMA2_Stream3 DMA2_Stream0
	USART10_TX		DMA2_Stream5 DMA2_Stream7

Table 9. DMA request differences migrating from STM32F1 Series to STM32F401/410/411/412/413/423 lines (continued)

Peripheral	DMA request	STM32F1 Series	STM32F401/410/411/412/413/423 lines
SAI1(2)	SAI1_A	NA	DMA2_Stream1 DMA2_Stream3
	SAI1_B		DMA2_Stream4 DMA2_Stream5
AES(6)	AES_IN	NA	DMA2_Stream6
	AES_OUT		DMA2_Stream5

1. Only available in STM32F410 line.
2. Only available in STM32F413/423 line.
3. Not applicable for STM32F410 line.
4. Not applicable for STM32F401/410 lines.
5. Only available in STM32F412 line.
6. Only available in the STM32F423 device.

3.4 Interrupts

Table 10 presents the interrupt vectors in the STM32F401/410/411/412/413/423 lines versus the STM32F1 Series.

Table 10. Interrupt vector differences between STM32F401/410/411/412/413/423 lines and STM32F1 Series

Position	STM32F1 Series	STM32F401/410/411/412/413/423 lines
0	WWDG	WWDG
1	PVD	PVD
2	TAMPER	TAMP_ STAMP
3	RTC	RTC_WKUP
4	FLASH	FLASH
5	RCC	RCC
6	EXTI0	EXTI0
7	EXTI1	EXTI1
8	EXTI2	EXTI2
9	EXTI3	EXTI3
10	EXTI4	EXTI4
11	DMA1_Channel1	DMA1_Stream0
12	DMA1_Channel2	DMA1_Stream1
13	DMA1_Channel3	DMA1_Stream2
14	DMA1_Channel4	DMA1_Stream3
15	DMA1_Channel5	DMA1_Stream4
16	DMA1_Channel6	DMA1_Stream5
17	DMA1_Channel7	DMA1_Stream6
18	ADC1_2	ADC
19	CAN1_TX / USB_HP_CAN_TX	CAN1_TX
20	CAN1_RX0 / USB_LP_CAN_RX0	CAN1_RX0
21	CAN1_RX1	CAN1_RX1
22	CAN1_SCE	CAN1_SCE
23	EXTI9_5	EXTI9_5
24	TIM1_BRK / TIM1_BRK _TIM9 (1)	TIM1_BRK / TIM9
25	TIM1_UP / TIM1_UP_TIM10(1)	TIM1_UP / TIM10
26	TIM1_TRG_COM / TIM1_TRG_COM_TIM11(1)	TIM1_TRG_COM / TIM11
27	TIM1_CC	TIM1_CC
28	TIM2	TIM2
29	TIM3	TIM3

Table 10. Interrupt vector differences between STM32F401/410/411/412/413/423 lines and STM32F1 Series (continued)

Position	STM32F1 Series	STM32F401/410/411/412/413/423 lines
30	TIM4	TIM4
31	I2C1_EV	I2C1_EV
32	I2C1_ER	I2C1_ER
33	I2C2_EV	I2C2_EV
34	I2C2_ER	I2C2_ER
35	SPI1	SPI1
36	SPI2	SPI2
37	USART1	USART1
38	USART2	USART2
39	USART 3	USART 3
40	EXTI15_10	EXTI15_10
41	RTC_Alarm	EXTI17 / RTC Alarm
42	OTG_FS_WKUP / USBWakeUp	EXTI18 / OTG_FS WKUP
43	TIM8_BRK / TIM8_BRK_TIM12(1)	TIM8_BRK_TIM12
44	TIM8_UP / TIM8_UP_TIM13(1)	TIM8_UP_TIM13
45	TIM8_TRG_COM / TIM8_TRG_COM_TIM14(1)	TIM8_TRG_COM_TIM14
46	TIM8_CC	TIM8_CC
47	ADC3	DMA1_Stream7
48	FSMC	FSMC
49	SDIO	SDIO
50	TIM5	TIM5
51	SPI3	SPI3
52	UART4	UART4
53	UART5	UART5
54	TIM6 / TIM6_DAC(1)	TIM6_GLB_IT/DAC1/DAC2(1)
55	TIM7	TIM7
56	DMA2_Channel1	DMA2_Stream0
57	DMA2_Channel2	DMA2_Stream1
58	DMA2_Channel3	DMA2_Stream2
59	DMA2_Channel4 / DMA2_Channel4_5(1)	DMA2_Stream3
60	DMA2_Channel5	DMA2_Stream4
61	ETH	DFSDM1_FLT0
62	ETH_WKUP	DFSDM1_FLT1/ EXTI19(1)

Table 10. Interrupt vector differences between STM32F401/410/411/412/413/423 lines and STM32F1 Series (continued)

Position	STM32F1 Series	STM32F401/410/411/412/413/423 lines
63	CAN2_TX	CAN2_TX
64	CAN2_RX0	CAN2_RX0
65	CAN2_RX1	CAN2_RX1
66	CAN2_SCE	CAN2_SCE
67	OTG_FS	OTG_FS
68	NA	DMA2_Stream5
69		DMA2_Stream6
70		DMA2_Stream7
71		USART6
72		I2C3_EV
73		I2C3_ER
74		CAN3_TX
75		CAN3_RX0
76		CAN3_RX1
77		CAN3_SCE
78		N/A
79		CRYPTO
80		RNG
81		FPU
82		UART7
83		UART8
84		SPI4
85		SPI5
87		SAI1
88		UART9
89		UART10
92		Quad-SPI

Table 10. Interrupt vector differences between STM32F401/410/411/412/413/423 lines and STM32F1 Series (continued)

Position	STM32F1 Series	STM32F401/410/411/412/413/423 lines
95	NA	I2CFMP1 event/ I2C4_EV(1)
96		I2CFMP1 error/ I2C4_ER(1)
97		LPTIM1/EXTI23
98		DFSDM2_FLT0
99		DFSDM2_FLT1
100		DFSDM2_FLT2
101		DFSDM2_FLT3
Color key		
	Same feature, but specification change or enhancement	
	Only in STM32F412/413/423 lines	
	Different Interrupt vector	
	Only in STM32F410/413/423 lines	
	Only in STM32F410/413/423 lines	
	Only in STM32F410/412/413/423 lines	
	Only in STM32F413/F423 line	
	Only in STM32F423 device	

1. Depending on the product line used.

3.5 RCC

The main differences related to the RCC (reset and clock controller), between the STM32F1 Series and the STM32F401/410/411/412/413/423 lines, are presented in *Table 11* below.

Table 11. RCC differences between STM32F401/410/411/412/413/423 lines and STM32F1 Series

RCC	STM32F1 Series	STM32F401/410/411/412/413/423 lines
HSI	8 MHz RC factory and user trimmed	16 MHz RC factory and user trimmed
LSI	40 kHz RC	32 kHz
HSE	Connectivity line:(1) 3 - 25 MHz Other lines: 4 - 16 MHz (up to 25 MHz in bypass mode)	4 - 26 MHz
LSE	32.768 kHz (up to 1 MHz in bypass mode) Available in backup domain (VBAT)	32.768 kHz. Configurable drive/consumption (not in STM32F401 lines). Available in backup domain (VBAT).
PLL	Connectivity line(1): 3 PLLs Main PLL sources: HSI/2, HSE, PLL2 (through divider) PLL2, PLL3 clocked by HSE through divider Other lines: 1 PLL The PLL sources are HSI, HSE.	Main PLL for system 1 PLL (PLLI2S) for I2S The PLL sources are HSI, HSE
System clock source	HSI, HSE or PLL	HSI, HSE or PLL
System clock frequency	Up to 72 MHz 8 MHz after reset using HSI	Up to 84 MHz (STM32F401 line), 100 MHz (STM32F410/411/412/413/423 lines) 16 MHz after reset using HSI
AHB frequency	Up to 72 MHz	Up to 84 MHz (STM32F401 line), 100 MHz (STM32F410/411/412/413/423 lines)
APB1 frequency	Up to 36 MHz	Up to 42 MHz (STM32F401 line), 50 MHz (STM32F410/411/412 lines)
APB2 frequency	Up to 72 MHz	Up to 84 MHz (STM32F401 line), 100 MHz (STM32F411 line)
RTC clock source	LSI, LSE or HSE/128	LSI, LSE or HSE (1 MHz) using 1/2, 1/3, ¼ clock pre-divider

Table 11. RCC differences between STM32F401/410/411/412/413/423 lines and STM32F1 Series (continued)

RCC	STM32F1 Series	STM32F401/410/411/412/413/423 lines
MCO clock source	MCO1 pin (PA8): (max 50 MHz) Connectivity line(1): HSI, HSE, SYSCLK, PLLCLK/2, PLL2CLK, PLL3CLK/2, XT1 ext 3-25 MHz (OSC_IN), PLL3CLK Other lines: HSI, HSE, SYSCLK, PLLCLK/2	MCO1 pin (PA8): HSI, LSE, HSE, PLLCLK MCO2 pin (PC9): HSE, PLLCLK, SYSCLK, PLLI2S With configurable prescaler, 1, 2, 3, 4, 5 for each output.
CSS	CSS (Clock Security System) on HSE	CSS (clock security system) on HSE and CSS on LSE
Internal oscillator measurement / calibration	– LSE connected to TIM5 CH4 IC: can measure HSI with respect to LSE clock high precision – LSI connected to TIM5 CH4 IC: can measure LSI with respect to HSI or HSE clock precision – HSE connected to TIM11 CH1 IC: can measure HSE with respect to LSE/HSI clock	
Interrupt	– CSS (linked to NMI IRQ) – LSIRDY, LSERDY, HSIRDY, HSERDY, PLLRDY (linked to RCC global IRQ)	

1. Connectivity line devices are STM32F105xx and STM32F107xx microcontrollers.

In addition to the differences described in *Table 11* above, the following additional adaptation steps may be needed for the migration.

3.5.1 Maximum clock frequency versus Flash wait state

For the STM32F1 the maximum system clock frequency and number of Flash memory wait states are linked by the conditions below:

- zero wait state, if 0 < SYSCLK ≤ 24 MHz
- one wait state, if 24 MHz < SYSCLK ≤ 48 MHz
- two wait states, if 48 MHz < SYSCLK ≤ 72 MHz

For the STM32F401/410/411/412/413/423 lines, the maximum system clock frequency and number of Flash memory wait states depend on the selected voltage range VDD.

Table 12. Number of wait states according to CPU clock (HCLK) frequency for STM32F401 line

Wait states (WS) (LATENCY)	HCLK (MHz)			
	Voltage range 2.7 V - 3.6 V	Voltage range 2.4 V - 2.7 V	Voltage range 2.1 V - 2.4 V	Voltage range 1.71 V - 2.1 V
0 WS (1 CPU cycle)	0 < HCLK ≤ 30	0 < HCLK ≤ 24	0 < HCLK ≤ 18	0 < HCLK ≤ 16
1 WS (2 CPU cycles)	30 < HCLK ≤ 60	24 < HCLK ≤ 48	18 < HCLK ≤ 36	16 < HCLK ≤ 32
2 WS (3 CPU cycles)	60 < HCLK ≤ 84	48 < HCLK ≤ 72	36 < HCLK ≤ 54	32 < HCLK ≤ 48
3 WS (4 CPU cycles)	-	72 < HCLK ≤ 84	54 < HCLK ≤ 72	48 < HCLK ≤ 64
4 WS (5 CPU cycles)	-	-	72 < HCLK ≤ 84	64 < HCLK ≤ 80
5 WS (6 CPU cycles)	-	-	-	80 < HCLK ≤ 84

Table 13. Number of wait states according to CPU clock (HCLK) frequency for STM32F410/411/412 lines

Wait states (WS) (LATENCY)	HCLK (MHz)			
	Voltage range 2.7 V - 3.6 V	Voltage range 2.4 V - 2.7 V	Voltage range 2.1 V - 2.4 V	Voltage range 1.71 V - 2.1 V
0 WS (1 CPU cycle)	0 < HCLK ≤ 30	0 < HCLK ≤ 24	0 < HCLK ≤ 18	0 < HCLK ≤ 16
1 WS (2 CPU cycles)	30 < HCLK ≤ 64	24 < HCLK ≤ 48	18 < HCLK ≤ 36	16 < HCLK ≤ 32
2 WS (3 CPU cycles)	64 < HCLK ≤ 90	48 < HCLK ≤ 72	36 < HCLK ≤ 54	32 < HCLK ≤ 48
3 WS (4 CPU cycles)	90 < HCLK ≤ 100	72 < HCLK ≤ 96	54 < HCLK ≤ 72	48 < HCLK ≤ 64
4 WS (5 CPU cycles)	-	96 < HCLK ≤ 100	72 < HCLK ≤ 90	64 < HCLK ≤ 80
5 WS (6 CPU cycles)	-	-	90 < HCLK ≤ 100	80 < HCLK ≤ 96
6 WS (7 CPU cycles)	-	-	-	96 < HCLK ≤ 100

Table 14. Number of wait states according to CPU clock (HCLK) frequency for STM32F413/423 line

Wait states (WS) (LATENCY)	HCLK (MHz)			
	Voltage range 2.7 V - 3.6 V	Voltage range 2.4 V - 2.7 V	Voltage range 2.1 V - 2.4 V	Voltage range 1.71 V - 2.1 V
0 WS (1 CPU cycle)	0 < HCLK ≤ 25	0 < HCLK ≤ 20	0 < HCLK ≤ 18	0 < HCLK ≤ 16
1 WS (2 CPU cycles)	25 < HCLK ≤ 50	20 < HCLK ≤ 40	18 < HCLK ≤ 36	16 < HCLK ≤ 32
2 WS (3 CPU cycles)	50 < HCLK ≤ 75	40 < HCLK ≤ 60	36 < HCLK ≤ 54	32 < HCLK ≤ 48
3 WS (4 CPU cycles)	75 < HCLK ≤ 100	60 < HCLK ≤ 80	54 < HCLK ≤ 72	48 < HCLK ≤ 64
4 WS (5 CPU cycles)	-	80 < HCLK ≤ 100	72 < HCLK ≤ 90	64 < HCLK ≤ 80
5 WS (6 CPU cycles)	-	-	90 < HCLK ≤ 100	80 < HCLK ≤ 96
6 WS (7 CPU cycles)	-	-	-	96 < HCLK ≤ 100

In addition to the VDD voltage range specified in above tables, the maximum frequency is limited by the power scale value indicated by software in VOS [1:0] bits of the PWR_CR register.

These bits modify the internal digital logic voltage from the power regulator.

This voltage scaling allows optimization of the power-consumption when the device is clocked at the maximum system frequency.

3.5.2 Peripheral access configuration

Since the address mapping of some peripherals has changed between STM32F401/410/411/412/413/423 lines and the STM32F1 Series, different registers are used to enable/disable the peripheral clock (by mode), or enter/exit reset.

Table 15. RCC registers used for peripheral access configuration

Bus	STM32F1 Series registers	STM32F401/410/411/412/413/423 line registers	Comments
AHB	RCC_AHBRSTR	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2)	Used to [enter/exit] the AHB peripheral from reset
	RCC_AHBENR	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2)	Used to [enable/disable] the AHB peripheral clock
	NA	RCC_AHB1LPENR RCC_AHB2LPENR	Used to [enable/disable] the AHB peripheral clock in Sleep mode
APB1	RCC_APB1RSTR		Used to [enter/exit] the APB1 peripheral from reset
	RCC_APB1ENR		Used to [enable/disable] the APB1 peripheral clock
	NA	RCC_APB1LPENR	Used to [enable/disable] the APB1 peripheral clock in Sleep mode
APB2	RCC_APB2RSTR		Used to [enter/exit] the APB2 peripheral from reset
	RCC_APB2ENR		Used to [enable/disable] the APB2 peripheral clock
	NA	RCC_APB2LPENR	Used to [enable/disable] the APB2 peripheral clock in Sleep mode

3.5.3 Peripheral clock configuration

Some peripherals have a dedicated clock source independent of the system clock, which is used to generate the clock required for their operation.

Table 16. Peripheral clock configuration

Peripheral	STM32F1 Series	STM32F401/410/411/412/413/423 lines
USB	In STM32F1 Series (connectivity device only), The USB 48 MHz clock is derived from the main PLL VCO output.	The USB 48 MHz clock is derived from the PLL48CLK main PLL 'Q' output.
SDIO/SDMMC	The SDIO AHB interface clock (SDIOCLK) is derived from the system clock and is equal to HCLK/2 (HCLK = AHB clock), while the SDIO adapter clock equals HCLK	The SDIO clock (SDIOCLK) is derived from the PLL48CLK main PLL 'Q' output and should be less than 48 MHz
RTC	The RTC clock is derived from one of the three following sources: – LSE clock – LSI clock – HSE divided by 128	The RTC clock is derived from one of the three following sources: – LSE clock – LSI clock – HSE divided by prescaler (1 to 31) and should be equal to 1 MHz
I2C	The I2C clock is APB1 clock (PCLK1)	
I2S	The I2S clocks are derived from one of the two following sources: – SYSCLK (system clock) – PLL3VCO (= 2x PLL3CLK) (only on connectivity devices).	The I2S clocks are derived from one of the two following sources: – an external clock I2S_CKIN – PLLI2SCLK

3.6 PWR

For STM32F401/410/411/412/413/423 lines the PWR controller presents some differences versus the F1 Series. These differences are summarized in *Table 17*.

Table 17. PWR differences between STM32F401/410/411/412/413/423 lines and STM32F1 Series

PWR	STM32F1 Series	STM32F401/410/411/412/413/423 lines
Power supplies	**VDD = 2.0 to 3.6 V**: external power supply for I/Os and the internal regulator. Provided externally through VDD pins.	**VDD = 1.7 to 3.6 V** (when internal voltage regulator is disabled) VDD = 1.8 to 3.6 V (when internal voltage regulator is enabled) External power supply for I/Os, Flash memory and internal regulator. It is provided externally through VDD pins.
	VSSA, VDDA = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to VDDA is 2.4 V when the ADC or DAC is used). VDDA and VSSA must be connected to VDD and VSS, respectively.	**VSSA, VDDA: 1.8 V to 3.6 V** (1.7V with external power-supply supervisor). VDDA is the external analog power supply for A/D and D/A converters. VDDA and VSSA must be connected to VDD and VSS respectively.
	VBAT = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present.	**VBAT = 1.65 to 3.6 V**: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present.
	VCORE = 1.8 V VCORE is the power supply for digital peripherals, SRAM and Flash memory. It is generated by an internal voltage regulator. In Stop mode the regulator supplies low-power preserving contents of registers and SRAM.	**VCORE = 1.2 V** (scalable). VCORE is the power supply for digital peripherals, SRAM and Flash memory. It is generated by an internal voltage regulator. The voltage regulator requires one or two external capacitors connected to dedicated pins VCAP_1, VCAP_2. In application Run mode, the voltage regulator output voltage can be scaled by software (lowered) to save power consumption when the device is clocked below the maximum frequency.
	VDD and VDDA must be at the same voltage value.	
Battery backup domain	RTC with backup registers (80 bytes) LSE PC13 to PC15 I/Os	
Power supply supervisor	– Integrated POR / PDR circuitry Programmable voltage detector (PVD) – NA	– Integrated POR / PDR circuitry Programmable voltage detector (PVD) – Brownout reset (BOR) BOR can be disabled after power-on

Table 17. PWR differences between STM32F401/410/411/412/413/423 lines and STM32F1 Series (continued)

PWR	STM32F1 Series	STM32F401/410/411/412/413/423 lines
Low-power modes	– Sleep mode – Stop mode (all clocks are stopped) – Standby mode (VCORE domain powered off)	
Wake-up sources	Sleep mode: – Any peripheral interrupt/wakeup event Stop mode: – Any EXTI line event/interrupt – PVD, RTC Standby mode: – WKUP pin (PA0) rising edge – RTC event – External reset in NRST pin – IWDG reset	

3.7 RTC

The STM32F401/410/411/412/413/423 lines and STM32F1 Series implement different RTC versions.

Table 18. RTC differences between STM32F401/410/411/412/413/423 lines and STM32F1 Series

RTC	STM32F1 Series	STM32F401/410/411/412/413/423 lines
Features	32-bit programmable counter. Programmable prescaler (divider up to 2^{20}). 32-bit programmable Alarm register. Alarm interrupt, Second interrupt for periodic interrupt signal, Overflow interrupt.	Calendar with sub-seconds, seconds, minutes, hours, day, date, month, year. Programmable alarm with interrupt function. The alarm can be triggered by any combination of the calendar fields. – Automatic wakeup unit – Includes 80 bytes backup registers. Enhanced precision, digital calibration circuit (0.95ppm accuracy) – Time-stamp for event saving. Tamper detection event.

Note: For more information about RTC features, please refer to the RTC chapter of the related product reference manuals.

3.8 GPIO

The STM32F401/410/411/412/413/423 lines' GPIO peripheral embeds identical features to the STM32F1 Series.

Minor adaptation of the code written for the F1 Series using the GPIO may be required on STM32F401/410/411/412/413/423 lines due to:

- Mapping of particular functions on different GPIOs (see pinout difference in *Section 1: Hardware migration*)
- Alternate function selection differences (AFSELy[3:0] in registers GPIOx_AFRL and GPIOx_AFRH).

The main GPIO features are:

- GPIO mapped on AHB bus for better performance.
- I/O pin multiplexer and mapping. Pins are connected to on-chip peripherals/modules through a multiplexer that allows only one peripheral alternate function (AF) to be connected to an I/O pin at a time. In this way, there cannot be any conflict between peripherals sharing the same I/O pin.

3.9 EXTI

The external interrupt/event controller (EXTI) is very similar on both STM32F1 and STM32F401/410/411/412/413/423 lines. *Table 19* shows the main differences.

Table 19. EXTI differences between STM32F1 Series and STM32F401/410/411/412/413/423 lines

EXTI	STM32F1 Series	STM32F401/410/411/412/413/423 lines
Number of event/interrupt lines	Up to 20 configurable lines	Up to 23 configurable lines

3.10 Flash

Table 20 presents the difference between the FLASH interface of the STM32F401/410/411/412/413/423 lines and the STM32F1 Series.

Table 20. Flash differences between STM32F1 Series and STM32F401/410/411/412/413/423 lines

Flash	STM32F1 Series	STM32F401/410/411/412/413/423 lines
Main/Program memory	0x0800 0000 – (up to) 0x080F FFFF	0x0800 0000 – (up to) 0x081F FFFF
	For XL-density devices: Up to 1 Mbyte Split into 2 banks Each bank: 256 pages of 2 Kbytes Each page: 8 rows of 256 bytes (Other devices have smaller memory size and only 1 bank, see RM0008 for details) Programming granularity: 16 bits Read granularity: 128 bits	Up to 1 Mbyte (up to 1.5 Mbytes for STM32F413xx/423xH devices) 4 sectors of 16 Kbytes 1 sector of 64 Kbytes 1,3,7 or 11 sectors of 128 Kbytes Programming granularity: 8, 16, 32, 64 bits Read granularity: 128 bits
Features	for XL-density device: read while write (RWW) Dual bank boot	-
Wait state	Up to 2 (depending on the frequency)	Up to 6 (depending on the supply voltage and frequency)
Accelerator	Pre-fetch buffer (2x64-bit words)	ART accelerator™: allowing 0 wait state when executing from the cache.
One time programmable (OTP)	NA	512 OTP bytes
Erase granularity	Page erase (1 Kbyte or 2 Kbytes) and mass erase	Sector and mass erase
Read protection (RDP)	No protection: RDP = 0x00A5, nRDP = 0xFF5A Protection: RDP = 0xFF = nRDP	Level 0 no protection RDP = 0xAA Level 1 memory protection RDP ≠ {0xAA, 0xCC} Level 2 RDP = 0xCC(1)
Proprietary code readout protection (PCROP)	NA	Granularity: 1 sector
Write protection (WRP)	Granularity: low, medium density devices: – 4 pages other devices: – 2 pages from page 0 to 61 – remaining pages from page 62 as a whole	Granularity: 1 sector

1. Memory read protection level 2 is an irreversible operation. When level 2 is activated, the level of protection cannot be decreased to level 0 or level 1.

3.11 ADC

Table 21 presents the differences between the ADC peripheral of STM32F1 Series and STM32F401/410/411/412/413/423 lines.

Table 21. Differences between the ADC peripheral of STM32F1 Series and STM32F401/410/411/412/413/423 lines

ADC	STM32F1 Series	STM32F401/410/411/412/413/423 lines
ADC type	SAR structure	
Instances	Up to 3 instances (STM32F103xC/D/E/F/G)	1 instance
Maximum sampling frequency	Up to 2 Msps in interleaved mode (STM32F105/107xx)	2.4 Msps
Number of channels	Up to 21 channels (STM32F103xC/D/E/F/G)	Up to 16 channels
Resolution	12-bit	
Conversion modes	Single / continuous / scan / discontinuous Dual mode	Single / continuous / scan / discontinuous
DMA	Yes	
Supply requirement	2.4 V to 3.6 V	1.8 V to 3.6 V (1.7 V with external power-supply supervisor)
Reference Voltage	External 2.4 V to VDDA	External VDDA - VREF+ < 1.2 V
Electrical Parameters	160 µA (Typ) on VREF DC current 0.8 mA (Typ) on VDDA DC current	300 µA (Typ.) on VREF DC current 1.8 mA (Typ.) on VDDA DC current
Input range	VREF- ≤ VIN ≤ VREF+	VREF- ≤ VIN ≤ VREF+

4 Revision history

Table 22. Document revision history

Date	Revision	Changes
18-Oct-2016	1	Initial release.
02-Dec-2016	2	Enlarged scope to include STM32F413/423 line.