**Introduction**

The STEVAL-POE002V1 power device evaluation board is equipped with a DC-DC converter stage, managed by the PM8804 controller, which provides 40 W (5 V-8 A) on the output.

The DC-DC converter stage is based on the fixed frequency Flyback topology with a secondary synchronous rectification managed by the controller via gate driver transformer.

The evaluation board embeds also the PM8805 controller, dedicated to the Ethernet interface (compliant with the Standard IEEE802.3.af/at/bt) and to the full active bridge rectification.

![Figure 1. STEVAL-POE002V1 evaluation board](image-url)
### 1. STEVAL-POE002V1 evaluation board overview

#### 1.1 Specifications, connectors and LEDs

**Table 1. STEVAL-POE002V1 specifications**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$ at RJ45 connector</td>
<td>From 41.2 to 57 V</td>
</tr>
<tr>
<td>$I_{IN}$ at RJ45 connector</td>
<td>1.0 A max. each pair</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>5 V ± 5%</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>8 A</td>
</tr>
<tr>
<td>Max. output power</td>
<td>40 W</td>
</tr>
<tr>
<td>Efficiency overall peak</td>
<td>&gt;90% full load</td>
</tr>
<tr>
<td>DC-DC efficiency</td>
<td>&gt;91% full load</td>
</tr>
<tr>
<td>Peak to peak output ripple at full load</td>
<td>50 mV</td>
</tr>
<tr>
<td>Transient response $ΔV$ pk-pk 100% to 50% load step</td>
<td>≈700 mV</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>≈ 280 KHz</td>
</tr>
</tbody>
</table>

**Table 2. STEVAL-POE002V1 connectors**

<table>
<thead>
<tr>
<th>Reference</th>
<th>Type</th>
<th>Specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>RJ45 connector</td>
<td>Data and power input</td>
</tr>
<tr>
<td>J2</td>
<td>RJ45 connector</td>
<td>Data output</td>
</tr>
<tr>
<td>J9</td>
<td>Power jack</td>
<td>Front Aux</td>
</tr>
<tr>
<td>J10</td>
<td>Power jack</td>
<td>Rear Aux</td>
</tr>
<tr>
<td>J4, TP9</td>
<td>Banana jack/turret</td>
<td>Positive of $V_{OUT}$</td>
</tr>
<tr>
<td>J6, TP10</td>
<td>Banana jack/turret</td>
<td>Negative of $V_{OUT}$ (Sec GND)</td>
</tr>
<tr>
<td>P1</td>
<td>Push button</td>
<td>SLEEP/WKUP</td>
</tr>
<tr>
<td>P2</td>
<td>Push button</td>
<td>SHDN</td>
</tr>
</tbody>
</table>

**Table 3. STEVAL-POE002V1 LEDs**

<table>
<thead>
<tr>
<th>Reference</th>
<th>Type</th>
<th>Function</th>
<th>Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>D4</td>
<td>Green LED</td>
<td>Monitor of T2 signal</td>
<td>LED on when T2 is low</td>
</tr>
<tr>
<td>D5</td>
<td>Green LED</td>
<td>Monitor of T1 signal</td>
<td>LED on when T1 is low</td>
</tr>
<tr>
<td>D6</td>
<td>Green LED</td>
<td>Monitor of T0 signal</td>
<td>LED on when T0 is low</td>
</tr>
<tr>
<td>D15</td>
<td>Green LED</td>
<td>Monitor of $V_{OUT}$</td>
<td>LED on when $V_{OUT}$ is present</td>
</tr>
<tr>
<td>D39</td>
<td>Green LED</td>
<td>Monitor of FAUX signal</td>
<td>LED on when frontal aux is present</td>
</tr>
<tr>
<td>D40</td>
<td>Green LED</td>
<td>Monitor of STBY signal</td>
<td>LED on when STBY is high</td>
</tr>
</tbody>
</table>
### Table 4. Tx signal possible configurations

<table>
<thead>
<tr>
<th>Classification</th>
<th>T0</th>
<th>T1</th>
<th>T2</th>
<th>Bridges</th>
<th>Finger number</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type 1 (13 W)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0 or 1</td>
<td>Legacy type</td>
<td></td>
</tr>
<tr>
<td>Type 2 (25.5 W)</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>2, 3</td>
<td>Legacy type</td>
<td></td>
</tr>
<tr>
<td>Type 3 (51 W)</td>
<td>1</td>
<td>0</td>
<td>2</td>
<td>4</td>
<td>New PD type</td>
<td></td>
</tr>
<tr>
<td>Type 4 (71 W)</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>≥ 5</td>
<td>New PD type</td>
<td></td>
</tr>
<tr>
<td>Type 3 on 4 pairs (13 W), or legacy 4 pairs (type 1 class)</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>2</td>
<td>0 or 1</td>
<td>New PD type</td>
</tr>
<tr>
<td>Type 3 on 4 pairs (25.5 W), or legacy 4 pairs (type 2 class)</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
<td>2, 3</td>
<td>New PD type</td>
</tr>
<tr>
<td>Rear AUX</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>any</td>
<td>N.A.</td>
<td>Aux present</td>
</tr>
<tr>
<td>Front AUX</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>N.A.</td>
<td>Aux present</td>
</tr>
</tbody>
</table>

The STEVAL-POE002V1 evaluation board is classified as type 3 and class 6. The default status of Tx signal is 000.

**Note:**  
Level 0 or low means the corresponding LED is on; level 1 or high means the LED is off.

### 1.2 Board setup

The STEVAL-POE002V1 evaluation board combines the PM8805 PD interface, compliant with the 802.3bt IEEE PoE standard, and the PM8804 PWM controller.

**Figure 2. STEVAL-POE002V1 evaluation board components**

- 1. POE IN
- 2. RAUX IN
- 3. DATA OUT
- 4. FAUX IN
- 5. OUTPUT
- 6. SLEEP
- 7. WAKE UP
When you use a bench power supply, follow the steps below.

**Step 1.** Set the power supply current limit to 50 mA  
**Step 2.** Apply 10 V and check the input current is 350-390 µA  
**Step 3.** Apply 20 V and check the input current is within the selected Class range (the default is Class 6, 39 mA ±2 mA)  
**Step 4.** Apply 48 V and check the input current is <30 mA and the output voltage is 5 V (without load)  
**Step 5.** Change the current limit to 1 A  
**Step 6.** Connect an electronic load between V_OUT and the sec GND  
**Step 7.** Turn the power supply on (48 V) and check the input current is coherent with the load current setting and the converter expected efficiency. For example, 5 V x 8 A = 40 W → expected efficiency is 90% so P_IN = 40/0.90=44.5 W, which, with 48 V as input voltage, gives input = 44.5/48 =930 mA  
**Step 8.** Change the load current as needed

### 1.3 Configurations

#### 1.3.1 PM8805 configurations

**Table 5. PM8805 control signal description**

<table>
<thead>
<tr>
<th>PM8805 behavior, standard operations</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FAUX</td>
<td>RAUX</td>
</tr>
<tr>
<td>Normal POE operation</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Sby PoE operation</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Front Aux operation</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Rear Aux operation</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

**Additional non standard operations**

| | FAUX | RAUX | STBY | PGD | Hot swap | Charge pump | Active bridge | MPS |
| Sleep mode/Wake up | 1 | 1 | 1 | 0 | Open | Off | LS enabled HS OFF | On |
| Rear Aux with MPS | 0 | 1 | 1 | 1 | Open | Off | LS enabled HS OFF | On |
| Shutdown/reboot | 1 | 1 | 0 | 0 | Open | Off | Off | Off |

#### 1.3.2 PoE

The STEVAL-POE002V1 evaluation board default operation mode is the PoE (0,0,0). The selected class resistors are 36.5 ohm for CLS1 and 150 ohm for CLS2, so the board is class 6; that is, the Tx LED configuration is 100 with T0 LED in off condition. The other classes can be adjusted using the following table.

**Table 6. PM8805 class description**

<table>
<thead>
<tr>
<th>PD class</th>
<th>CLS1 resistor (Ω)</th>
<th>CLS2 resistor (Ω)</th>
<th>Min. (mA)</th>
<th>Max. (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class 0</td>
<td>2 K</td>
<td>2 K</td>
<td>0</td>
<td>4.0</td>
</tr>
<tr>
<td>Class 1</td>
<td>150</td>
<td>150</td>
<td>9.0</td>
<td>12.0</td>
</tr>
<tr>
<td>Class 2</td>
<td>80.6</td>
<td>80.6</td>
<td>17.0</td>
<td>20.0</td>
</tr>
</tbody>
</table>
Classification phase is valid only for PoE devices, so it is not required when connected to any non-PoE power source such as a wall adapter: in those cases, the CLS buffers are never turned on.

Depending on the PD type and class, the relevant PD electrical parameters are summarized in the table below.

<table>
<thead>
<tr>
<th>PD class</th>
<th>CLS1 resistor (Ω)</th>
<th>CLS2 resistor (Ω)</th>
<th>Min. (mA)</th>
<th>Max. (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class 3</td>
<td>51.1</td>
<td>51.1</td>
<td>26.0</td>
<td>30.0</td>
</tr>
<tr>
<td>Class 4</td>
<td>36.5</td>
<td>36.5</td>
<td>36.0</td>
<td>44.0</td>
</tr>
<tr>
<td>Class 5</td>
<td>36.5</td>
<td>2 K</td>
<td>36/0</td>
<td>44/4</td>
</tr>
<tr>
<td>Class 6</td>
<td>36.5</td>
<td>150</td>
<td>36/9</td>
<td>44/12</td>
</tr>
<tr>
<td>Class 7</td>
<td>36.5</td>
<td>80.6</td>
<td>36/17</td>
<td>44/20</td>
</tr>
<tr>
<td>Class 8</td>
<td>36.5</td>
<td>51.1</td>
<td>36/26</td>
<td>44/30</td>
</tr>
</tbody>
</table>

Table 7. PM8805 PD main parameters

<table>
<thead>
<tr>
<th>PD type</th>
<th>Class</th>
<th>CLS1 sign.</th>
<th>CLS2 sign.</th>
<th>Pin (W)</th>
<th>Vin min. (V)</th>
<th>Vin max. (V)</th>
<th>IN max. (mA)</th>
<th>P_peak (W) for 50 ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>13.0</td>
<td>37.0</td>
<td></td>
<td>350</td>
<td>14.4</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>3.84</td>
<td>42.1</td>
<td></td>
<td>90</td>
<td>5.00</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>6.49</td>
<td>40.8</td>
<td></td>
<td>160</td>
<td>8.36</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>13.0</td>
<td>37.0</td>
<td></td>
<td>350</td>
<td>14.4</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>25.5</td>
<td>42.5</td>
<td></td>
<td>600</td>
<td>28.05</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>3.84</td>
<td>42.1</td>
<td></td>
<td>90</td>
<td>5.00</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>6.49</td>
<td>40.8</td>
<td></td>
<td>160</td>
<td>8.36</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>13.0</td>
<td>37.0</td>
<td></td>
<td>350</td>
<td>14.4</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>25.5</td>
<td>42.5</td>
<td></td>
<td>600</td>
<td>28.05</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>4</td>
<td>0</td>
<td>40.0</td>
<td>44.3</td>
<td></td>
<td>900</td>
<td>42</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>4</td>
<td>1</td>
<td>51.0</td>
<td>42.5</td>
<td></td>
<td>1200</td>
<td>53.55</td>
</tr>
<tr>
<td>3</td>
<td>7</td>
<td>4</td>
<td>2</td>
<td>62.0</td>
<td>42.9</td>
<td>57</td>
<td>1440</td>
<td>65.10</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>4</td>
<td>3</td>
<td>71.3</td>
<td>41.2</td>
<td></td>
<td>1730</td>
<td>74.86</td>
</tr>
</tbody>
</table>

1.3.3 FAUX connector

A voltage applied at J9 connector (FAUX) sets automatically the correct input configuration (FAUX=1, RAUX=0, STBY=do not care).

If the STEVAL-POE002V1 evaluation board is already powered by a PSE, the following conditions apply:

1. FAUX voltage lower than PSE voltage: the evaluation board is still powered from PSE and T0,T1,T2 signal configuration remains the same according to Table 4. Tx signal possible configurations
2. FAUX voltage is greater than PSE voltage, but the difference is less than 2 V: a current sharing occurs between PSE and FAUX to supply the evaluation board. T0,T1,T2 signal configuration remains unchanged as in the previous case
3. FAUX voltage is greater than PSE voltage and the difference is greater than 2 V: the evaluation board is powered by FAUX, PSE is disconnected as its load has significantly decreased (~3 mA) and PD does not ensure MPS condition.

The PM8805 device works in Front aux mode (T0=0,T1=0,T2=1). When the FAUX connector (J9) is unplugged, PSE is not connected and the output voltage is interrupted as a new detection/classification procedure must be done before PSE powers the board again.
1.3.4 RAUX with MPS

A voltage applied at J10 connector (RAUX) sets automatically the correct input configuration (FAUX=0; RAUX=1; Stby=1).

The hot swap MOSFET is opened to give prevalence of the RAUX source over the PoE interface.

The STEVAL-POE002V1 evaluation board is configured to put the PSE in MPS mode triggering the STBY pin threshold by a proper divider (R69, R76 and R120) supplied by the RAUX input voltage, to pull the STBY pin up and enable the MPS current, drawn from the PSE.

The RAUX voltage can be in one of the following ranges, depending on the PSE voltage available at RJ45 connector (J1):

- RAUX voltage lower than PSE input voltage of less than 8 V: when RAUX voltage is applied and the evaluation board is already powered by PSE, switching between the two power supply sources works properly. The PM8805 device goes in Rear auxiliary with MPS mode and PSE remains connected to the evaluation board (T0=0,T1=0, T2=1)

![Figure 3. PSE to RAUX switchover at VPSE≈53.5 V, VRAUX≈46 V, I_{OUT}=8 A](image)

- Ch1: VDC input voltage; Ch2: PSE input current
- Ch3: RAUX signal; Ch4: RAUX input current

When RAUX power supply is unplugged from J10, PSE is immediately available to supply the evaluation board, without causing output voltage interruptions, and the PM8805 device goes back to normal operating mode.
Figure 4. RAUX to PSE switchover at $I_{\text{OUT}}=8\, \text{A}$, $V_{\text{RAUX}}=46\, \text{V}$, $PSE=53.5\, \text{V}$

- Ch1: VDC input voltage; Ch2: PSE input current
- Ch3: Vout output voltage; Ch4: RAUX input current

- RAUX voltage lower than PSE input voltage of more than 8 V: when RAUX voltage is applied and the evaluation board is already powered by PSE, switching between the two power supply sources works properly as in the previous case. When RAUX power supply is unplugged from J10, during the switchover, the following failures of the PM8805 hot swap MOSFET might occur:
  - hot swap MOSFET drop between drain and source is greater than the datasheet parameter $V_{\text{ds\_fail}}$ (12 V min./16 V max.)
  - hot swap MOSFET current is greater than the datasheet parameter $\text{Short}$ (4 A min./6 A max.)

If one of these failures occurs, the power good signal is forced to low level according to the datasheet parameter $T_{\text{retry}}$ (9 min./11 max. msec), stopping the Flyback converter switching, then it is released causing an output voltage interruption as shown in the following figure.
Figure 5. RAUX to PSE switchover at $I_{OUT}=8\ A$

- Ch1: VDC input voltage; Ch2: PGD
- Ch3: RAUX signal; Ch4: Vout output voltage

- RAUX voltage is greater than PSE input voltage of at least a diode forward voltage: when RAUX voltage is applied and the evaluation board is already powered by PSE, switching between the two power supply sources works properly as reported in the previous cases, but in this condition MPS current is drawn by RAUX source, then PSE is no more able to stay connected to evaluation board. In this case, when RAUX source is removed, the output voltage goes to zero until PSE has successfully completed detection and classification phases, and the voltage is reapplied to the PD interface.
2 Measurements

2.1 Efficiency

The STEVAL-POE002V1 evaluation board is composed by a PoE interface compliant with the last standard IEEE802.3bt, thanks to the PM8805 interface and a fixed frequency Flyback topology with a secondary synchronous rectification converter that receives DC voltage from the PoE output.

The PM8805 device integrates two N-channel MOSFET bridges, one for every 2 pairs of PoE interfaces and a hot swap MOSFET placed in series to the outputs of the two bridges.

![Figure 6. STEVAL-POE002V1 evaluation board efficiency measurements](image)

The red line indicates the STEVAL-POE002V1overall efficiency at 48 VDC input voltage applied to RJ45 connector J1. The blue line indicates the DC-DC converter eficiency, that does not include the following losses of the associated POE interface section:

- RJ45 connector J1
- PoE data transformer T1
- common chokes T5,T6 placed on the two power supply pairs
- PM8805 interface that integrates the dual POWER MOS bridges and a hot swap MOSFET
- Flyback converter input filter

The DC-DC efficiency is measured between output test points TP9/TP10 and input test points across the input capacitor C28 of the DC-DC Flyback converter.
2.2 Output voltage ripple

Figure 7. Output voltage ripple: input voltage=48 V, $I_{OUT}$ at no load

- Ch3: Vout ripple; Ch4: Iout
Figure 8. Output voltage ripple: input voltage=48 V, I_{OUT} at full load 8 A

- Ch3: Vout ripple; Ch4: Iout
2.3 Input voltage ripple

**Figure 9.** Input voltage ripple before and after Flyback input filter \( I_{\text{OUT}} = 0 \) A

- Ch1: Vin ripple before input filter; Ch2: Primary VGate
- Ch3: Vin ripple after input filter; Ch4: Input current (J1 connector pairs)
Figure 10. Input voltage ripple before and after Flyback input filter \( I_{OUT}=8 \, A, \, V_{IN}=48 \, V \)

- Ch1: Vin ripple before input filter; Ch2: Primary VGate
- Ch3: Vin ripple after input filter; Ch4: Input current (J1 connector pairs)
2.4 Startup

Figure 11. Input voltage at startup: \( I_{\text{out}} = 8 \text{ A} \), \( V_{\text{in}} = 48 \text{ V} \)

- Ch1: PDG; Ch2: Soft start
- Ch3: Primary VGate; Ch4: Input voltage
Figure 12. Output voltage at startup: I_{out}=8 \, A, \, V_{in}=48 \, V

- Ch1: PGD; Ch2: Soft start
- Ch3: Primary VGate; Ch4: Output voltage
2.5 PoE connector unplugged power off

Figure 13. Power off at primary side: Iout=8 A, Vin= 48 V

- Ch1: PGD; Ch2: Soft start
- Ch3: Primary VGate; Ch4: Input voltage
Figure 14. Power off at primary side: $I_{\text{out}}$ at no load, $V_{\text{in}}$= 48 V

- Ch1: PGD; Ch2: Soft start
- Ch3: Primary VGate; Ch4: Input voltage
2.6 Primary side waveforms

Figure 15. Primary/secondary steady state: Iout at no load, Vin=48 V

- Ch1: Primary Q4 VDrain voltage; Ch2: Primary Q4 VGate voltage
- Ch3: Secondary Q1 VDrain voltage; Ch4: Secondary Q1 VGate voltage
Figure 16. Primary steady state: Iout=8 A, Vin=48 V

- Ch1: Primary Q4 VDrain voltage; Ch2: Primary Q4 VGate voltage
- Ch3: Secondary Q1 VDrain voltage; Ch4: Secondary Q1 VGate voltage
2.7 Load transient side waveforms

Figure 17. Load transient: Iout=4 to 8 A, Vin= 48 V

- Ch3: Output voltage; Ch4: Output current
2.8 Overvoltage and overcurrent protections

Figure 18. Overload protection as the first level of OCP (Vin= 48 V)

- Ch1: Primary VCS; Ch2: Primary Q4 VDrain voltage
- Ch3: Soft start;
  Ch4: Input current
Figure 19. Overload protection as the second level of OCP (Vin= 48 V)

- Ch1: Primary VCS; Ch2: Output voltage
- Ch3: Primary VGate; Ch4: Output current
2.9 Gloop measurements

Figure 20. Overvoltage protection (Vin= 48 V, Iout=8 A)
- Ch1: Primary VCS; Ch2: Output voltage
- Ch3: Primary VGate; Ch4: Output current

Figure 21. Gloop plot (Vin= 48 V, Iout=8 A)
2.10 Board thermography

Figure 23. STEVAL-POE002V1 evaluation board thermography at Iout=8 A, Vout=48 V (top view)

A = Q4 ; B = Q1; C = T3;
Figure 24. STEVAL-POE002V1 evaluation board thermography at I_{out}=8\ A, V_{out}=48\ V (bottom view)

A = R_{25}/C_{25}
Figure 25. STEVAL-POE002V1 circuit schematic (1 of 4)

Figure 26. STEVAL-POE002V1 circuit schematic (2 of 4)
Figure 27. STEVAL-POE002V1 circuit schematic (3 of 4)

Figure 28. STEVAL-POE002V1 circuit schematic (4 of 4)

Note the optional circuit on the bottom side.
## Bill of materials

<table>
<thead>
<tr>
<th>Item</th>
<th>Q.ty</th>
<th>Ref.</th>
<th>Part/value</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Order code</th>
</tr>
</thead>
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<tr>
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References

Freely available on www.st.com:
1. PM8804 datasheet
2. PM8805 datasheet
## Revision history

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