Charge pump stress estimation in switching applications

Introduction

The aim of this application note is to provide a criterion for charge pump stress estimation in automotive switching applications.

The present analysis can be exploited to estimate the workload to be accounted for the charge pump when using pre-driver devices.

Peak & Hold injection, electro-valve control and H-Bridge driving can be listed among the most stressing applications in terms of timings and switching frequency.

Independently on the application, this document aims at providing a set of information, equations and criteria useful to choose the correct external transistors and components, along with the switching frequency. The analysis is focused on the charge pump stress induced by these parameters. The ST L9945, an 8-channel configurable HS/LS pre-driver, is considered as the reference device to be used in several applications (P&H, H-Bridge, HS/LS). The ST STD105N10F7AG NMOS transistor is taken as an example of driver used in power applications.

1 Charge pump stress factors

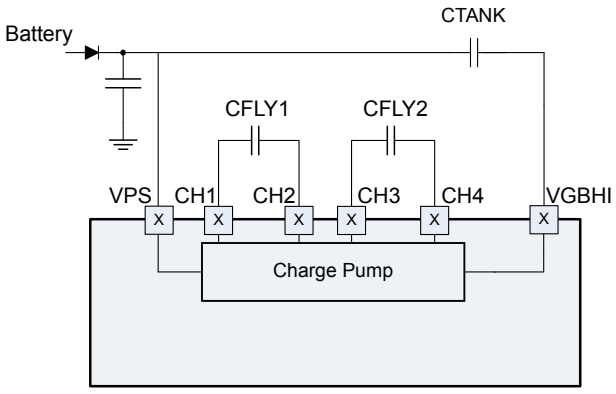
The charge pump works by switching the battery voltage V_{PS} onto flying capacitors and then storing the charge into a tank capacitor by means of a proper circuit re-connection (see Figure 1). Such operation aims at generating an output voltage V_{GBHI} higher than the battery one. This allows using an NMOS transistor to drive the load in both high-side and low-side configurations. PMOS drivers are usually used as high-side switches and do not require any charge pump intervention during switching. The charge pump stress estimation for a single channel must be done accounting for several aspects:

- Charge pump capability
- Target gate-to-source voltage of the external driver
- Charge pump intervention based on driver side (HS/LS)
- External FET gate charge
- External Miller capacitor charge
- External pull down network
- Eventual Internal absorption due to leakage and polarization of pre-driver circuitry
- Tolerance Margin

The control signal switching frequency is also a highly relevant parameter that must be taken in account when analyzing many of the points above.

All these aspects can be analyzed separately and then merged to evaluate final workload.

Figure 1. Charge pump block diagram



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1.1 Charge pump capability

The charge pump capability is a feature depending on the design and varies among different devices. It is usually listed in the electrical characteristics of the device.

A well dimensioned charge pump must guarantee a stable output voltage V_{GBHI} in the worst case applicative scenario foreseen for the flexible device.

As example, Table 1 shows the electrical characteristics of the charge pump embedded in the ST L9945. Focusing on the first row, the charge pump capability is given by the "Test Condition" information.

Note that capability is expressed as the maximum equivalent DC current that charge pump is able to provide. Depending on the internal design, the capability may also vary with the battery voltage.

Therefore, in order to verify the stress induced on the charge pump, it is necessary to estimate the mean current absorbed by each output channel performing different applications. The mean consumption of each channel must be summed and the result compared with the capability.

In this application note, we will consider I_{CP_MAX} = 15 mA as the charge pump capability of the device. However, in case the application requires external FETs to switch also at very low battery, a worst case analysis shall consider a capability of 6 mA only. In fact, in corner cases of deep cold crank, the battery voltage VPS may drop below the 8 V threshold.

Note: Automotive scenarios feature a wide temperature range (typically from -40 °C to +150 °C).

Another fundamental characteristic of a charge pump is represented by its ability to resist to current peaks. When several channels are switching synchronously, all the charge requests overlap in a very short time interval, causing peaks higher than 1 A. A well designed charge pump must take in account the maximum number of channels that can switch simultaneously and must resist to such amount of charge that is instantaneously requested. The robustness against peak current request can be evaluated considering the external tank capacitor C_{TANK}. Eq. (1) can be exploited to estimate the voltage drop occurring on VGBHI during a fast discharge. For instance, a peak current of 1 A, lasting 1 µs, causes a 2.13 V voltage drop on a 470 nF tank capacitor. Refer to Section 3.4 Case study: ST L9945 in application for an example.

Eq:

$$\Delta V_{TANK} = \left(\frac{I_{PEAK}}{C_{TANK}}\right) \times \Delta t_{peak} \quad (1)$$

Table 1. Charge pump electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{VGBHI}	Charge pump voltage versus charge pump load current	V_{VPS} ≥ 8 V; I_{VGBHI} = 15 mA (DC)	VVPS+9	VVPS +12	VVPS+16	V
		V_{VPS_UV} ≤ V_{VPS} < 8 V; I_{VGBHI} = 6 mA (DC)	VVPS+5		VVPS+16	V
f_{CP}	Charge pump frequency	Dependent on t_{SYS}	184	200	216	kHz
C_{TANK}	Charge pump tank capacitor	Connected to VPS I_{VGBHI} = 15 mA	420	470	520	nF
C_{FLY}	Charge pump flying capacitors	Connected between CH1-CH2, CH3-CH4; I_{VGBHI} = 15 mA	198	220	242	nF
V_{CP_UV}	Under voltage threshold	Referenced to VVPS	VVPS+3.9		VVPS+5.1	V
Vh_{CP_UV}	Under voltage hysteresis	Referenced to VVPS	250			mV
t_{CP_UV}	Under voltage filter time		10		30	µs
V_{VGBHI_MAX}	Charge pump max voltage	Referenced to GND			80	V
$t_{CPstartup}$	Startup time		0.05		2	ms

1.2 Target gate-to-source voltage of the external driver

In order to switch on the external FET, the gate-to-source voltage (V_{GS}) must be higher than the ON threshold voltage V_{TH}. Gate threshold voltage (gathered from STD105N10F7AG electrical characteristics) is shown in the table below.

Table 2. On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 100 V			1	µA
		V_{DS} = 100 V, T_C = 125 °C(1)			100	µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 40 A		6.8	8	mΩ

1. *Defined by design, not subject to production test.*

Considering ST STD105N10F7AG NMOS transistor as an example of power MOS, the maximum threshold voltage listed in the electrical characteristics is V_{TH_MAX} = 4.5 V.

In no case V_{GS} must violate the product AMR. In our case, V_{GS_MAX} = 20 V, as highlighted in the table below. It is necessary to operate with V_{GS} >> V_{TH} in order to guarantee the proper overdrive to the external FET, which ensures operating in the switch region. The higher the VGS, the lower the channel parasitic resistance R_{DSon}. On the other hand, the higher the V_{GS}, the higher the charge pump effort in order to inject the gate charge necessary to bias the device, as shown in Figure 3.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	80	A
I_D	Drain current (continuous) at T_C = 100 °C	62	A
I_{DM}(1)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	120	W
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operation junction temperature range		

1. *Pulse width limited by safe operating area.*

The target gate-to-source voltage V_{GS_TYP} is usually a feature of the flexible device and depends on the charge pump internal design. Table 1 shows the typical charge pump output voltage V_{GBHI_TYP} = V_{PS} + 12 V. The voltage step with respect to battery supply VPS will be the target V_{GS_TYP} applied on the external FET when used as HS.

Therefore, for our applications, we will consider V_{GS_TYP} = 12 V.

It is important choosing an external FET compatible with the device target VGS, following the criteria mentioned above. The ST STD105N10F7AG NMOS transistor fits the requirements because:

- V_{TH_MAX} < V_{GS_TYP} < V_{GS_MAX}
- V_{GS_TYP} ≈ 3 * V_{TH_MAX}.

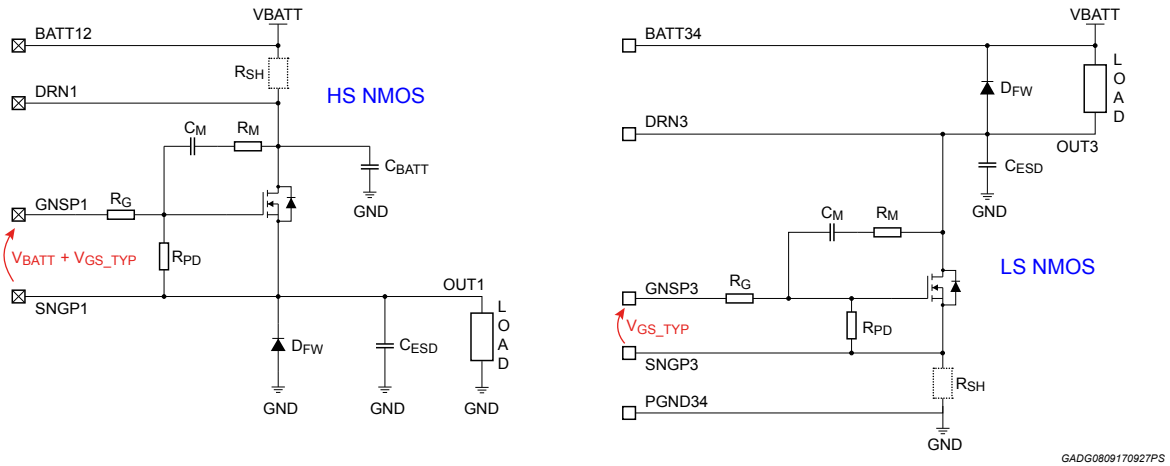
1.3 Charge pump intervention based on driver side (HS/LS)

The main reason behind the implementation of a charge pump is to allow NMOS transistor usage on HS in power applications. Because NMOS has much lower R_{DSon} than the PMOS, it is usually preferred as both LS and HS switch in power applications in order to limit the power losses on the driver and to feed the load with the full battery voltage. However, this requires a charge pump in order to effectively bias the NMOS transistor with a high V_{GS} when the driver is used on HS.

As the battery voltage V_{PS} may undergo severe fluctuations during its operation, some devices make use of the charge pump to drive also the LS NMOS. This helps preventing failure in turning on the FET when battery voltage drops below an acceptable value (e.g. V_{PS} < 6 V). On the other side, using charge pump to bias also LS transistors implies a higher workload in terms of current absorption from the tank capacitor.

For instance, L9945 drives both HS and LS NMOS transistors with the charge pump. Therefore, also LS contributions have to be accounted for when evaluating charge pump stress.

Figure 2. HS and LS NMOS biasing

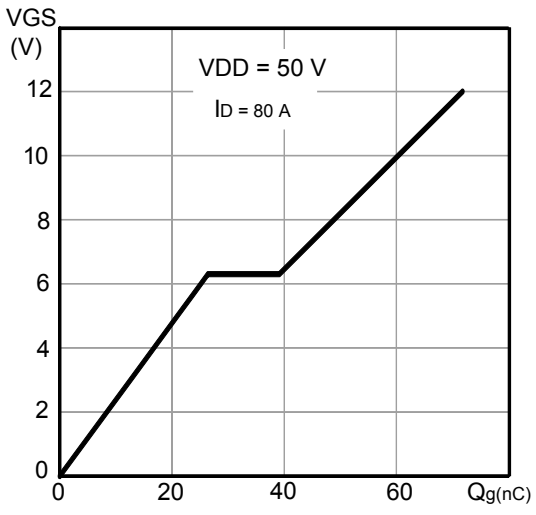


1.4 External FET gate charge

Once the transistor has been chosen according to the criteria mentioned in Target gate-to-source voltage of the external driver, the gate charge needed to switch it on with the target V_{GS_TYP} can be evaluated by looking at the Q_G – V_{GS} graph in its electrical characteristics.

Looking the figure here below, we can estimate that Q_{GS_TYP} = 70 nC is the gate charge needed to bring the gate-to-source voltage up to V_{GS_TYP}.

Figure 3. STD105N10F7AG: Gate charge vs Gate-to-Source Voltage



However, as stated in Section 1.1 Charge pump capability, it is necessary to convert this information into a mean current requirement in order to compare it with the I_{CP_MAX}. Every time the external FET needs to be switched ON, a Q_{GS_TYP} charge pulse must be provided by the charge pump. Therefore, the equivalent DC current can be evaluated dividing the charge injected on the switching period TSW, as shown in the equation below.

Eq: Mean current absorption for switching on the external FET:

$$I_{G_{mean}} = \frac{\Delta Q}{\Delta T} = \frac{Q_{GS_{typ}}}{T_{SW}} = Q_{GS_{typ}} * f_{SW} \quad (2)$$

For instance, if the switching frequency is 20 KHz, given the gate charge estimated above, an IG_MEAN = 1.4 mA is absorbed by the channel under analysis.

1.5 External Miller capacitor charge

In order to improve EMI performances, an external Miller capacitor C_M is usually mounted between gate and drain of the external FET (see Figure 2). This helps smoothing the ON/OFF transitions, thus reducing the electromagnetic emissions. On the other hand, the presence of such capacitor implies an additional amount of charge Q_M to be supplied by the charge pump when switching ON the transistor.

Such contribution depends on FET side and battery supply voltage:

- For HS FETs the gate node voltage swing is $V_{GS\_TYP} + V_{PS}$

  The amount of charge to be stored in C_M is

  Eq:Amount of charge to be stored in the external Miller capacitor for HS NMOS:

$$Q_{M_{HS}} = C_M{}^* \Delta V = C_M{}^* \left(V_{GS_{typ}} + V_{PS} \right) \quad (3)$$

- For LS FETs the gate node voltage swing is V_{GS_TYP}

  The amount of charge to be stored in C_M is

  Eq: Amount of charge to be stored in the external Miller capacitor for LS NMOS:

$$Q_{M_{LS}} = C_M{}^* \Delta V = C_M{}^* V_{GS_{typ}} \quad (4)$$

The dependency on battery supply voltage applies only to HS FETs and varies between Passenger Vehicle (PV) and Commercial Vehicle (CV) applications:

- For PV, the battery voltage is nominally 12 V, but V_{PS} = 14 V should be considered as the typical battery voltage
- For CV, the battery voltage is nominally 24 V, but V_{PS} = 28 V should be considered as the typical battery voltage

For instance, if C_M = 1.5 nF:

- For HS FETs
  - PV: Q_{M_HS} = 39 nC
  - CV: Q_{M_HS} = 60 nC
- For LS FETs, Q_{M_HS} = 18 nC, independently on V_{PS}

These contributions must be converted into mean current absorption aliquots. As for the Section 1.4 External FET gate charge, the Q_M is an impulsive charge that must be supplied every time the external MOS is switched on. Therefore, the equivalent DC current can be evaluated dividing the charge injected on the switching period T_{SW}, as shown in the equation below.

Eq: Mean current absorption for charging the external Miller capacitor

$$I_{M_{mean}} = \frac{\Delta Q}{\Delta T} = \frac{Q_M}{T_{SW}} = Q_M{}^* f_{SW} = \begin{cases} C_M{}^* \left(V_{GS_{typ}} + V_{PS} \right)^* f_{SW}, & for HSFETs \\ C_M{}^* V_{GS_{typ}}{}^* f_{SW}, & for LSFETs \end{cases} \quad (5)$$

For instance, if C_M = 1.5 nF and f_{SW} = 20 KHz:

- For HS FETs
  - PV: I_{M_MEAN} = 780 µA
  - CV: I_{M_MEAN} = 1.2 mA
- For LS FETs, I_{M_MEAN} = 360 µA

Note: The I_{M_MEAN} contribution for LS FETs must be considered only in case the charge pump supplies also LS NMOS.

1.6 External pull down network

In order to avoid wrong biasing of the external drivers at startup, many devices put the output channels in three-state by default. In order to keep the NMOS reliably OFF until the channel is enabled, an external pull down network must be implemented. Usually, a pull down resistor R_{PD} is mounted between gate and source of the NMOS, as shown in Figure 2.

The pull down network insertion adds a permanent current path between the gate node and the ground (directly to GND in case of LS, to GND through the load in case of HS). Such path causes a sort of “leakage” that cannot be neglected when the device is switched ON. Referring to Figure 2:

- When the NMOS is OFF, no current flows through R_{PD} since both gate and source node are brought to GND
- When the NMOS is ON, a V_{GS_TYP} voltage falls on R_{PD}, independently on FET side. Even when the driver is fully switched ON, the charge pump must continuously supply a certain amount of charge to keep it ON, thus balancing the charge subtracted by the pull down path. The current needed depends on the pull-down resistor value. Therefore, it’s recommended to choose a high value (tens of kΩ) for R_{PD} in order not to stress the charge pump. In fact, such resistor is only helpful during the three-state phase at startup, while it has no effect during normal operation since the NMOS is actively switched OFF by the pre-driver.

While the gate charge and the Miller capacitor charge are impulsive contributions, the pull-down network aliquot is a DC contribution to be accounted during the whole ON phase. Therefore, the mean current absorbed by R_{PD} over a period depends on the control signal duty-cycle ($dc_{\%}$).

Eq: Mean current absorption by the pull down network

$$I_{PD_{mean}} = I_{PD_{ON}} * dc_{\%} = \frac{V_{GS_{typ}}}{R_{PD}} * dc_{\%} \quad (6)$$

For instance, if R_{PD} = 47 kΩ and $dc_{\%}$ = 80%, I_{PD_MEAN} ≈ 205 µA.

1.7 Eventual Internal absorption due to leakage and polarization of pre-driver circuitry

The pre-driver device features an internal circuitry needed to control the biasing of the external FET. In addition, internal and external clamping protections might be present to protect both the pre-driver and the FETs against AMR violations. All these circuitries, along with other eventual hissing needed for internal purpose into the IC, may require a biasing current and add some leakage contributions.

The biasing/leakage internal currents are static contributions depending on the pre-driver output state. Therefore, their weight depends on control signal duty-cycle and can be estimated as follows:

Eq: Internal absorption due to biasing of the pre-driver stages and leakage:

$$I_{BIAS_{mean}} = I_{BIAS_{ON}} * dc_{\%} + I_{BIAS_{OFF}} * \left(1 - dc_{\%}\right) \quad (7)$$

Depending on the pre-driver architecture, there could or could not be any DC current consumption from the charge pump; the presence of such a contribution shall be checked either on the datasheet or in a specific pre-driver design guideline provided by designers.

The presence or absence of static internal current consumption directly affects Eq. (9), where I_{BIAS_ON} and I_{BIAS_OFF} can be assumed null in case the architecture under analysis features no internal absorption.

1.8 Tolerance Margin

It is always recommended to consider a TM% additional margin (usually 20%) over the total channel consumption, in order to account all the external leakages and the tolerances of the external components.

2 Total charge pump stress evaluation

By evaluating the stress induced on every channel of the device and summing all the contributions, the total charge pump stress can be evaluated.

In order for the flexible pre-driver to operate correctly, the condition $I_{CP\_MEAN} < I_{CP\_MAX}$ must be verified for all possible configurations.

2.1 Single channel mean absorption

As discussed in Charge pump stress factors the channel mean absorption depends on several aspects. In general, the following contributions must be accounted for:

Eq: Channel mean absorption:

$$I_{CH_{mean}} = \left(I_{G_{mean}} + I_{M_{mean}} + I_{PD_{mean}} + I_{BIAS_{mean}}\right)^{*}(1 + TM_{\%}) \quad (8)$$

Replacing the expressions of each addend in Eq. (8) we provide a formula in order to estimate the consumption for both HS and LS configurations:

Eq: Explicit channel mean absorption for HS and LS configurations

$$I_{CH_{mean}} = \quad (9)$$

$$\begin{cases} \left\{\left[Q_{GS_{typ}} + C_M{}^{*}\left(V_{GS_{typ}} + V_{PS}\right)\right]^{*} f_{SW} + \left(\frac{V_{GS_{typ}}}{R_{PD}} + I_{BIAS_{ON}} - I_{BIAS_{OFF}}\right)^{*} dc_{\%} + I_{BIAS_{OFF}}\right\}^{*}(1 + TM_{\%}) & for\ HS\ FETs \\ \left\{\left[Q_{GS_{typ}} + C_M{}^{*} V_{GS_{typ}}\right]^{*} f_{SW} + \left(\frac{V_{GS_{typ}}}{R_{PD}} + I_{BIAS_{ON}} - I_{BIAS_{OFF}}\right)^{*} dc_{\%} + I_{BIAS_{OFF}}\right\}^{*}(1 + TM_{\%}) & for\ LS\ FETs \end{cases}$$

Where:

- Q_{GS_TYP} is the gate charge to be injected in the external FET in order to generate the VGS_TYP
- C_M is the Miller capacitor mounted between gate and source of the external FET in order to improve EMI behavior
- V_{GS_TYP} is the target gate-to-source voltage of the external FET (usually depends on the pre-driver characteristics)
- V_{PS} is the battery supply voltage
- f_{SW} is the control signal switching frequency
- R_{PD} is the external pull-down resistor used to keep the NMOS OFF in case of pre-driver three-state
- $dc_{\%}$ is the duty-cycle of the control signal
- $TM_{\%}$ is the tolerance margin to account for the pre-driver internal leakage/absorption and for the precision of the external components

Note: If I_{BIAS_ON} and I_{BIAS_OFF} are not indicated in the electrical characteristics table of the charge pump, they could have been already been accounted for in the charge pump capability and therefore they must not be considered in Eq. (9)

2.2 Total charge pump absorption

By simply summing all channel contributions evaluated according Eq. (9), the total charge pump stress can be estimated.

Eq: Total charge pump absorption

$$I_{CP_{mean}} = \Sigma_{i=1}^{N_{CH}} I_{CH_{mean_i}} \quad (10)$$

2.2.1 L9945 Charge pump stress calculator

In order to summarize all the points explored in this paper, the **ST L9945 Charge Pump Stress Calculator** has been developed. Such a tool is a Microsoft Excel® workbook that applies all the equations formulated during our analysis in order to evaluate final stress on the L9945 charge pump.

The tool allows configuring each channel independently and helps understanding how each channel activity will impact on total stress: a simple color code will highlight channels whose mean consumption is above the average expected value (1/8 of the total capacity).

The analysis can be performed for different values of the power supply, including corner cases for cold cranking and load dump. The charge pump capacity is automatically adapted to the selected battery supply scenario.

The tool is contained in a file attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it.

2.3 Key points for a robust configuration

When building a configuration with a flexible pre-driver device, the following key points should be verified:

- When analyzing charge pump stress, it is useful to consider the worst case for the control signal duty-cycle. As discussed in Section 1.6 External pull down network, the higher the duty-cycle, the higher the pull down network absorption is;
- Use HS switches only for critical loads that need to be disconnected from battery supply voltage when not used. HS FETs induce a higher stress on the charge pump as discussed in External Miller capacitor charge;
- It is always recommended to keep the charge pump workload below 80% of the total capacity in order to be robust against phenomena like load dump. During such events, battery voltage may raise up to 35 V (PV) or 60 V (CV) (clamped by external protection circuitry, see Figure 5) for a certain time interval (typ. 500 ms). As a consequence, charge pump stress will increase during such interval due to External Miller capacitor charge. However, no functional issue should occur if a suitable workload margin has been left;
- Charge pump capability is often dependent on battery supply voltage. Events like cold cranking (battery supplying current to electric starter motor in a very cold environment, see Figure 4) may force the battery voltage to drop down to 3 V until the system has been fully started. Usually, charge pump capability is strongly limited under these conditions, and it is very likely to observe failures in trying to control loads. Therefore, when battery voltage drops below an acceptable threshold, it is recommended to disable all the channels that are not safety related in order to guarantee the functionality of the critical features.

Figure 4. Battery voltage profile during a cold cranking event

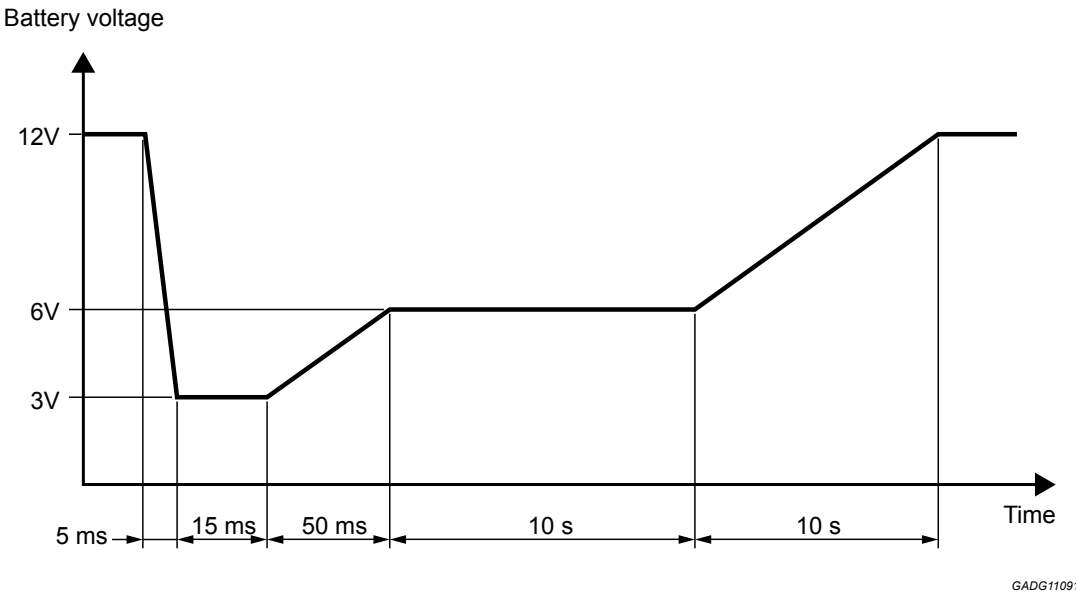
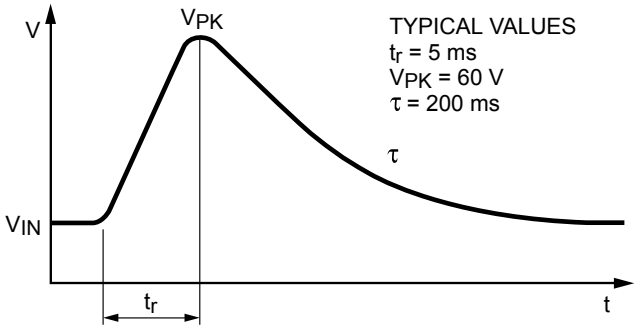


Figure 5. **Load dump in CV systems**



3 Case study: ST L9945 configuration for CV applications

The following case study is based on ST L9945 flexible pre-driver, configured to drive all its 8 channels with independent PWM. Common CV applications are:

- Lambda probe heater control
- Lamp control
- Starter relay
- GDI/PFI Injection
- Oil/Fuel pump control

In the following examples, for all channels the following parameters are considered:

- NMOS: STD105N10F7AG
- VGS_TYP: 12 V
- IBIAS_ON = 530 µA
- IBIAS_OFF = 480 µA

Table 4 shows the configuration under analysis.

Safe and starter relays are implemented with HS switches because they need to disconnect the loads from the battery supply in case of safety issues, system stress or simply when the loads are not used. In general, these switches are always ON during normal operation and therefore their absorption is mainly related to the pull-down network and the internal biasing. When the application may tolerate a certain voltage drop on the battery line (e.g. lamp), a HS PMOS switch can be used as safe relay. This solution is not recommended for injectors: they need the full battery voltage to be applied in order to speed up the needle lifting phase.

All other switches are mounted LS in order to avoid unnecessary charge pump stress when switching. Some of them are permanently switching (lambda probe heater, see Figure 6), some others like injectors switch only during a time window of fixed length which is periodically activated (see Figure 7). Lamps require an initial switching during the inrush phase, and once the lamp is fully lit, the switch is kept ON in a steady state (see Figure 8).

Table 4. L9945 configuration for CV applications

Ch.	Function	Applicative Considerations
1	Safe relay for Injectors	This switch is always ON, unless safety issues occur
2	PFI Injector	Very high frequency due to small current ripple requirements
3	PFI Injector	Very high frequency due to small current ripple requirements
4	Safe relay for Lamps	This switch is always ON, unless safety issues occur (PMOS)
5	Lamp	After initial PWM (≈ 200 Hz), the switch is kept ON. (Worst case is DC)
6	Starter relay	This switch is always ON, unless safety issues occur
7	Lambda Probe Heater	Low frequency because thermal phenomena are slow (≈ 100 Hz)
8	Lamp	After initial PWM (≈ 200 Hz), the switch is kept ON. (Worst case is DC)

Figure 6. **Lambda probe heater control**

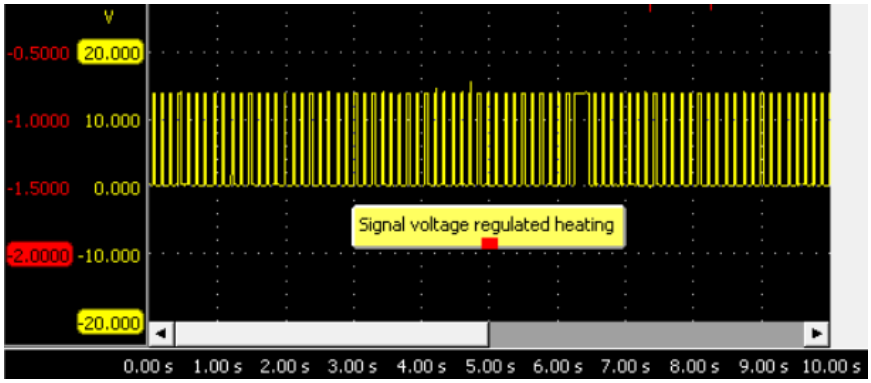


Figure 7. **Peak and Hold injection example**

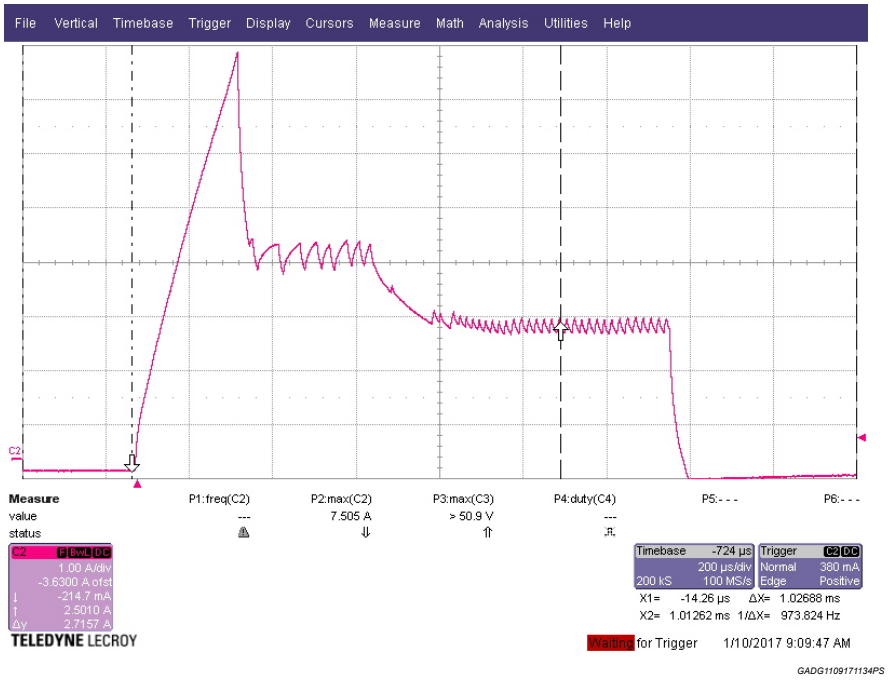
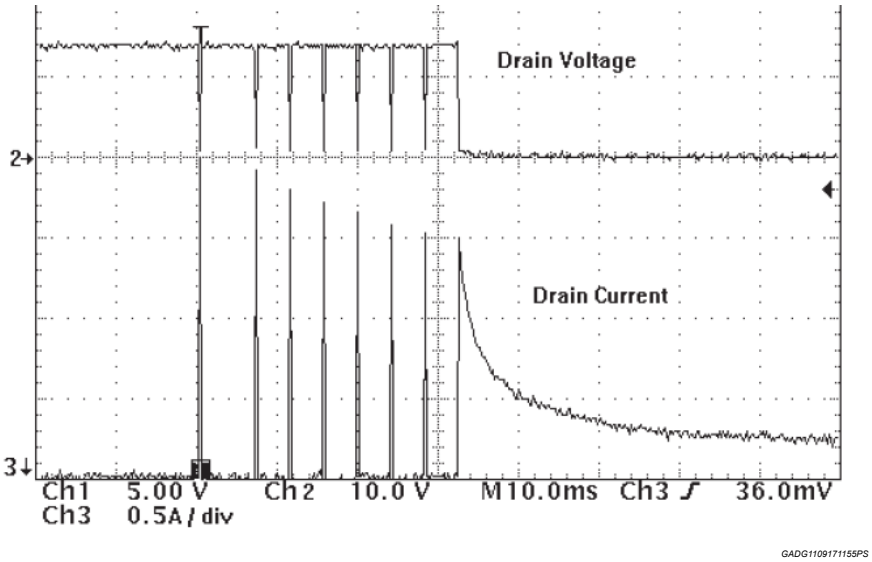


Figure 8. **Lamp control with LS switch**



3.1 Proposed configuration for normal operation

Figure 9. **Example 1: CV applications with independent PWM an all channels**

Battery supply voltage [V]	CV	28

Channel configuration									
CH	SIDE	FET TYPE	Qgs_typ [nC]	Fsw [kHz]	dc [%]	Cm [nF]	Rpd [kOhm]	TM%	Imean [mA]
1	HS	NMOS	70	0	80.00	1.5	47	20	0.942
2	LS	NMOS	70	22	80.00	1.5	47	20	3.192
3	LS	NMOS	70	22	80.00	1.5	47	20	3.192
4	HS	PMOS	70	0	80.00	1.5	47	20	0.000
5	LS	NMOS	70	0	80.00	1.5	47	20	0.942
6	HS	NMOS	70	0	80.00	1.5	47	20	0.942
7	LS	NMOS	70	0.1	95.00	1.5	47	20	0.935
8	LS	NMOS	70	0	80.00	1.5	47	20	0.942
Total charge pump workload									11.089

Color Scale For Total Workload
Charge pump capacity has been overcome
More than 80% of charge pump capacity is being used
Less than 80% of charge pump capacity is being used

Color Scale For Channel Workload
The channel uses more than 25% of the charge pump capacity
The channel uses more than 12.5% of the charge pump capacity
The channel uses less than 12.5% of the charge pump capacity

GADG1109171213PS

3.2 Load dump

In case of load dump, nothing would change in terms of charge pump stress because even if the battery supply voltage raises up to 60 V, the HS FETs are almost in a DC regime. On the other hand, stress induced by LS switches is not depending on V_{PS}.

3.3 Cold cranking

In case of cold cranking, charge pump capability is compromised and drops down to I_{CP_MAX} = 6 mA. Figure 10 shows that full functionality is not achievable, and a reconfiguration is needed to guarantee critical functions such as starter relay and the control one of the two injectors (see Figure 11).

Figure 10. Charge pump stress during cold cranking

Battery supply voltage [V]								MIN	3.8
Channel configuration									
CH	SIDE	FET TYPE	Qgs_typ [nC]	Fsw [kHz]	dc [%]	Cm [nF]	Rpd [kOhm]	TM%	Imean [mA]
1	HS	NMOS	70	0	80.00	1.5	47	20	0.942
2	LS	NMOS	70	22	80.00	1.5	47	20	3.192
3	LS	NMOS	70	22	80.00	1.5	47	20	3.192
4	HS	PMOS	70	0	80.00	1.5	47	20	0.000
5	LS	NMOS	70	0	80.00	1.5	47	20	0.942
6	HS	NMOS	70	0	80.00	1.5	47	20	0.942
7	LS	NMOS	70	0.1	95.00	1.5	47	20	0.935
8	LS	NMOS	70	0	80.00	1.5	47	20	0.942
Total charge pump workload									11.089

Color Scale For Total Workload
Charge pump capacity has been overcome
More than 80% of charge pump capacity is being used
Less than 80% of charge pump capacity is being used

Color Scale For Channel Workload
The channel uses more than 25% of the charge pump capacity
The channel uses more than 12.5% of the charge pump capacity
The channel uses less than 12.5% of the charge pump capacity

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Figure 11. **Limiting charge pump stress during cold cranking**

Battery supply voltage [V]	MIN	3.8

Channel configuration									
CH	SIDE	FET TYPE	Qgs_typ [nC]	Fsw [kHz]	dc [%]	Cm [nF]	Rpd [kOhm]	TM%	Imean [mA]
1	HS	NMOS	70	0	80.00	1.5	47	20	0.942
2	LS	NMOS	70	22	80.00	1.5	47	20	3.192
3	LS	NMOS	70	22	80.00	1.5	47	20	0.000
4	HS	PMOS	70	0	80.00	1.5	47	20	0.000
5	LS	NMOS	70	0	80.00	1.5	47	20	0.000
6	HS	NMOS	70	0	80.00	1.5	47	20	0.942
7	LS	NMOS	70	0.1	95.00	1.5	47	20	0.000
8	LS	NMOS	70	0	80.00	1.5	47	20	0.000
Total charge pump workload									5.077

Color Scale For Total Workload
Charge pump capacity has been overcome
More than 80% of charge pump capacity is being used
Less than 80% of charge pump capacity is being used

Color Scale For Channel Workload
The channel uses more than 25% of the charge pump capacity
The channel uses more than 12.5% of the charge pump capacity
The channel uses less than 12.5% of the charge pump capacity

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3.4 Case study: ST L9945 in application

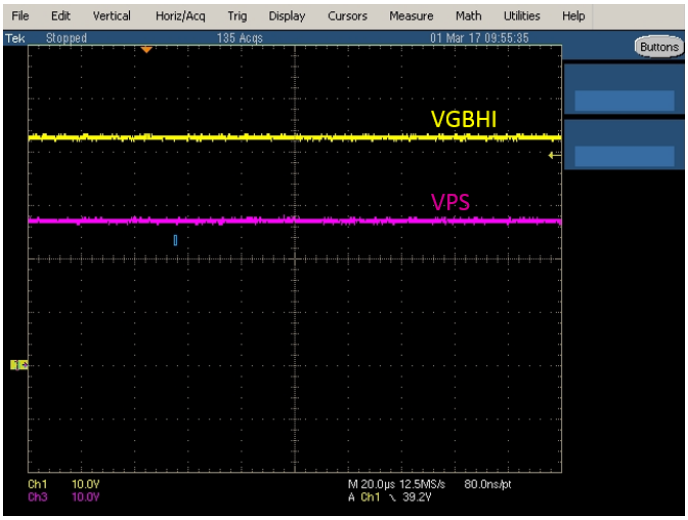
The following case study is based on ST L9945 flexible pre-driver, configured to drive all its 8 channels with independent PWM. Corner cases have been found for CV applications in various operating scenarios.

In the following examples, for all channels the following parameters are considered:

- NMOS: STD105N10F7AG
- V_{GS_TYP}: 12 V
- I_{BIAS_ON} = 530 µA
- I_{BIAS_OFF} = 480 µA

Figure 12 shows ST L9945 charge pump (VGBHI) while resting. All channels have been enabled but kept OFF. Hence, I_{BIAS_OFF} represents the only static leakage, causing almost no ripple on VGBHI pin.

Figure 12. Charge pump resting. All channels enabled but kept OFF



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3.4.1 Typical battery supply

These tests have been performed with VPS = 28 V at room temperature (≈ 25 °C). Starting from an initial switching profile, frequency has been gradually increased until the I_{CP_MAX} = 15 mA has been overcome. Refer to Figure 13.

Figure 13. Switching profiles for supply typical scenario

Battery supply voltage [V]	CV	28

Channel configuration

CH	SIDE	FET TYPE	Qgs_typ [nC]	Fsw [kHz]	dc [%]	Cm [nF]	Rpd [kOhm]	TM%	Imean [mA]
1	HS	NMOS	70	10	80.00	0.47	47	20	1.935
2	HS	NMOS	70	10	80.00	0.47	47	20	1.935
3	LS	NMOS	70	4	80.00	0.47	47	20	1.232
4	LS	NMOS	70	4	80.00	0.47	47	20	1.232
5	HS	PMOS	70	0	80.00	0.47	47	20	0.000
6	HS	PMOS	70	0	80.00	0.47	47	20	0.000
7	LS	NMOS	70	22	80.00	0.47	47	20	2.866
8	LS	NMOS	70	22	80.00	0.47	47	20	2.866
Total charge pump workload									12.066

Color Scale For Total Workload
Charge pump capacity has been overcome
More than 80% of charge pump capacity is being used
Less than 80% of charge pump capacity is being used

Initial profile

Battery supply voltage [V]	CV	28

Channel configuration

CH	SIDE	FET TYPE	Qgs_typ [nC]	Fsw [kHz]	dc [%]	Cm [nF]	Rpd [kOhm]	TM%	Imean [mA]
1	HS	NMOS	70	15	80.00	0.47	47	20	2.468
2	HS	NMOS	70	15	80.00	0.47	47	20	2.468
3	LS	NMOS	70	15	80.00	0.47	47	20	2.231
4	LS	NMOS	70	15	80.00	0.47	47	20	2.231
5	HS	PMOS	70	0	80.00	0.47	47	20	0.000
6	HS	PMOS	70	0	80.00	0.47	47	20	0.000
7	LS	NMOS	70	22	80.00	0.47	47	20	2.866
8	LS	NMOS	70	22	80.00	0.47	47	20	2.866
Total charge pump workload									15.128

Color Scale For Total Workload
Charge pump capacity has been overcome
More than 80% of charge pump capacity is being used
Less than 80% of charge pump capacity is being used

Critical profile

GADG1109171310PS

Figure 14 shows the device performance when the initial switching profile is applied. Note how ripple on VGBHI pin has increased, with higher negative peaks corresponding to the simultaneous switching of more than one channel. The external FET gate signal has been monitored on every channel, showing that each output is regularly switching with a stable ON voltage.

Figure 14. Initial profile

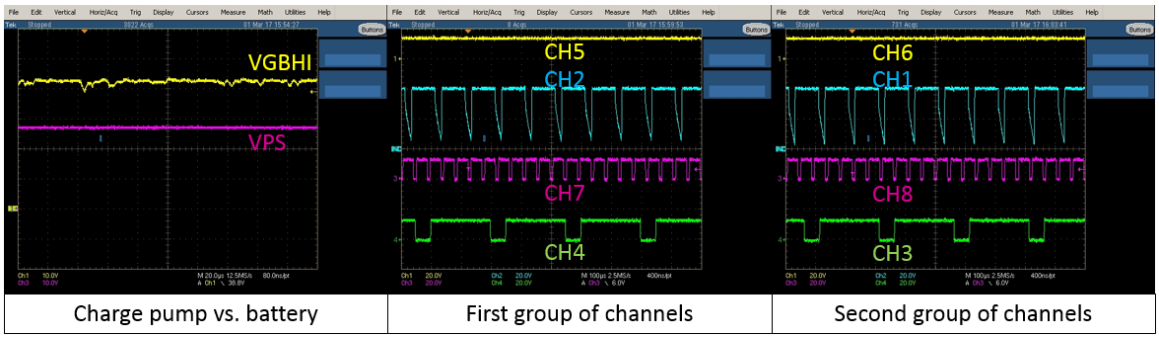

image16.png

Figure 15 shows the device performance when the critical switching profile is applied. Note how ripple on VGBHI pin has increased, but still VGBHI is stably above VPS. The external FET gate signal has been monitored on every channel, showing that each output is regularly switching with a stable ON voltage.

Figure 15. Critical profile

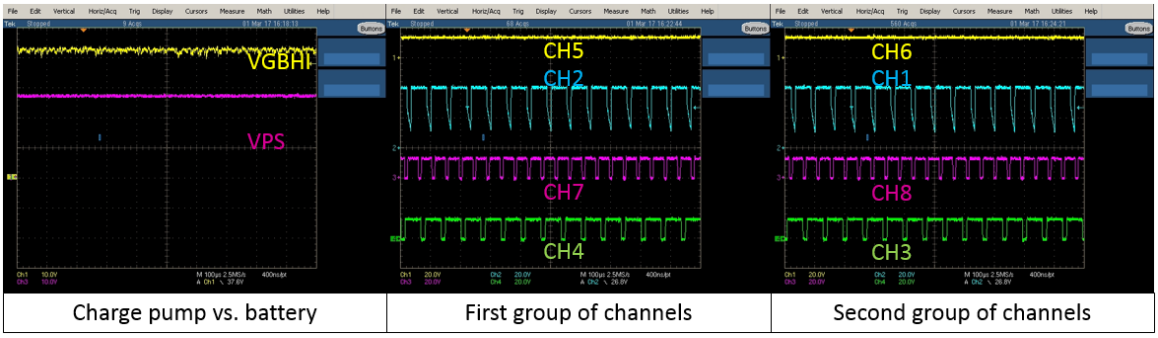

image17.png

The 20% tolerance margin guarantees that the critical switching profile can be sustained without any issue.

Note: L9945 was able to sustain 6 NMOS channels switching at 25 kHz at room temperature without causing any charge pump undervoltage. However, such condition is too stressing and is not guaranteed over the whole temperature range, since performances may degrade too much and the 20% tolerance margin might be insufficient.

Junction temperature has been monitored while switching at critical profile. After an initial transient, T_j was stable at 73 °C, meaning that a self-heating ΔT = 48 °C occurs while performing in this condition. Since L9945 has an operating range equal to [-40;+150] °C, the critical profile can be sustained without issues if ambient temperature T_a is below 102 °C. Hence, operation is more limited by self-heating rather than charge pump capability.

Note: Consider that in real applications loads are not active 100% of the time. Many of them, such as injectors, have a windowed operation. Hence, self-heating should be less than the estimated ΔT, that was measured with all channels continuously switching. The actual self-heating is strongly dependent on the application type and package thermal impedance. Results shown here can be considered as a reliable worst case estimation for ΔT.

A current peak stress test has also been performed, with 6 NMOS channels switching simultaneously at 8 kHz frequency. Results are plotted in Figure 16. Note how peaks on VGBHI are much higher in respect of the previous situations, where the phase relation between control signals was random. When 6 signals are in phase, the negative peak can be as high as 7 V. The recovery time after such peak has been measured and it's around 20 µs, meaning that simultaneous switching could be sustained even at 50 kHz at room temperature. Obviously, such estimation doesn't take into account the temperature variations and the process spread. To be conservative, a 50% tolerance margin can be considered so simultaneous switching on 6 NMOS channels can be sustained without issues at a 25 kHz rate, given the configuration reported in the present case study.

Figure 16. Current peaks analysis: charge pump vs battery

Burst of 12 current peaks at 8 kHz | Charge pump recovery time

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3.4.2 Max operating voltage

These tests have been performed with VPS = 36 V at room temperature (≈ 25 °C). Starting from an initial switching profile, frequency has been gradually increased until the I_{CP_MAX} = 15 mA has been overcome. Refer to Figure 17.

Figure 17. Switching profiles for supply typical scenario

Battery supply voltage [V]								MAX_OP	36.0
Channel configuration									
CH	SIDE	FET TYPE	Qgs_typ [nC]	Fsw [kHz]	dc [%]	Cm [nF]	Rpd [kOhm]	TM%	Imean [mA]
1	HS	NMOS	70	10	80.00	0.47	47	20	1.980
2	HS	NMOS	70	10	80.00	0.47	47	20	1.980
3	LS	NMOS	70	4	80.00	0.47	47	20	1.232
4	LS	NMOS	70	4	80.00	0.47	47	20	1.232
5	HS	PMOS	70	0	80.00	0.47	47	20	0.000
6	HS	PMOS	70	0	80.00	0.47	47	20	0.000
7	LS	NMOS	70	22	80.00	0.47	47	20	2.866
8	LS	NMOS	70	22	80.00	0.47	47	20	2.866
Total charge pump workload									12.156

Color Scale For Total Workload
Charge pump capacity has been overcome
More than 80% of charge pump capacity is being used
Less than 80% of charge pump capacity is being used

Initial profile

Battery supply voltage [V]								MAX_OP	36.0
Channel configuration									
CH	SIDE	FET TYPE	Qgs_typ [nC]	Fsw [kHz]	dc [%]	Cm [nF]	Rpd [kOhm]	TM%	Imean [mA]
1	HS	NMOS	70	15	80.00	0.47	47	20	2.535
2	HS	NMOS	70	15	80.00	0.47	47	20	2.535
3	LS	NMOS	70	15	80.00	0.47	47	20	2.231
4	LS	NMOS	70	15	80.00	0.47	47	20	2.231
5	HS	PMOS	70	0	80.00	0.47	47	20	0.000
6	HS	PMOS	70	0	80.00	0.47	47	20	0.000
7	LS	NMOS	70	22	80.00	0.47	47	20	2.866
8	LS	NMOS	70	22	80.00	0.47	47	20	2.866
Total charge pump workload									15.264

Color Scale For Total Workload
Charge pump capacity has been overcome
More than 80% of charge pump capacity is being used
Less than 80% of charge pump capacity is being used

Critical profile

GADG1109171514PS

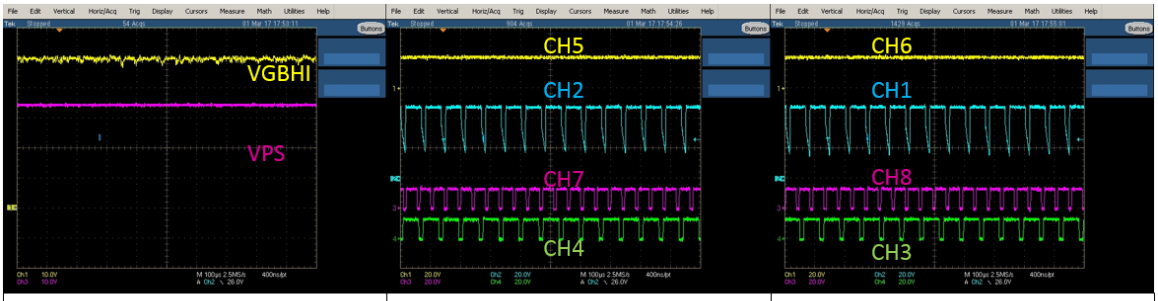
Figure 18 shows the device performance when the initial switching profile is applied. Note how ripple on VGBHI pin has increased, with higher negative peaks corresponding to the simultaneous switching of more than one channel. The external FET gate signal has been monitored on every channel, showing that each output is regularly switching with a stable ON voltage.

Figure 18. Initial switching profile

GADG1109171523PS

Figure 19 shows the device performance when the critical switching profile is applied. Note how ripple on VGBHI pin has increased, but still VGBHI is stably above VPS. The external FET gate signal has been monitored on every channel, showing that each output is regularly switching with a stable ON voltage.

Figure 19. Critical switching profile



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The 20% tolerance margin guarantees that the critical switching profile can be sustained without any issue.

Note: L9945 was able to sustain 6 NMOS channels switching at 25 kHz at room temperature without causing any charge pump overvoltage. However, such condition is too stressing and is not guaranteed over the whole temperature range, since performances may degrade too much and the 20% tolerance margin might be insufficient.

Junction temperature has been monitored in while executing critical profile. After an initial transient, T_j was stable at 90 °C, meaning that a self-heating ΔT = 65 °C occurs while performing in this condition. Since L9945 has an operating range equal to [-40;+150] °C, the critical profile can be sustained without issues if ambient temperature T_a is below 85 °C. Hence, operation is more limited by self-heating rather than charge pump capability.

Note: Consider that in real applications loads are not active 100% of the time. Many of them, such as injectors, have a windowed operation. Hence, self-heating should be less than the estimated ΔT, that was measured with all channels continuously switching. The actual self-heating is strongly dependent on the application type and package thermal impedance. Results shown here can be considered as a reliable worst case estimation for ΔT.

A current peak stress test has also been performed, with 6 NMOS channels switching simultaneously at 8 kHz frequency. Results are plotted in Figure 20. Note how peaks on VGBHI are much higher in respect of the previous situations, where the phase relation between control signals was random. When 6 signals are in phase, the negative peak can be as high as 7 V. The recovery time after such peak has been measured: it's around 20 µs, meaning that simultaneous switching could be sustained even at 50 kHz at room temperature. Obviously, such estimation doesn't take in account the temperature variations and the process spread. To be conservative, a 50% tolerance margin can be considered: simultaneous switching on 6 NMOS channels can be sustained without issues at a 25 kHz rate, given the configuration reported in the present case study.

Figure 20. Current peaks analysis: charge pump vs battery

Burst of 12 current peaks at 8 kHz	Charge pump recovery time

GADG1109171539PS

Revision history

Table 5. **Document revision history**

Date	Version	Changes
20-Mar-2019	1	Initial release.

Contents

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