Getting started with STM32L5 Series hardware development

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features such as power supply, clock management, reset control, boot mode settings and debug management.

It shows how to use the STM32L5 Series MCUs and describes the minimum hardware resources required to develop an application using the STM32L5 Series devices.

Detailed reference design schematics are also contained in this document with descriptions of the main components, interfaces and modes.

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1 General information

The STM32L5 Series are Arm®-based devices.

Note: *Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.*

2 Power supplies management

2.1 Power supplies

The STM32L5 Series devices require a 1.71 V to 3.6 V operating voltage supply (V_{DD}). Several independent supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{DDDSI}), can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V

  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through V_{DD} pins.

- V_{DD12} = 1.05 V to 1.32 V

  V_{DD12} is the external power supply bypassing the internal regulator when connected to an external SMPS. It is provided externally through VDD12 pins and only available on packages with the external SMPS supply option. It does not need any external capacitance and cannot drive an external load.

- V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 V (DACs/OPAMPs) / 2.4 V (VREFBUF) to 3.6 V

  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage.

- V_{DDUSB} = 3.0 V to 3.6 V (USB used)

  V_{DDUSB} is the external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.

- V_{DDIO2} = 1.08 V to 3.6 V

  V_{DDIO2} is the external power supply for 14 I/Os (Port G[15:2]). The V_{DDIO2} voltage level is independent from the V_{DD} voltage.

Note: *When the functions supplied by V_{DDA}, V_{DDIO2} or V_{DDUSB} are not used, these supplies should preferably be shorted to V_{DD}.*

Note: *On small packages, V_{DDA}, V_{DDIO2} or V_{DDUSB} independent power supplies may not be present as a dedicated pin and are internally bonded to V_{DD}.*

- V_{BAT} = 1.55 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

- V_{REF-}, V_{REF+}

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  When V_{DDA} < 2 V, V_{REF+} must be equal to V_{DDA}. When $V_{DDA} \geq$ 2 V, V_{REF+} must be between 2 V and V_{DDA}.

  V_{REF+} can be grounded when ADC and DAC are not active.

  The internal voltage reference buffer supports two output voltages, which are configured with VRS bit in the VREF_CSR register:

  > V_{REF+} around 2.048 V. This requires V_{DDA} equal to or higher than 2.4 V.

  > V_{REF+} around 2.5 V. This requires V_{DDA} equal to or higher than 2.8 V.

V_{REF-} and V_{REF+} pins are not available on all packages. When not available, they are bonded to V_{SSA} and V_{DDA}, respectively.

When the V_{REF+} is double-bonded with V_{DDA} in a package, the internal voltage reference buffer is not available and must be kept disable (refer to datasheet for packages pinout description).

V_{REF-} must always be equal to V_{SSA}.

- V_{DDSMPS} = 2 V to 3.6 V VDDSMPS is the external power supply for the SMPS step-down converter. It is provided externally through the VDDSMPS supply pin, and must be connected to the same supply as V_{DD}.

- • VLXSMPS is the switched SMPS step-down converter output.
- • V15SMPS are the power supply for the system regulator. It is provided externally through the SMPS step-down converter VLXSMPS output.

Note: *The SMPS power supply pins are available only on a specific package with SMPS step-down converter option.*

- • VDD12 = 1.05 to 1.32 V VDD12 is the external power supply bypassing the internal regulator when connected to an external SMPS. It is provided externally through VDD12 pins and only available on packages with the external SMPS supply option. VDD12 does not require any external decoupling capacitance and cannot support any external load.

Note: *The VDD12 power supply pins are available only on a specific package with external SMPS option.*

Note:

Independent power supplies are not present when the related features are not supported on the product, they are not present neither on small packages where they are bonded together with other supply pin.

An embedded linear voltage regulator is used to supply the internal digital power V_{CORE}. V_{CORE} is the power supply for digital peripherals and SRAMs. The Flash is supplied by V_{CORE} and V_{DD}.

The following figures present an overview of the STM32L5 Series power supply depending on the device.

Figure 1. **STM32L552xx and STM32L562xx power supply overview**
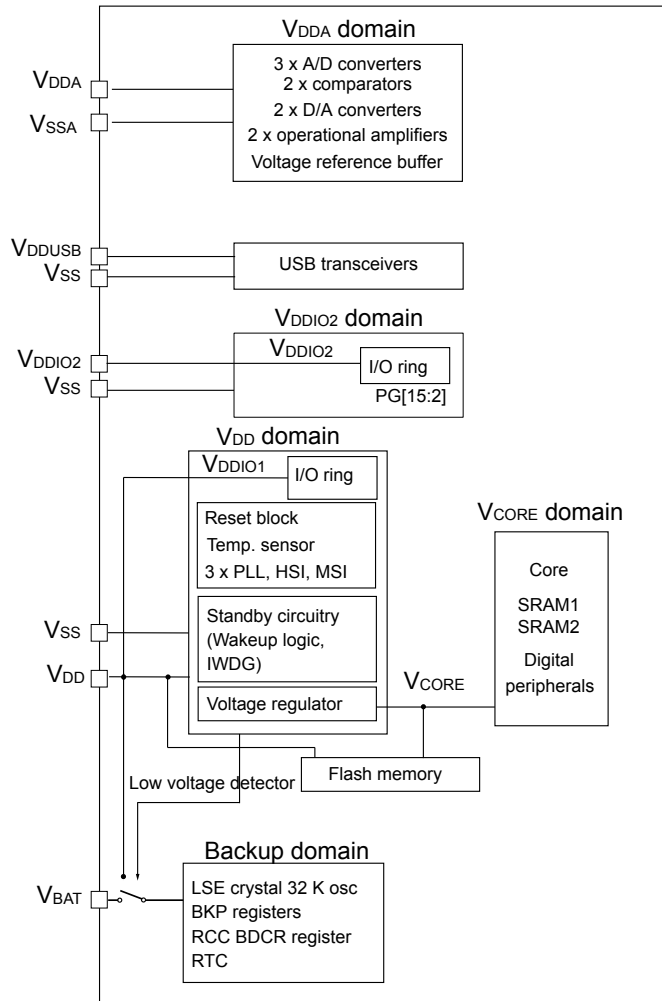
In the STM32L552xxxxP and STM32L562xxxxP devices, the I/Os and system analog peripherals (such as PLLs, and reset block) are fed by V_{DD} supply source. The V_{CORE}, power supply for digital peripherals and memories is generated from external SMPS.

Figure 2. STM32L552xxxxP and STM32L562xxxxP power supply overview
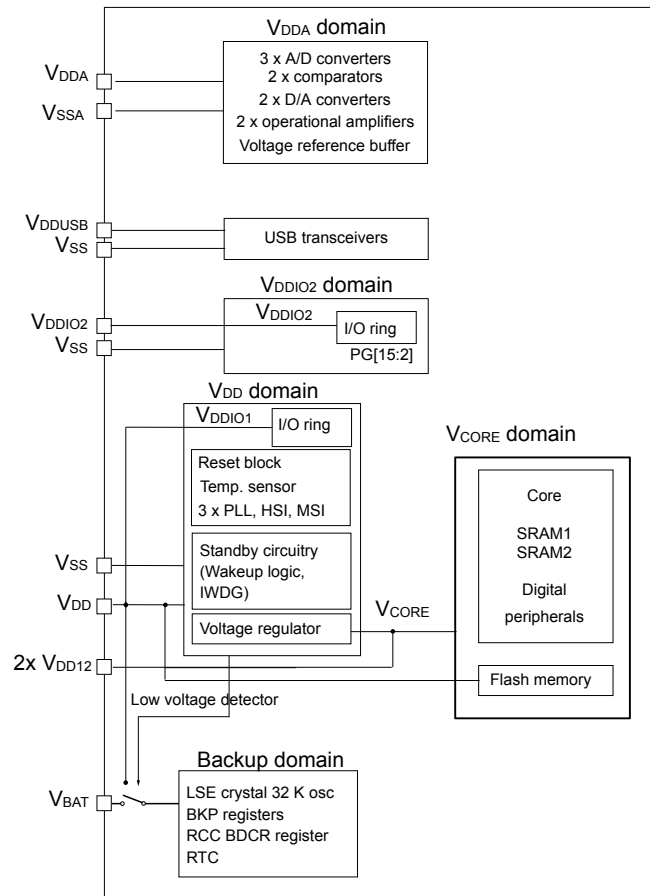
Note: *If the selected package has the external SMPS option but no external SMPS is used by the application (the embedded LDO is used instead), the VDD12 pins are kept unconnected.*

In the STM32L552xxxxQ and STM32L562xxxxQ devices, the I/Os, the embedded SMPS step-down converter and the system analog peripherals (such as PLLs and reset block) are fed by V_{DD} supply source. The embedded linear voltage regulator that provides the V_{CORE} supply for digital peripherals and memories is fed by the SMSP step-down converter output.

Figure 3. STM32L552xxxxQ and STM32L562xxxxQ power supply overview
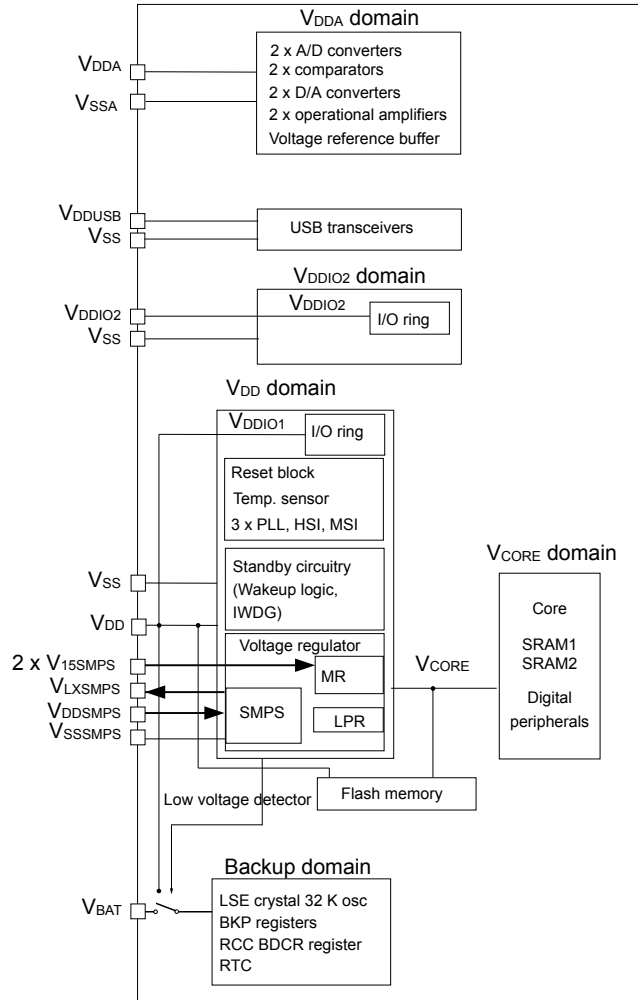
Note: If the selected package has the SMPS step-down converter option but the SMPS is not used by the application (and the embedded LDO is used instead), it is recommended to set the SMPS power supply pins as follows:

- V_{DDSMPS} and V_{LXSMPS} connected to V_{SS}
- V_{15SMPS} connected to V_{DD}.

2.1.1 Independent analog peripherals supply

To improve ADC and DAC conversion accuracy and to extend the supply flexibility, the analog peripherals have an independent power supply which can be separately filtered and shielded from noise on the PCB.

- The analog peripherals voltage supply input is available on a separate V_{DDA} pin.
- An isolated supply ground connection is provided on V_{SSA} pin.

The V_{DDA} supply voltage can be different from V_{DD}. The presence of V_{DDA} must be checked before enabling any of the analog peripherals supplied by V_{DDA} (A/D converter, D/C converter, comparators, operational amplifiers, voltage reference buffer).

The V_{DDA} supply can be monitored by the peripheral voltage monitoring, and compared with two thresholds (1.65 V for PVM3 or 1.8 V for PVM4), refer to reference manual section: Peripheral voltage monitoring (PVM) for more details.

When a single supply is used, V_{DDA} can be externally connected to V_{DD} through the external filtering circuit in order to ensure a noise-free V_{DDA} reference voltage.

ADC and DAC reference voltage

To ensure a better accuracy on low-voltage inputs and outputs, the user can connect to V_{REF+} a separate reference voltage lower than V_{DDA}. V_{REF+} is the highest voltage, represented by the full scale value, for an analog input (ADC) or output (DAC) signal.

V_{REF+} can be provided either by an external reference or by an internal buffered voltage reference (V_{REFBUF}).

The internal voltage reference is enabled by setting the ENVR bit in the V_{REFBUF} control and status register (VREF_CSR). The voltage reference is set to 2.5 V when the VRS bit is set and to 2.048 V when the VRS bit is cleared. The internal voltage reference can also provide the voltage to external components through V_{REF+} pin. Refer to the device datasheet or reference manual for further information.

2.1.2 Independent I/O supply rail

Some I/Os from Port G (PG[15:2]) are supplied from a separate supply rail. The power supply for this rail can range from 1.08 V to 3.6 V and is provided externally through the V_{DDIO2} pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}. The V_{DDIO2} pin is available only for some packages. Refer to the pinout diagrams or tables in the related device datasheet(s) for I/O list(s).

After reset, the I/Os supplied by V_{DDIO2} are logically and electrically isolated and therefore are not available. The isolation must be removed before using any I/O from PG[15:2], by setting the IOSV bit in the PWR_CR2 register, once the $V_{DDIO2\ supply\ is\ present}$.

The V_{DDIO2} supply is monitored by the peripheral voltage monitoring (PVM2) and compared with the internal reference voltage (3/4 V_{REFINT}, around 0.9 V), refer to reference manual section: Peripheral voltage monitoring (PVM) for more details.

2.1.3 Independent USB transceivers supply

The USB transceivers are supplied from a separate V_{DDUSB} power supply pin. V_{DDUSB} range is from 3.0 V to 3.6 V and its voltage level is completely independent from V_{DD} or V_{DDA}.

After reset, the USB features supplied by V_{DDUSB} are logically and electrically isolated and therefore are not available. The isolation must be removed before using the USB OTG peripheral, by setting the USV bit in the PWR_CR2 register, once the $V_{DDUSB\ supply\ is}$ present.

The V_{DDUSB} supply is monitored by the peripheral voltage monitoring (PVM1) and compared with the internal reference voltage (V_{REFINT}, around 1.2 V), refer to reference manual section: Peripheral voltage monitoring (PVM) for more details.

2.1.4 Battery Backup domain

To retain the content of the backup registers and supply the RTC function when V_{DD} is turned off, the V_{BAT} pin can be connected to an optional backup voltage supplied by a battery or by another source.

The V_{BAT} pin powers the RTC unit, the LSE oscillator and the PC13 to PC15 I/Os, allowing the RTC to operate even when the main power supply is turned off. The switch to the V_{BAT} supply is controlled by the power-down reset embedded in the Reset block.

Caution: During $t_{RSTTEMPO}$ (temporization at V_{DD} startup) or after a PDR has been detected, the power switch between V_{BAT} and V_{DD} remains connected to V_{BAT}.

Caution: During the startup phase, if V_{DD} is established in less than $t_{RSTTEMPO}$ (refer to the datasheet for the value of $t_{RSTTEMPO}$) and $V_{DD} > V_{BAT} + 0.6$ V, a current may be injected into V_{BAT} through an internal diode connected between V_{DD} and the power switch (V_{BAT}).

Caution: If the power supply/battery connected to the V_{BAT} pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the V_{BAT} pin.

If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD} with a 100 nF external ceramic decoupling capacitor.

When the Backup domain is supplied by V_{DD} (analog switch connected to V_{DD}), the PC13, PC14 and PC15 pins, belonging to V_{BAT} domain, can have these functions:

• GPIO pins
• RTC or LSE pins (refer to reference manual section: RTC functional description)

Note: *Due to the fact that the analog switch can transfer only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is restricted: the frequency has to be limited to 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (for instance to drive a LED).*

When the Backup domain is supplied by V_{BAT} (analog switch connected to V_{BAT} because V_{DD} is not present), the following functions are available:

• PC13, PC14 and PC15 can be controlled only by RTC or LSE refer to reference manual section: RTC functional description
• PA0, PE6 and PC13 can be used as tamper inputs/outputs (TAMP_IN1, TAMP_IN2, TAMP_IN3, TAMP_OUT2).

Backup domain access

After a system reset, the Backup domain (RTC registers and backup registers) is protected against possible unwanted write accesses. To enable access to the Backup domain, proceed as follows:

1. Enable the power interface clock by setting the PWREN bits in the APB1 peripheral clock enable register 1 (RCC_APB1ENR1).
2. Set the DBP bit in the Power control register 1 (PWR_CR1) to enable access to the Backup domain.
3. Select the RTC clock source in the Backup domain control register (RCC_BDCR).
4. Enable the RTC clock by setting the RTCEN [15] bit in the Backup domain control register (RCC_BDCR).

VBAT battery charging

When V_{DD} is present, It is possible to charge the external battery on V_{BAT} through an internal resistance.

The V_{BAT} charging is done either through a 5 kΩ resistor or through a 1.5 kΩ resistor depending on the V_{BRS} bit value in the PWR_CR4 register. The battery charging is enabled by setting V_{BE} bit in the PWR_CR4 register. It is automatically disabled in V_{BAT} mode.

2.1.5 Voltage regulator

Two embedded linear voltage regulators supply all the digital circuitries, except for the Standby circuitry and the Backup domain. The main regulator output voltage (V_{CORE}) can be programmed by software to three different power ranges (range 0, 1 and 2) in order to optimize the consumption depending on the system's maximum operating frequency (refer to reference manual Section: Clock source frequency versus voltage scaling and to Section: Read access latency.

The voltage regulators are always enabled after a reset. Depending on the application modes, the V_{CORE} supply is provided either by the main regulator (MR) or by the low-power regulator (LPR).

• In Run, Sleep and Stop 0 modes, both regulators are enabled and the main regulator (MR) supplies full power to the V_{CORE} domain (core, memories and digital peripherals).
• In Low-power run and Low-power sleep modes, the main regulator is off and the low-power regulator (LPR) supplies low power to the V_{CORE} domain, preserving the contents of the registers and of internal SRAM.
• In Stop 1 and Stop 2 modes, the main regulator is off and the low-power regulator (LPR) supplies low power to the V_{CORE} domain, preserving the contents of the registers and internal SRAMs.
• In Standby mode with SRAM2 content preserved (RRS bit is set in the PWR_CR3 register), the main regulator (MR) is off and the low-power regulator (LPR) provides the supply to SRAM2 only. The core and digital peripherals (except Standby circuitry and Backup domain) and SRAM1 are powered off.
• In Standby mode, both regulators are powered off. The contents of the registers and SRAMs is lost except for the Standby circuitry and the Backup domain.
• In Shutdown mode, both regulators are powered off. When exiting from Shutdown mode, a power-on reset is generated. Consequently, the contents of the registers and of SRAMx is lost, except for the Backup domain.

The packages with external SMPS supply option (STM32L5x2xxxxP) can force an external V_{DD12} supply on the V_{CORE} power domain when the MR is in use.

• When V_{DD12} is forced by an external source and is higher than the output of the internal LDO, the current is taken from this external supply and the overall power efficiency is significantly improved if using an external step-down DC/DC converter.

In the packages with SMPS step-down converter (STM32L552xxxxQ), the embedded linear voltage regulator that provides the VCORE supply is fed by the SMSP step-down converter output.

The following table summarizes the SMPS behavior depending on the main regulator range, V_{DD} and consumption.

Table 1. SMPS mode summary

Ranges	Max AHB clock	V_{CORE}	SMPS mode	
			$V_{DD} \leq 2.05$ V	$V_{DD} > 2.05$ V
Range 0	110 MHz	1.28 V	Automatic Bypass mode	HP mode Max current consumption = 120 mA
Range 1	80 MHz	1.2 V	Automatic Bypass mode	HP mode Max current consumption = 80 mA
Range 2	26 MHz	1.0 V	Software Bypass mode (1)	LP mode or HP mode Max current consumption = 30 mA

1. *The user application must use PVD0 to monitor the V_{DD} supply and request the SMPS Bypass mode.*

2.1.6 Dynamic voltage scaling management

• Main regulator Range 0: high performance. It provides a typical output voltage at 1.28 V. It is used when the system clock frequency is up to 110 MHz. The Flash access time for read access is minimum, write and erase operations are possible.

• Main regulator Range 1: medium performance. It provides a typical output voltage at 1.2 V. It is used when the system clock frequency is up to 80 MHz. The Flash access time for read access is minimum, write and erase operations are possible.

• Main regulator Range 2: low-power range. It provides a typical output voltage at 1.0 V. The system clock frequency can be up to 26 MHz.The Flash access time for a read access is increased as compared to Range 1; write and erase operations are not possible.

2.2 Power supply schemes

The circuit is powered by a stabilized power supply, V_{DD}.

- The V_{DD} pins must be connected to V_{DD} with external decoupling capacitors; one single Tantalum or ceramic capacitor (minimum 4.7 µF typical 10 µF) for the package + one 100 nF ceramic capacitor for each V_{DD} pin).

- The V_{DD12} pins, when available, can be connected to an external SMPS. As these V_{DD12} pins are also connected to internal regulators, they cannot accommodate a decoupling capacitance, neither can they be shared with an external circuitry for other purposes.

- The V_{DDA} pin must be connected to two external decoupling capacitors (10 nF ceramic capacitor + 1 µF Tantalum or ceramic capacitor).

  Additional precautions can be taken to filter digital noise: V_{DDA} can be connected to V_{DD} through a ferrite bead.

- The V_{REF+} pin can be provided by an external voltage reference in which case a 100 nF external capacitor and a 1 µF capacitor must be connected on this pin.

  It can also be provided internally by the Voltage Reference Buffer in which case an external capacitor of 1 µF (typical) must be connected on this pin.

- The V_{BAT} pin can be connected to an external battery to preserve Backup domain content.

  When V_{DD} is present, it is possible to charge the external battery on V_{BAT} through a 5 kΩ or 1.5 kΩ internal resistor.

  If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD} with a 100 nF external ceramic decoupling capacitor.

- The SMPS step-down converter requires an external coil with typical value of 4.7 µH to be connected between the dedicated VLXSMPS pin to VSSSMPS via a capacitor of 4.7µF.

Figure 4. STM32L552xx power supply scheme
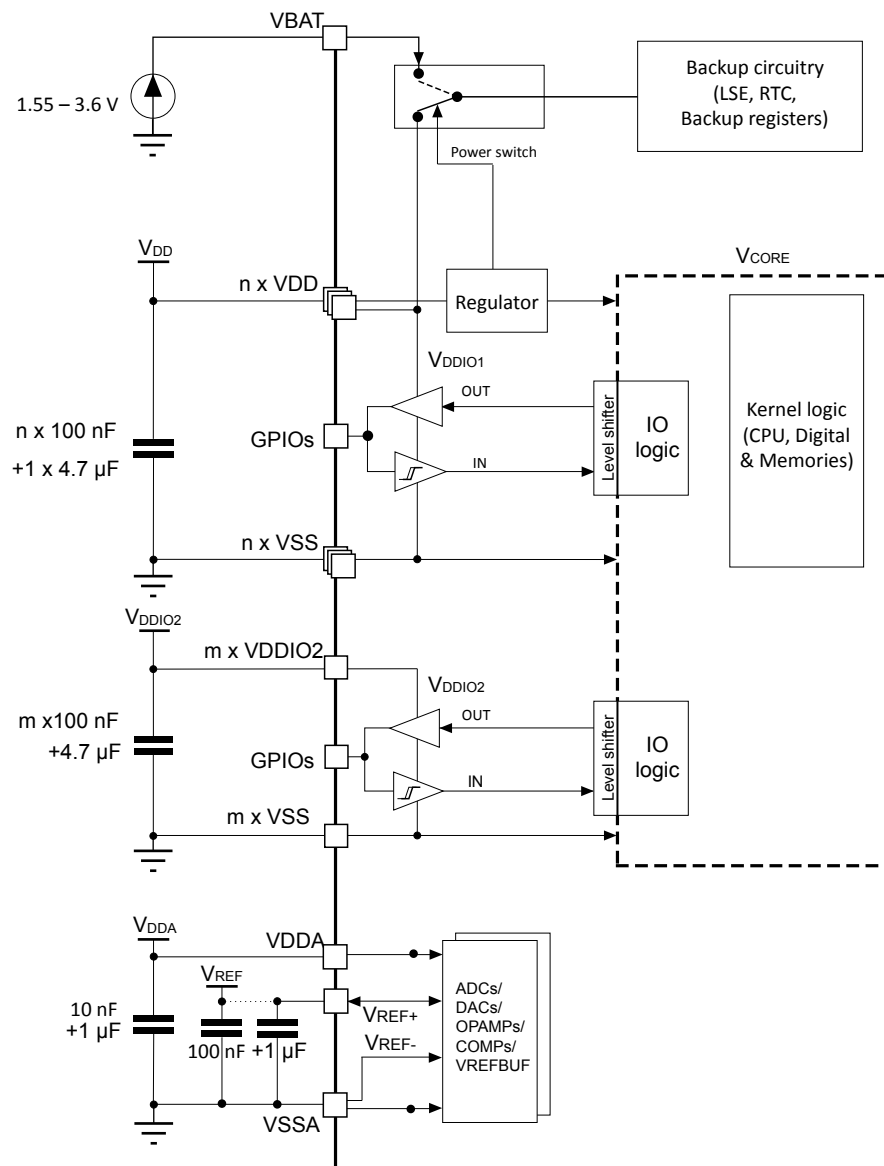
Figure 5. STM32L552xxxxP power supply overview
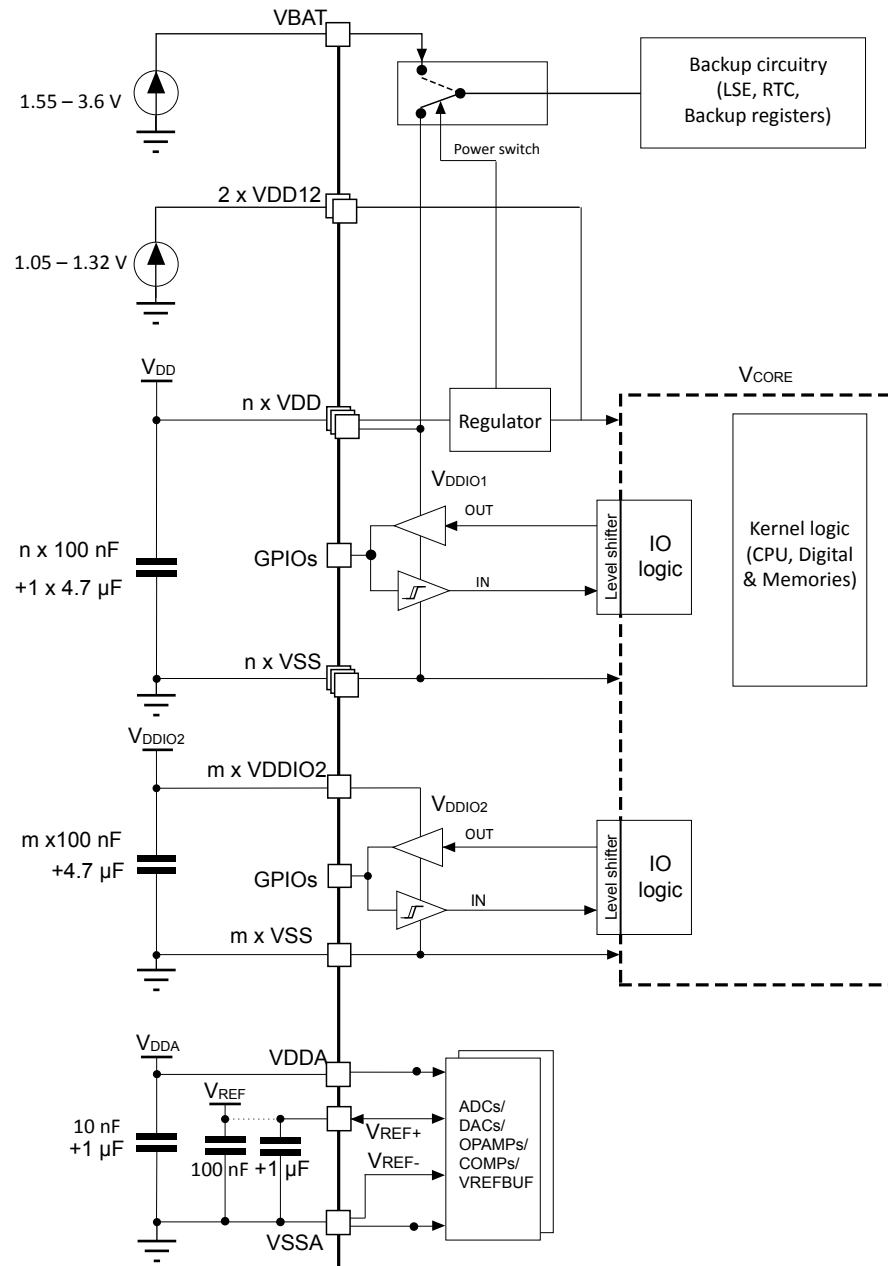
Figure 6. STM32L552xxxxQ power supply overview
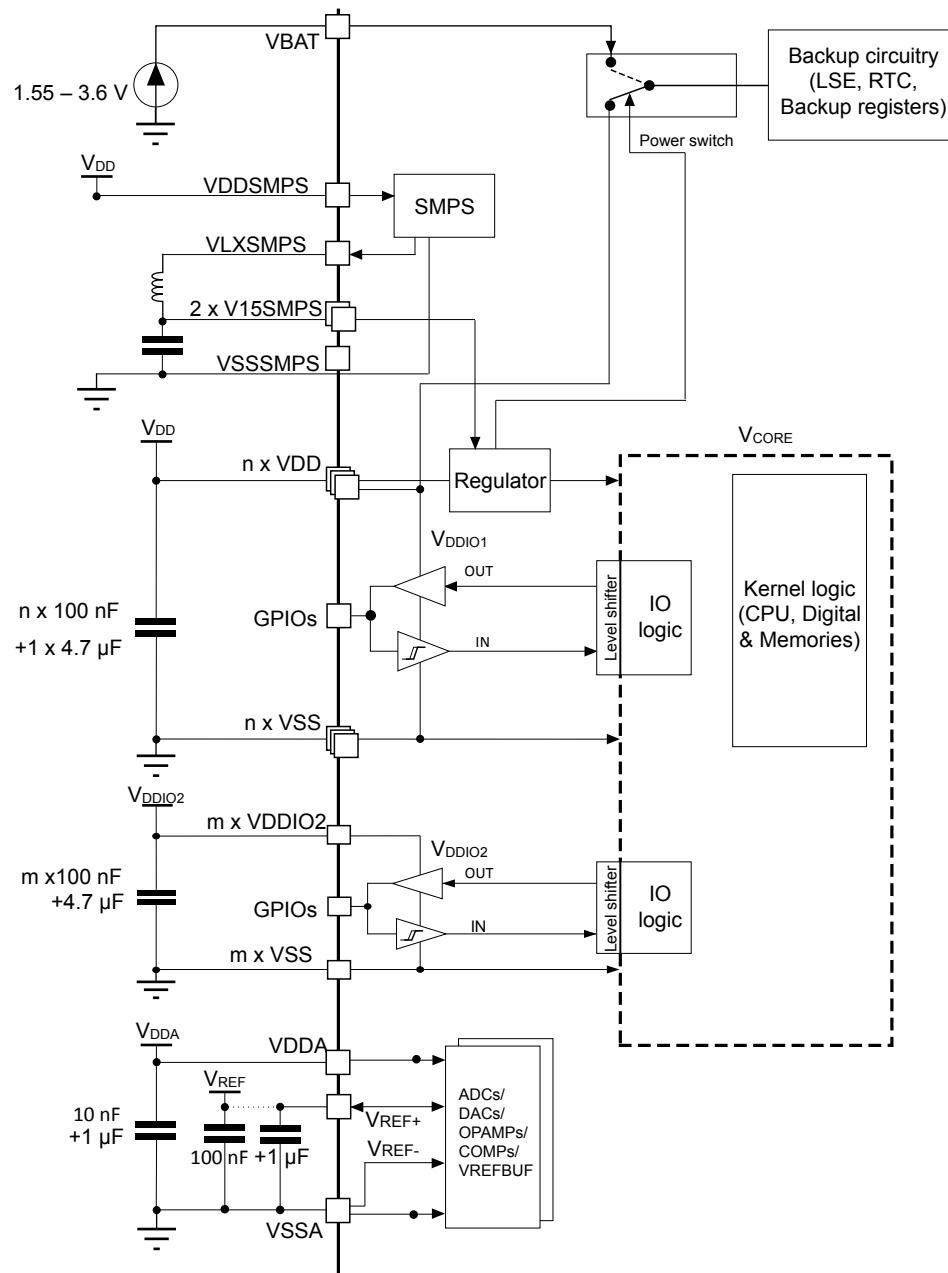
2.3 Power supply sequence between V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{DDSMPS} and V_{DD}

2.3.1 Power supplies isolation

The STM32L5 Series features a powerful reset system which ensures that the main power supply (V_{DD}) has reached a valid operating range before releasing the MCU reset. This reset system is also in charge of isolating the independent power domains: V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{DDSMPS} and V_{DD}. This reset system is supplied by V_{DD} and is not functional before V_{DD} reaches a minimal voltage (1 V in worse case conditions).

In order to avoid leakage currents between the available supplies and V_{DD} (or ground), V_{DD} must be provided first to the MCU and released last.

2.3.2 General requirements

During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{DDSMPS}) must remain below V_{DD} +300 mV.

- When V_{DD} is above 1 V, all power supplies are independent.

Figure 7. Power-up/down sequence
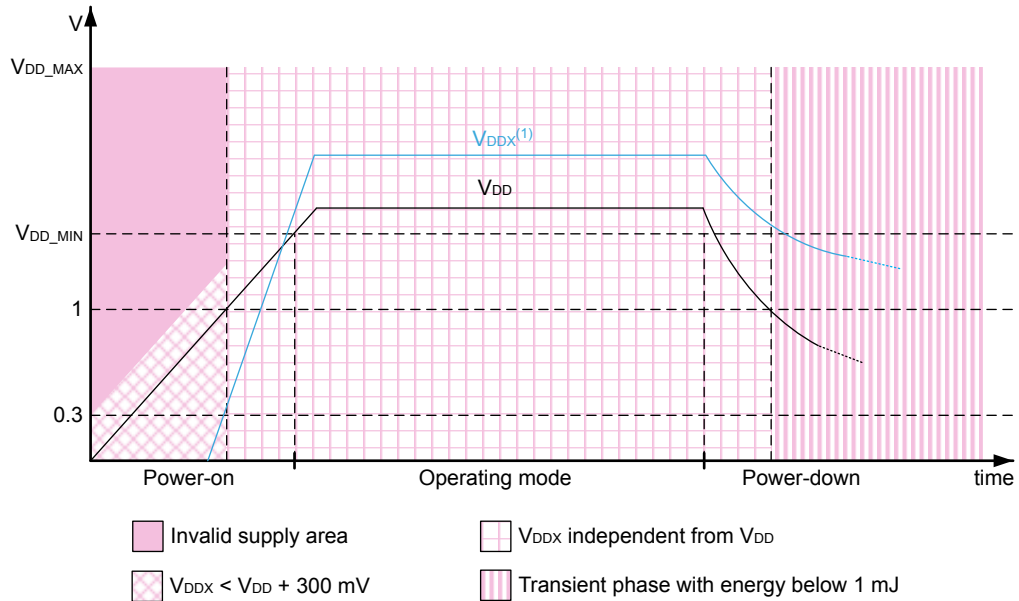
1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDIO2} and V_{DDUSB}.

Note: *V_{BAT} is an independent supply and has no constraint versus V_{DD}.*

All power supply rails can be tied together.

2.3.3 Particular conditions during power-down phase

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 8. Power-down phase
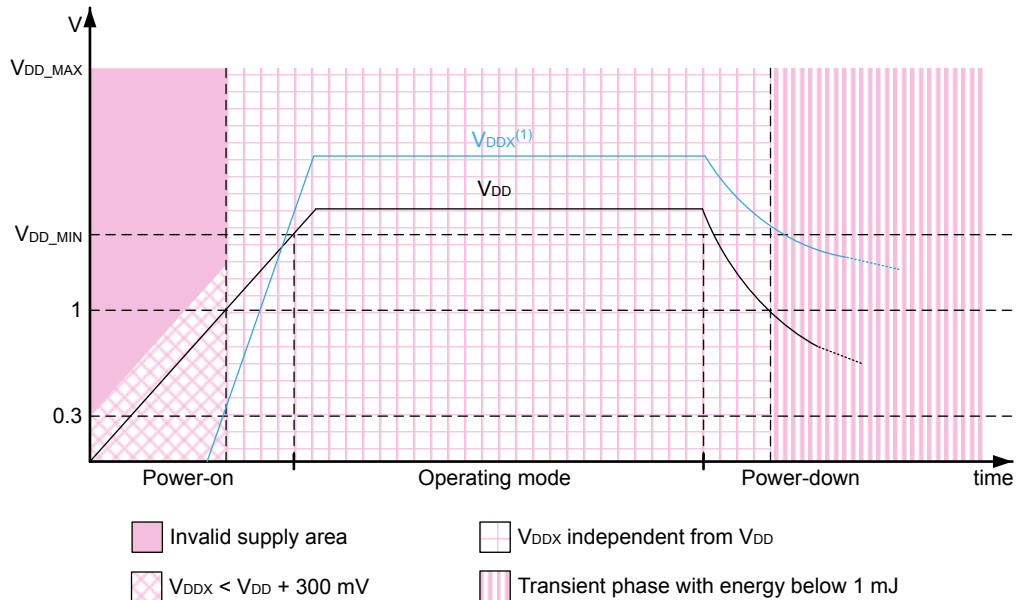
1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{DDSMPS}.

V_{DDX} (V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{DDSMPS}) power rails must be switched off before V_{DD}. Note that during the power-down transient phase, V_{DDX} can remain temporarily above V_{DD}.

Example of computation of the energy provided to the MCU during the power-down phase:

If the sum of decoupling capacitors on V_{DDX} is 10 µF and V_{DD} drops below 1 V while V_{DDX} is still at 3.3 V, the energy remaining in the decoupling capacitors is:

$E = \frac{1}{2} C V^2 = \frac{1}{2} \times 10^{-5} \times 3.3^2 = 0.05$ mJ

The energy remaining in the decoupling capacitors is below 1 mJ so it is acceptable for the MCU to absorb it.

2.4 Reset and power supply supervisor

2.4.1 Power-on reset (POR) / power-down reset (PDR) / Brownout reset (BOR)

The device has an integrated power-on reset (POR) / power-down reset (PDR), coupled with a Brownout reset (BOR) circuitry. The BOR is active in all power modes except Shutdown mode, and cannot be disabled.

Five BOR thresholds can be selected through option bytes.

During power-on, the BOR keeps the device under reset until the supply voltage V_{DD} reaches the specified V_{BORx} threshold. When V_{DD} drops below the selected threshold, a device reset is generated. When V_{DD} is above the V_{BORx} upper limit, the device reset is released and the system can start.

On STM32L5 devices, continuous monitoring of the power supply might be changed to periodical sampling to reduce power consumption in Stop2, Standby and Shutdown modes. This setup can be done by setting ENULP bit in the power status register 3 (PWR_SR3).

Sampling time is controlled by internal temporization, the typical duration is of 12 ms at 25°C; the duration shortens exponentially with an increasing temperature. At around 70°C, the monitoring becomes continuous. When the sampling mode is activated, a fast supply-drop between two samples is not detected. This feature is targeting mainly battery operated devices.

For more details on the Brownout reset thresholds, refer to the electrical characteristics section in the datasheet.

Figure 9. **Brownout reset waveform**
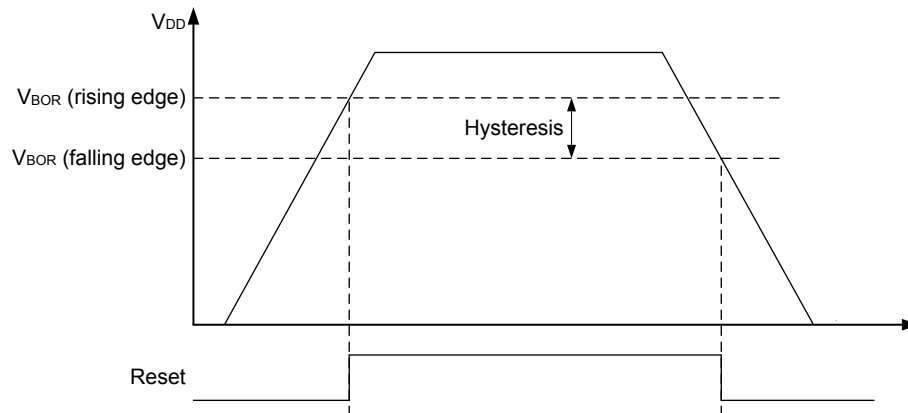
2.4.2 Power reset

A power reset is generated when one of the following events occurs:

1. a Brownout reset (BOR).
2. when exiting from Standby or Shutdown mode.

A Brownout reset, including power-on or power-down reset (POR/PDR), sets all registers to their reset values except the Backup domain.

When exiting Standby or Shutdown mode, all registers in the V_{CORE} domain are set to their reset value. Registers outside the V_{CORE} domain (RTC, WKUP, IWDG, and Standby/Shutdown modes control) are not impacted.

2.4.3 System reset

A system reset sets all registers to their reset values except the reset flags in the clock control/status register (RCC_CSR) and the registers in the Backup domain.

A system reset is generated when one of the following events occurs:

*   A low level on the NRST pin (external reset)
*   Window watchdog event (WWDG reset)
*   Independent watchdog event (IWDG reset)
*   A firewall event (FIREWALL reset)
*   A software reset (SW reset)
*   Low-power management reset
*   Option byte loader reset
*   A Brownout reset

The reset source can be identified by checking the reset flags in the control/status register, RCC_CSR.

These sources act on the NRST pin and it is always kept low during the delay phase. The RESET service routine vector is fixed at address 0x0000_0004 in the memory map.

The system reset signal provided to the device is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In case of an external reset, the reset pulse is generated while the NRST pin is asserted low.

In case on an internal reset, the internal pull-up R_{PU} is deactivated in order to save the power consumption through the pull-up resistor.

Figure 10. Simplified diagram of the reset circuit
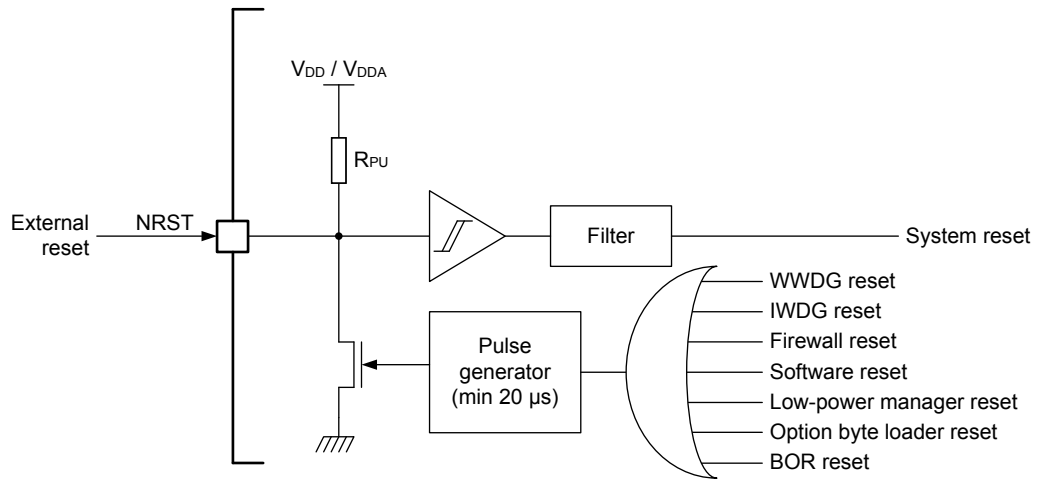
Software reset

The SYSRESETREQ bit in Cortex®-M33 application interrupt and reset control register must be set to force a software reset on the device).

Low-power mode security reset

To prevent that critical applications mistakenly enter a low-power mode, two low-power mode security resets are available. If enabled in option bytes, the resets are generated in the following conditions:

1. Entering Standby mode: this type of reset is enabled by resetting nRST_STDBY bit in User option Bytes. In this case, whenever a Standby mode entry sequence is successfully executed, the device is reset instead of entering Standby mode.
2. Entering Stop mode: this type of reset is enabled by resetting nRST_STOP bit in User option bytes. In this case, whenever a Stop mode entry sequence is successfully executed, the device is reset instead of entering Stop mode.
3. Entering Shutdown mode: this type of reset is enabled by resetting nRST_SHDW bit in User option bytes. In this case, whenever a Shutdown mode entry sequence is successfully executed, the device is reset instead of entering Shutdown mode.

For further information on the User Option Bytes, refer to reference manual section: *Option bytes description*.

Option byte loader reset

The option byte loader reset is generated when the OBL_LAUNCH bit (bit 27) is set in the FLASH_CR register. This bit is used to launch the option byte loading by software.

Charging/discharging the pull-down capacitor through the internal resistor adds to the device power consumption. The recommended value of 100 nF for the capacitor can be reduced to 10 nF to limit power consumption.

2.4.4 Backup domain reset

The Backup domain has two specific resets.

A Backup domain reset is generated when one of the following events occurs:

1. Software reset, triggered by setting the BDRST bit in the Backup domain control register (RCC_BDCR).
2. V_{DD} or V_{BAT} power on, if both supplies have previously been powered off.

A Backup domain reset only affects the LSE oscillator, the RTC, the backup registers and the RCC Backup domain control register.

3 Packages

3.1 Package selection

Package should be selected by taking into account the constraints that are strongly dependent upon the application.

The list below summarizes the most frequent ones:

- Amount of interfaces required. Some interfaces might not be available on some packages. Some interfaces combinations might not be possible on some packages.
- PCB technology constrains. Small pitch and high ball density could require more PCB layers and higher class PCB.
- Package height.
- PCB available area.
- Noise emission or signal integrity of high speed interfaces.

    Smaller packages usually provide better signal integrity. This is further enhanced as small pitch and high ball density requires multilayer PCBs which allow better supply/ground distribution.
- Compatibility with other devices.

Table 2. Package summary for STM32L5 Series

Package	Size (mm) [1]	Pitch (mm)	Height (mm) [2]	Legacy	External SMPS	Step-down converter
UFQFN48	7 x 7	0.5	0.6	x	x	-
LQFP48	7 x 7	0.5	1.6	x	x	-
LQFP64	10 x 10	0.5	1.6	x	x	x
WLCSP81	4.36 x 4.07	0.4	0.59	-	x	x
LQFP100	14 x 14	0.5	1.6	x	-	x
UFBGA132	7 x 7	0.5	0.6	x	x	x
LQFP144	20 x 20	0.5	1.6	x	-	x

1. Body size, excluding pins for LQFP.
2. Maximum value

3.2 Pinout compatibility

Table 3. Pinout summary for STM32L5 Series

Pin name	STM32L5x2xxxx Packages						STM32L5x2xxxxP Packages (External SMPS)					STM32L5x2xxxxQ Packages (Internal SMPS)				
	UFQFPN	LQFP				UFBGA	UFQFPN	LQFP		UFBGA	WLCSP	UFQFPN	LQFP		UFBGA	WLCSP
	48	48	64	100	144	132	48	48	64	132	81	64	100	144	132	81
Specific IOs																
PC14	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
PC15	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
PH0/OSC_IN	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
PH1_OSC_OUT	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
System pins																
BOOT0/PH3	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
NRST	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Power pins																
VBAT	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
VDDUSB	-	-	x	x	x	x	-	-	x	x	x	x	x	x	x	x
VSSA [1]	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-
VREF- [1]	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-
VDDA [2]	-	-	-	x	x	x	-	-	-	x	x	-	x	x	x	x
VREF+ [2]	-	-	-	x	x	x	-	-	-	x	x	-	x	x	x	x
VDDIO2	-	-	-	-	x	x	-	-	-	x	x	-	-	x	x	x
VDD12_1 VDD12_2	-	-	-	-	-	-	x	x	x	x	x	-	-	-	-	-
VDDSMPS	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x
VSSSMPS	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x
V15SMPS_1 V15SMPS_2	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x
VLXSMPS	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x

1. "-" means that VSSA and VREF- are connected internally and available on a single pin.
2. "-" means that VDDA and VREF+ are connected internally and available on a single pin.

4 Clocks

Four different clock sources can be used to drive the system clock (SYSCLK):

- HSI16 (high speed internal) 16 MHz RC oscillator clock
- MSI (multispeed internal) RC oscillator clock
- HSE oscillator clock, from 4 to 48 MHz
- PLL clock

The MSI is used as system clock source after startup from Reset, configured at 4 MHz.

The devices have the following additional clock sources:

- 32 kHz low speed internal RC (LSI RC) which drives the independent watchdog and optionally the RTC used for Auto-wakeup from Stop and Standby modes.
- 32.768 kHz low speed external crystal (LSE crystal) which optionally drives the real-time clock (RTCCLK).
- RC 48 MHz internal clock sources (HSI48) to potentially drive the USB full speed, the SDMMC and the RNG.

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

Several prescalers can be used to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB, the APB1 and the APB2 domains is 110 MHz.

4.1 HSE clock

The high speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE external crystal/ceramic resonator
- HSE user external clock

The resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

Table 4. HSE/LSE clock sources

Clock source	Hardware configuration
External clock	OSC_IN · OSC_OUT · GPIO · External souce
External clock (available on some packages, refer to the corresponding datasheet)	CK_IN · GPIO · External souce

Clock source	Hardware configuration
Crystal/ceramic resonators	OSC_IN OSC_OUT C_{L1} C_{L2} Load capacitors

1. The value of R_{EXT} depends on the crystal characteristics. A typical value is in the range of 5 to 6 R_S (resonator series resistance).To fine tune the R_{EXT} value, refer to AN2867 (Oscillator design guide for ST microcontrollers).
2. Load capacitance, C_L, has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where: C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF. Refer to Section 7.4 Decoupling to minimize its value.

4.1.1 External crystal/ceramic resonator (HSE crystal)

The 4- to 48-MHz external oscillator has the advantage of producing a very accurate rate on the main clock.

The associated hardware configuration is shown in Table 4. HSE/LSE clock sources . Refer to the electrical characteristics section of the datasheet for more details.

The HSERDY flag in the *clock control register (RCC_CR)* indicates if the HSE oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the *clock interrupt enable register (RCC_CIER)*.

The HSE crystal can be switched on and off using the HSEON bit in the clock control register (RCC_CR).

4.1.2 External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 48 MHz. The user selects this mode by setting the HSEBYP and HSEON bits in the *clock control register (RCC_CR)*. The external clock signal (square, sinus or triangle) with ~40-60% duty cycle depending on the frequency (refer to the datasheet) has to drive the following pin (see Table 4. HSE/LSE clock sources).

- On devices where OSC_IN and OSC_OUT pins are available: OSC_IN pin must be driven while the OSC_OUT pin can be used as a GPIO.
- Otherwise, the CK_IN pin must be driven.

Note: *For details on pin availability, refer to the pinout section in the corresponding device datasheet.*

To minimize the consumption, it is recommended to use the square signal.

4.2 HSI16 clock

The HSI16 clock signal is generated from an internal 16 MHz RC oscillator.

The HSI16 RC oscillator has the advantage of providing a clock source at low cost (no external components). It also has a faster startup time than the HSE crystal oscillator however, even with calibration the frequency is less accurate than an external crystal oscillator or ceramic resonator.

The HSI16 signal can also be used as a backup source (auxiliary clock) if the HSE crystal oscillator fails. Refer to reference manual section: *Clock security system (CSS)*.

4.3 MSI clock

The MSI clock signal is generated from an internal RC oscillator. Its frequency range can be adjusted by software by using the MSIRANGE[3:0] bits in the clock control register (RCC_CR). Twelve frequency ranges are available: 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz.

The MSI RC oscillator has the advantage of providing a low-cost (no external components) low-power clock source. In addition, when trimmed by the 32.768 kHz external oscillator (LSE), the MSI can provide the USB device with very accurate clock removing the need for an external high speed crystal (HSE).

4.3.1 Hardware auto calibration with LSE (PLL-mode)

When a 32.768 kHz crystal is present in the application, it is possible to configure the MSI in a PLL-mode by setting the MSIPLLEN bit in the *clock control register (RCC_CR)*. When configured in PLL-mode, the MSI automatically calibrates itself thanks to the LSE. This mode is available for all MSI frequency ranges. At 48 MHz, the MSI in PLL-mode can be used for the USB FS device, saving the need of an external high-speed crystal.

For more details on how to calibrate the MSI frequency variation, refer to reference manual section: *Internal/ external clock measurement with TIM15/TIM16/TIM17*.

4.4 LSE clock

The LSE crystal is a 32.768 kHz low speed external crystal or ceramic resonator. It has the advantage of providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The LSE crystal is switched on and off using the LSEON bit in *backup domain control register (RCC_BDCR)*. The crystal oscillator driving strength can be changed at runtime using the LSEDRV[1:0] bits in the *backup domain control register (RCC_BDCR)* to obtain the best compromise between robustness and short start-up time on one side and low-power-consumption on the other side. The LSE drive can be decreased to the lower drive capability (LSEDRV=00) when the LSE is ON. However, once LSEDRV is selected, the drive capability can not be increased if LSEON=1.

The LSERDY flag in the AHB1 peripheral clocks enable in Sleep and Stop modes register (RCC_AHB1SMENR) indicates whether the LSE crystal is stable or not. At startup, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the *clock interrupt enable register (RCC_CIER)*.

4.4.1 External source (LSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHz. The user selects this mode by setting the LSEBYP and LSEON bits in the AHB1 peripheral clocks enable in *Sleep and Stop modes register (RCC_AHB1SMENR)*. The external clock signal (square, sinus or triangle) with ~50 % duty cycle has to drive the OSC32_IN pin while the OSC32_OUT pin can be used as GPIO. See Table 4. HSE/LSE clock sources.

5 Boot configuration

5.1 Boot mode selection

At startup, a BOOT0 pin, nBOOT0 and NSBOOTADDx [24:0] / SECBOOTADD0 [24:0] option bytes are used to select the boot memory address which includes:

• Boot from any address in user Flash

• Boot from system memory bootloader

• Boot from any address in embedded SRAM

• Boot from root security service (RSS)

Refer to the following tables for boot modes when TrustZone® is disabled and enabled.

Table 5. Boot modes when TrustZone is disabled (TZEN=0)

nBOOT0 FLASH_OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR[26]	Boot address option-bytes selection	Boot area	ST programmed default value
-	0	1	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
-	1	1	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000
1	-	0	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
0	-	0	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000

When TrustZone is enabled by setting the TZEN option bit, the boot space must be in secure area. The SECBOOTADD0 [24:0] option bytes are used to select the boot secure memory address.

A unique boot entry option can be selected by setting the BOOT_LOCK option bit. All other boot options are ignored.

Table 6. Boot modes when TrustZone is enabled (TZEN=1)

BOOT_LOCK	nBOOT0 FLASH_OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR[26]	RSS command	Boot address option-bytes selection	Boot area	ST programmed default value
0	-	0	1	0	SECBOOTADD0 [24:0]	Secure boot address defined by user option bytes SECBOOTADD0 [24:0]	Flash: 0x0C00 0000
	-	1	1	0	N/A	RSS: 0x0FF8 0000	RSS: 0x0FF8 0000
	1	-	0	0	SECBOOTADD0 [24:0]	Secure boot address defined by user option bytes SECBOOTADD0 [24:0]	Flash: 0x0C00 0000
	0	-	0	0	N/A	RSS: RSS: 0x0FF8 0000	RSS: 0x0FF8 0000
	-	-	-	≠ 0	N/A	RSS: RSS: 0x0FF8 0000	RSS: 0x0FF8 0000

BOOT_LOCK	nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	RSS command	Boot address option-bytes selection	Boot area	ST programmed default value
1	-	-	-	-	SECBOOTADD0 [24:0]	Secure boot address defined by user option bytes SECBOOTADD0 [24:0]	Flash: 0x0C00 0000

Note: *When the device boots from SRAM, in the application initialization code, the user has to relocate the vector table in SRAM using the NVIC exception table and the offset register.*

5.2 Embedded bootloader and RSS

The embedded bootloader is located in the system memory and programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces:

- USART1 on pins PA9/PA10, USART2 on pins PA2/PA3, USART3 on pins PC10/PC11
- I2C1 on pins PB6/PB7, I2C2 on pins PB10/PB11, I2C3 on pins PC0/PC1
- SPI1 on pins PA4/PA5/PA6/PA7, SPI2 on pins PB12/PB13/PB14/PB15, SPI3 on pins PB5/PG9/PG10/PG12
- USB DFU interface on pins PA11/PA12
- FDCAN1 on pins PB8/PB9

For further details on STM32 bootloader, refer to AN2606.

The root secure services (RSS) are embedded in a Flash memory area named secure information block, programmed during ST production.

The RSS enables for example the secure firmware installation (SFI) using the RSS extension firmware (RSSe SFI).

This feature allows the customers to protect the confidentiality of the firmware to be provisioned into the STM32 device when the production is subcontracted to a third party.

The RSS is available on all devices, after enabling the TrustZone through the TZEN option bit.

6 Debug management

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a SW connector and a cable connecting the host to the debug tool.

The following figure shows the connection of the host to a development board.

Figure 11. Host-to-board connection
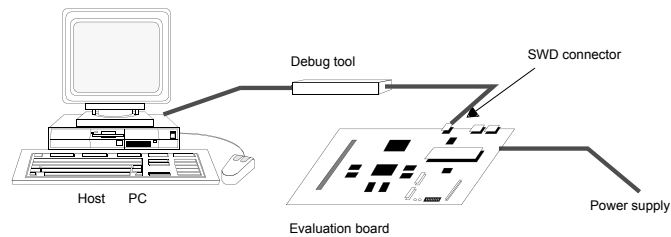
The Nucleo demonstration board embeds the debug tools (ST-LINK) so it can be directly connected to the PC through an USB cable. The ST-LINK requires by default to have an enumeration with a host that is able to supply 100 mA to power the STM32L5 MCU, hence user must use jumper JP1 on the Nucleo board which can be set in case maximum current consumption on U5V does not exceed 100 mA.

6.1 SWJ debug port (JTAG and serial wire)

The STM32L5 Series core integrates the serial wire / JTAG debug port (SWJ-DP). It is an Arm standard CoreSight™ debug port that combines a JTAG-DP (5-pin) interface and a SW-DP (2-pin) interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port

6.2 Pinout and debug port pins

The STM32L5 Series devices are offered in various packages with different numbers of available pins. As a result, some functionality related to the pin availability may differ from one package to another.

6.2.1 SWJ debug port pins

Five pins are used as outputs for the SWJ-DP as alternate functions of general-purpose I/Os (GPIOs). These pins, shown in Table 7. Debug port pin assignment, are available on all packages.

Table 7. Debug port pin assignment

SWJ-DP pin name	Type	Description	Type	Debug assignment	Pin assignment
		JTAG debug port		SW debug port	
JTMS/SWDIO	I	JTAG test mode selection	I/O	Serial wire data input/output	PA13
JTCK/SWCLK	I	JTAG test clock	I	Serial wire clock	PA14
JTDI	I	JTAG test data input	-	-	PA15
JTDO/TRACESWO	O	JTAG test data output	-	TRACESWO if async trace is enabled	PB3
JNTRST	I	JTAG test nReset	-	-	PB4

6.2.2 Flexible SWJ-DP pin assignment

After reset (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins which are immediately usable by the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

Table 8. SWJ I/O pin availability shows the different possibilities for releasing some pins. For more details, see the related STM32L5 Series reference manual.

Table 8. SWJ I/O pin availability

Available debug ports	SWJ I/O pin assigned				
	PA13 / JTMS/ SWDIO	PA14 / JTCK/ SWCLK	PA15 / JTDI	PB3 / JTDO	PB4/ JNTRST
Full SWJ (JTAG-DP + SW-DP) - reset state	X	X	X	X	X
Full SWJ (JTAG-DP + SW-DP) but without JNTRST	X	X	X	X	
JTAG-DP disabled and SW-DP enabled	X	X	-		-
JTAG-DP disabled and SW-DP disabled	Released				

6.2.3 Internal pull-up and pull-down resistors on JTAG pins

The JTAG input pins must *not* be floating since they are directly connected to flip-flops which control the debug mode features. Special care must be taken with the SWCLK/TCK pin that is directly connected to the clock of some of these flip-flops.

To avoid any uncontrolled I/O levels, the STM32L5 Series embeds internal pull-up and pull-down resistors on the JTAG input pins:

- JNTRST: internal pull-up
- JTDI: internal pull-up
- JTMS/SWDIO: internal pull-up
- TCK/SWCLK: internal pull-down

Once a JTAG I/O is released by the user software, the GPIO controller takes control again. The reset states of the GPIO control registers put the I/Os in the following equivalent states:

- JNTRST: input pull-up
- JTDI: input pull-up
- JTMS/SWDIO: input pull-up
- JTCK/SWCLK: input pull-down
- JTDO: input floating

The software can then use these I/Os as standard GPIOs.

Note: *The JTAG IEEE standard recommends to add pull-up resistors on TDI, TMS and nTRST but, there is no special recommendation for TCK. However, for the STM32L5 Series, an integrated pull-down resistor is used for JTCK.*

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

6.2.4 SWJ debug port connection with standard JTAG connector

The following figure shows the connection between the STM32L5 Series devices and a standard JTAG connector.

Figure 12. JTAG connector implementation
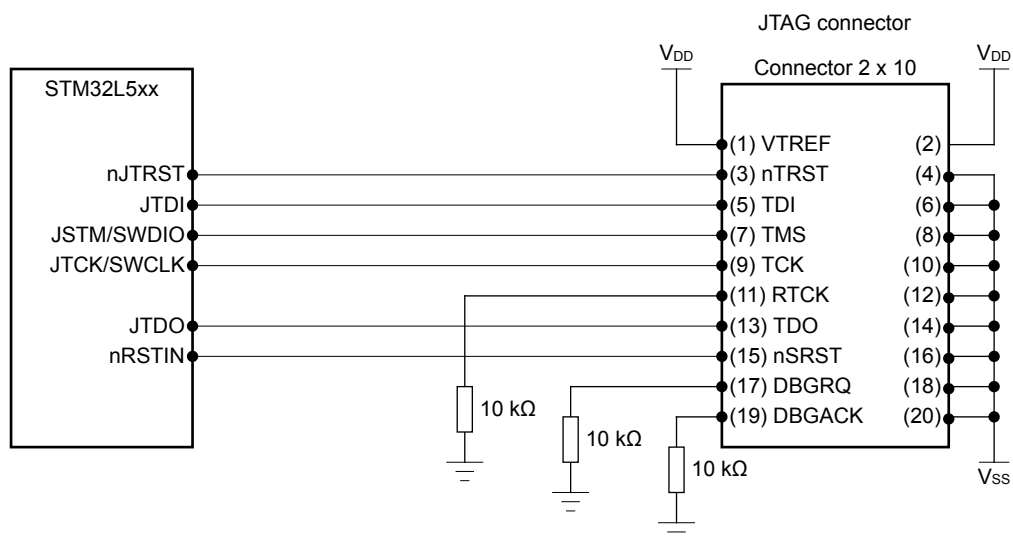
6.3 Serial wire debug (SWD) pin assignment

The same SWD pin assignment is available on all STM32L5 Series packages.

Table 9. SWD port pins

SWD pin name	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	I/O	Serial wire data input/output	PA13
SWCLK	I	Serial wire clock	PA14

6.3.1 SWD pin assignment

After reset (SYSRESETn or PORESETn), the pins used for the SWD are assigned as dedicated pins which are immediately usable by the debugger host.

However, the MCU offers the possibility to disable the SWD, therefore releasing the associated pins for general-purpose I/O (GPIO) usage. For more details on how to disable SWD port, refer to the I/O pin alternate function multiplexer and mapping section of the related STM32L5 Series reference manual.

6.3.2 Internal pull-up and pull-down on SWD pins

Once the SWD I/O is released by the user software, the GPIO controller takes control of these pins. The reset states of the GPIO control registers put the I/Os in the equivalent states:

- SWDIO: alternate function pull-up
- SWCLK: alternate function pull-down

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

6.3.3 SWD port connection with standard SWD connector

The following figure shows the connection between the STM32L5 Series and a standard SWD connector.

Figure 13. SWD port connection
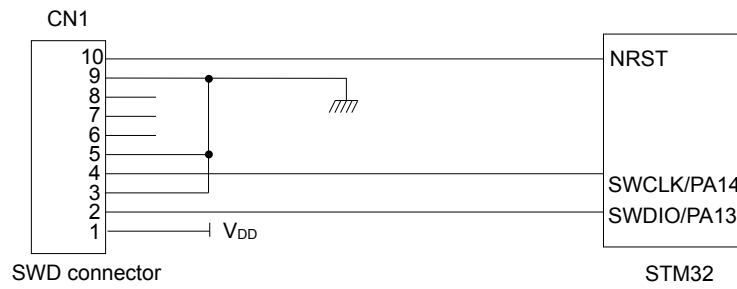
7 Recommendations

7.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

7.2 Component position

A preliminary layout of the PCB must separate circuits into different blocks:

- High-current circuits
- Low-voltage circuits
- Digital component circuits
- Circuits separated according to their EMI contribution in order to reduce noise due to cross-coupling on the PBC.

7.3 Ground and power supply (V_{SS}, V_{DD}, V_{SSA}, V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{DDSMPS})

Respect the following rules related to grounding:

- Ground every block (noisy, low-level sensitive, digital or others) individually
- Return all grounds to a single point
- Avoid loops (or ensure they have a minimum area)

In order to improve analog performance, the user must use separate supply sources for V_{DD} and V_{DDA}, and place the decoupling capacitors as close as possible to the device.

The power supplies should be implemented close to the ground line to minimize the area of the supplies loop. This is due to the fact that the supply loop acts as an antenna, and acts as the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

7.4 Decoupling

All power supply and ground pins must be properly connected to the power supplies. These connections (including pads, tracks and vias) must have an impedance as low as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors (100 nF) and a Tantalum or ceramic capacitor of about 10 µF connected in parallel on the STM32L5 Series device. Some package use a common V_{SS} for several V_{DD} instead of a pair of power supply (one V_{SS} for each V_{DD}), in that case the capacitors must be between each V_{DD} and the common V_{SS}.These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application needs. The following figure shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 14. Typical layout for V$_{DD}$/V$_{SS}$
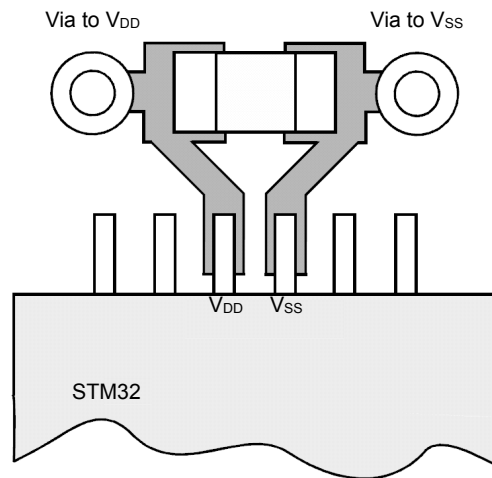
7.5 Other signals

When designing an application, the EMC performance can be improved by closely studying the following:

- Signals for which a temporary disturbance affects the running process permanently (which is the case for interrupts and handshaking strobe signals but, not the case for LED commands).

   For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.

   For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.

- Noisy signals (example, clock)
- Sensitive signals (example, high impedance)

7.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance and avoid extra power consumption, the unused features of the device should be disabled and disconnected from the clock tree. The unused clock source should be disabled and the unused I/Os should not be left floating. The unused I/O pins should be configured as analog input by software; they should also be connected to a fixed logic level 0 or 1 by an external or internal pull-up or pull-down or configured as output mode using software.

8 Reference design

8.1 Description

The reference designs shown in the following reference design figures are based on the STM32L5 Series LQFP144.

This reference design can be tailored to any STM32L5 Series device with a different package, using the pin correspondence given in Section 8.2 Component references.

8.1.1 Clock

Two clock sources are used for the microcontroller:

- LSE: X2– 32.768 kHz crystal for the embedded RTC
- HSE: X1– 8 MHz crystal for the STM32L5 Series microcontroller

Refer to Section 4 Clocks.

8.1.2 Reset

The reset signal in the Reference design figures shown in Section 8.2 Component references is active low. The reset sources include:

- Reset button (B1)
- Debugging tools via the connector CN1

Refer to Section 2.4 Reset and power supply supervisor.

8.1.3 Boot mode

The boot option is configured by setting switches SW1 (Boot 0). Refer to Section 5 Boot configuration.

Note: *When waking up from Standby mode, the Boot pin is sampled. In this situation, the user needs to pay attention to its value.*

8.1.4 SWD interface

The reference design shows the connection between the STM32L5 Series and a standard SWD connector. Refer to Section 6 Debug management.

Note: *It is recommended to connect the reset pins so as to be able to reset the application from the tools.*

8.1.5 Power supply

Refer to Section 2 Power supplies management.

8.2 Component references

Table 10. Mandatory components

Reference	Component name	Value	Quantity	Comments
U1A	Microcontroller	STM32L5 Series LQFP144	1	144-pin package
C8, C11, C13	Capacitor	100 nF	10 + 2	Ceramic capacitors (decoupling capacitors)
C9, C10	Capacitor	4.7 µF	1	Tantalum / chemical / ceramic capacitor (decoupling capacitor)
C6, C16	Capacitor	1 µF	3	Ceramic capacitor (decoupling capacitor)
C14, C15	Capacitor	1 µF	1	Ceramic capacitor (decoupling capacitor) used for internal voltage reference buffer
C	Capacitor	4.7 µF	1	SMPS output capacitor, used in the STM32L5x2xxxxQ
L	Inductor	4.7 µH	1	SMPS inductance, used in the STM32L5x2xxxxQ

Table 11. Optional components

Reference	Component name	Value	Quantity	Comments
R1	Resistor	390 Ω	1	Used for HSE: the value depends on the crystal characteristics, refer to application note AN2687
R3, R4, R5	Resistor	10 kΩ	3	Used for ST Link interface
C5	Capacitor	100 nF	1	Ceramic capacitor
C7	Capacitor	10 nF	1	Ceramic capacitor
C1, C2	Capacitor	6.8 pF	2	Used for LSE: the value depends on the crystal characteristics. Fits for MC-306 32.768K-E3, which has a load capacitance of 6 pF.
C3, C4	Capacitor	20 pF	2	Used for HSE: the value depends on the crystal characteristics, refer to application note AN2687
X1	Quartz	8 MHz	1	Used for HSE
X2	Quartz	32.764 kHz	1	Used for LSE
SW1	Switch	-	1	Used to select the right boot mode
B1	Push-button	-	1	-
L1	Ferrite bead	-	1	For EMC reduction on V_{DDA} supply, can be replaced by a direct connection between V_{DD} and V_{DDA}

Figure 15. STM32L5x2xx reference design
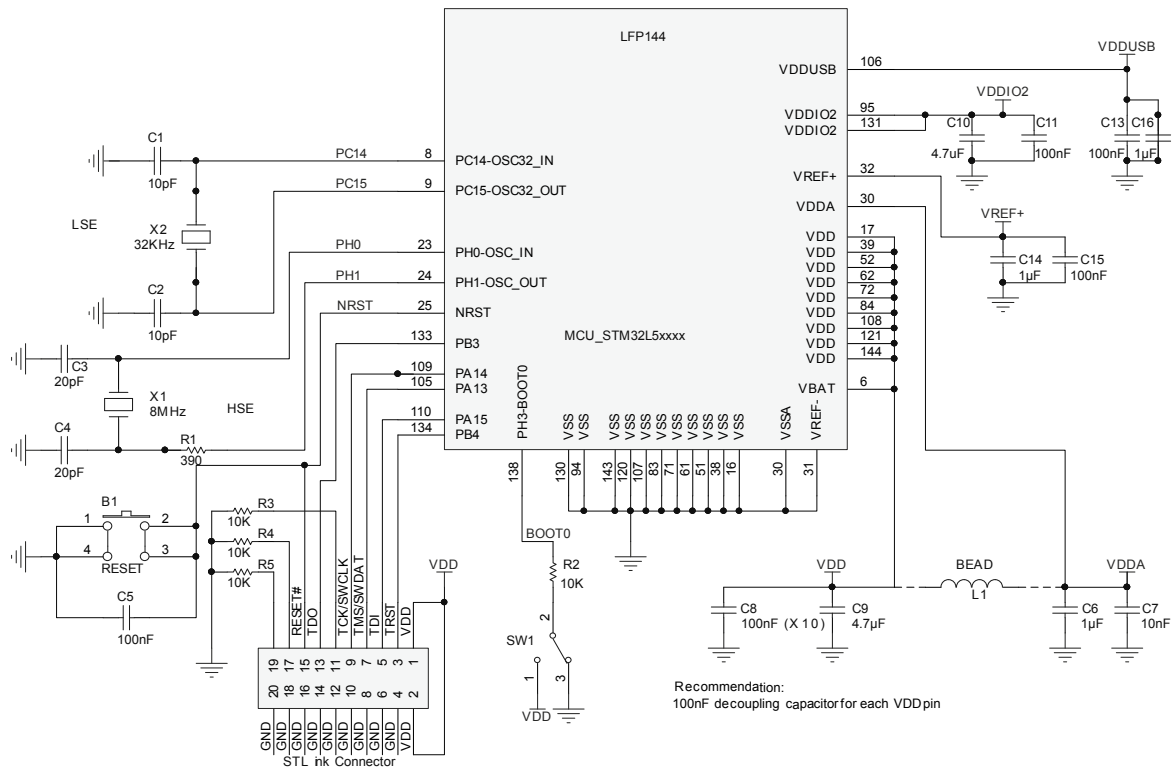
Figure 16. STM32L5x2xxxxQ Series reference design
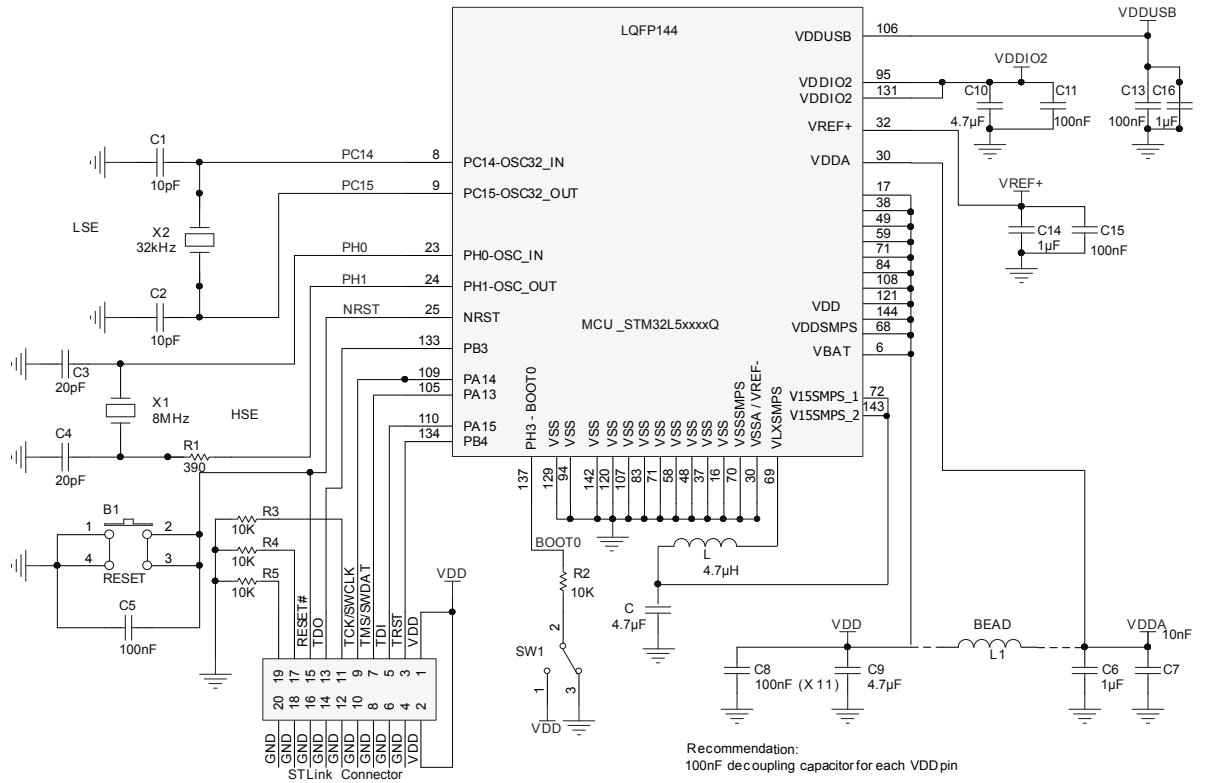
Revision history

Table 12. Document revision history

Date	Version	Changes
04-Oct-2019	1	Initial release.

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IMPORTANT NOTICE – PLEASE READ CAREFULLY