AN5071
Application note

STM32WB ultra-low-power features overview

Introduction

Microcontrollers of the STM32WB Series are built using an innovative architecture to reach best-in-class, ultra-low power figures thanks to their high flexibility, powerful Radio and advanced set of peripherals. They can operate up to 64 MHz and achieve 80 DMIPS performances at 64 MHz, thanks to the integration of the ART Accelerator™ while maintaining the smallest possible dynamic power consumption.

The STM32WB MCUs include a low power RF proprietary subsystem, having its own dedicated Arm® Cortex®-M0+ to offload the Cortex®-M4 from performing real-time RF communication tasks, resulting in best power efficiency between the user and the communication tasks.

The STM32WB MCUs feature the FlexPowerControl, which increases flexibility in the power modes management while at the same time reducing the overall application consumption.

The STM32WB devices embed a high number of smart and performing peripherals, a large set of advanced and low-power analog features, and several peripherals tuned for low-power modes. Thanks to the batch acquisition sub-mode (BAM), these microcontrollers optimize the consumption when data are transferred with communication peripherals, while the rest of the device is kept in low-power mode.

Based on the solid foundations the STM32L4 Series, already embedding several innovations to minimize the consumption in the different modes while maintaining most of the existing peripherals, the STM32WB allow an easy migration from a dual chip solution (STM32L4 + Bluetooth Low Energy / 802.15.4) to a single chip, with almost the same power budget.

The STM32WB MCUs include an embedded SMPS that improves even more the power figures in applications where the supply voltage is high, as well as the overall consumption.

Thanks to their built-in internal voltage regulator and voltage scaling, device consumption in active modes is kept at a minimum, whatever the external supply voltage. This makes these devices particularly suited for portable battery-supplied products, down to 1.71 V. In addition, their multi-voltage domains allow to supply the product at low voltage (thus reducing consumption) while the analog-to-digital converters can operate with a higher supply and reference voltage, up to 3.6 V.

STM32WB microcontrollers support a battery backup domain to keep the RTC running, and a set of 20 registers, each 32-bit wide, that can be retained in case of power loss. This optional backup battery can be charged when the main supply is present.

The STM32WB devices support many low-power modes, each of them with several submodes options. This allows the designer to achieve the best compromise between low-power consumption figure, shorter startup time, available set of peripherals and maximum number of wake-up sources.

Contents

List of tables

List of figures

1 Energy-efficient processing

STM32WB MCUs are based on an Arm®(a) Cortex®-M4 with FPU and DSP instruction set.

The high processing performance in Run mode (expressed in DMIPS/MHz) is achieved thanks to the use of a Cortex®-M4 core associated with the interfaces of its memories. To ensure full performance operation up to 64 MHz, STM32WB microcontrollers embed the ART Accelerator™, which masks the Flash memory access wait state, and makes it possible to achieve 1.25 DMIPS/MHz, whatever the system clock frequency.

The high energy efficiency, expressed as mA/DMIPS, is obtained by adapting dynamically the internal supply voltage to the operating frequency. This method is called “undervolting”.

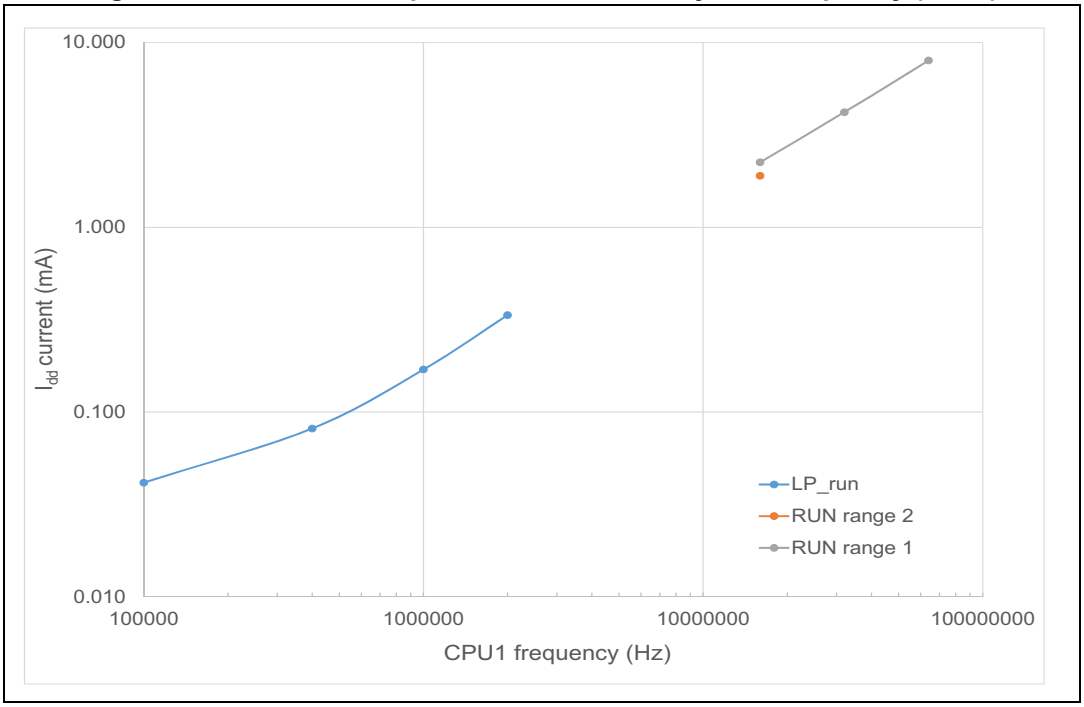
STM32WB MCUs offer two dynamically selectable voltages and frequency ranges:

1. Range 1 for system frequency up to 64 MHz
2. Range 2 for system frequency up to 16 MHz with improved efficiency (up to 15% higher than Range 1).

When the RF is not used a dedicated Low-power run mode (LPRun) allows the core to execute at up to 2 MHz, with improved efficiency, up to 20% higher compared to Range 2. Note that in this case the RF cannot be used, as it requests at least 32 MHz to operate.

Figure 1 shows the typical current consumption of the STM32WB55, as a function of system frequency, for different run modes.

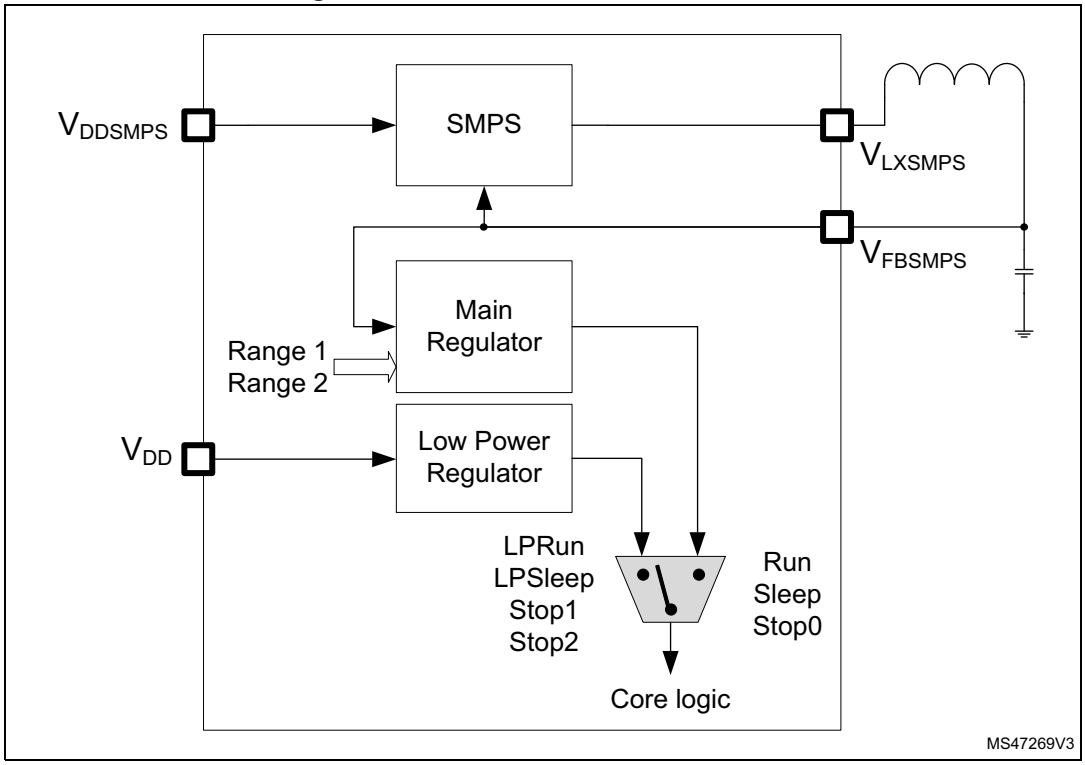
Figure 1. Current consumption vs. Cortex®-M4 system frequency (25 °C)



a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Figure 2 shows the power distribution from the internal LDO regulator in the different Run modes.

Figure 2. Power distribution architecture



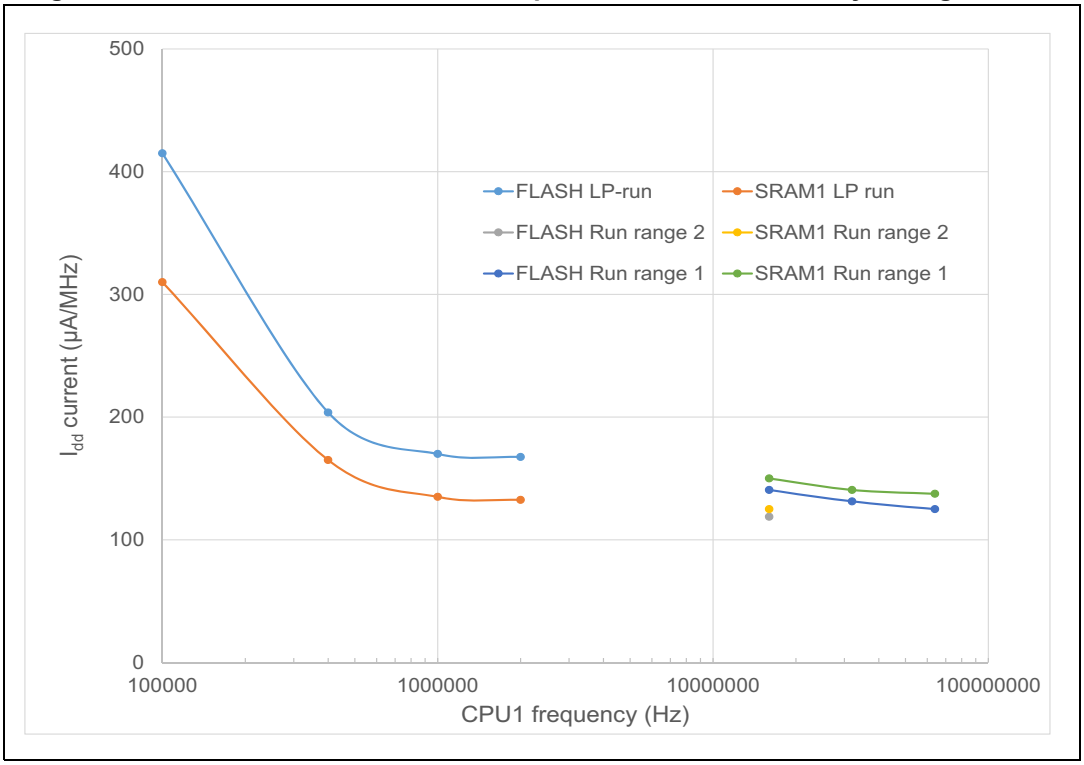
STM32WB microcontrollers allow the CPU1 Cortex®-M4 to execute code either from the internal Flash memory, the SRAM1 and SRAM2, or from the external Quad-SPI.

When running from internal SRAM the current consumption is the lowest. When running from the internal Flash memory the ART Accelerator™ tends to reduce the number of access to the memory thus reducing the overall current consumption. Note that when the RF subsystem is in use, the ART Accelerator cannot be disabled, as the Cortex®-M0+ and the Cortex®-M4 share the same Flash memory.

Figure 3 shows the consumption of the STM32WB55 for two main memory configurations:

- execution from the internal Flash memory, ART Accelerator™ enabled;
- execution from the internal SRAM1, Flash memory disabled.

Figure 3. STM32WB55 - Current consumption for different memory configurations



The location of the executable code and data within the memory system impacts not only the current consumption but also the overall computation performance. As an example, *Table 1* details the overall performances measured on a STM32WB55 at 64 MHz system clock running a more complex algorithm, such as CoreMark® from EEMBC® organization.

Table 1. STM32WB55 performance with system clock at 64 MHz

Configuration	mA/MHz	CoreMark® per MHz	CoreMark® per mA	Comments
FLASH ART On	0.125	3.25	26	Cache On, Prefetch buffer Off
SRAM1	0.117	2.40	20	Code and Data in SRAM1

The ART Accelerator™ allows to run the Cortex®-M4 core almost at the maximum efficiency figures published by Arm®. *Table 2* gives the impact of the SMPS on the same figures.

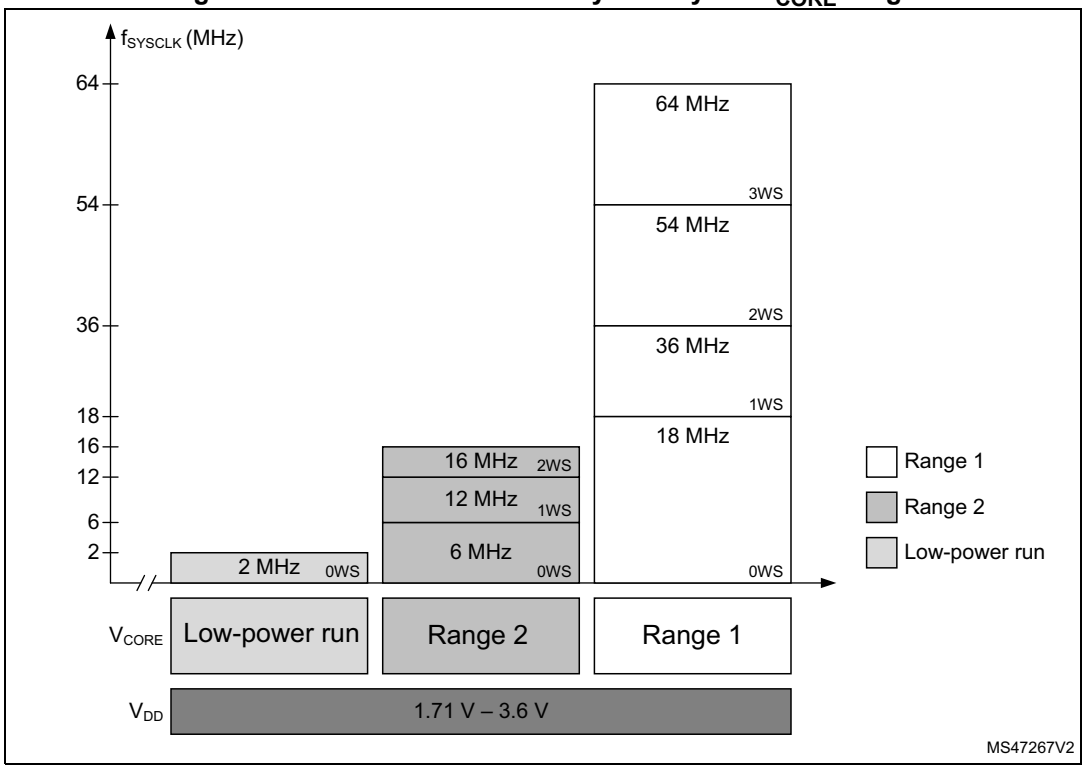
Table 2. STM32WB55 performance with SMPS

Configuration	mA/MHz	CoreMark® per MHz	CoreMark® per mA
FLASH ART On	0.077	3.25	42
SRAM1	0.073	2.40	33

Selection of the SMPS, when possible, improves the efficiency (CoreMark® per mA) by almost 40%.

Figure 4 shows the STM32WB Flash memory latency (number of wait states to be programmed in the Flash memory access control register), depending on regulator voltage scaling range and system clock frequency.

Figure 4. STM32WB Flash memory latency vs. V_{CORE} range



2 FlexPowerControl description

FlexPowerControl reduces the application power consumption thanks to high flexibility in the power management, smart peripherals and architecture.

The STM32WB features an independent management of the power state by the RF sub-system and the Cortex®-M4 application CPU. A dedicated HW mechanism selects the lowest possible power consumption state.

2.1 Several low-power modes

The STM32WB microcontrollers implement many different power modes, seven of them are low-power.

On top of these modes, the power consumption can be modulated by selecting different clock sources and frequencies, as well as clocking off peripherals not in use.

In all these modes, except Shutdown, the safe power monitoring Brown out reset (BOR) and the IWDG can stay active to guarantee safe execution.

Table 3 summarizes the features available for each mode and provides an indication of the current consumption, while *Figure 5* shows the possible transitions between low-power modes.

2.1.1 Low-power run and Low-power sleep modes

When the RF sub-system is not in use and when the application CPU can run below 2 MHz, the low power run mode and low power sleep mode result in the best power performance.

They offer Run and Sleep mode functionality for applications with extremely low current consumption where some peripherals cannot be switched off, or where the CPU is processing continuously at low speed to minimize current variations.

Several features have been put in place to reduce the current consumption:

- the core logic is supplied by the low-power voltage regulator to reduce the quiescent current;
- the Flash memory can be switched off (power-down mode and clock gating) in Low-power sleep mode. It can also be switched off in Low-power run when the application processor is executing from SRAM1;
- the system clock is limited to 2 MHz maximum. The MSI internal RC oscillator can be selected as it supports several frequency ranges, with a small MCU total consumption down to 48 µA in Low-power sleep Flash memory off at 100 kHz.

Batch acquisition sub-mode (BAM)

The STM32WB microcontrollers support the power efficient batch acquisition sub-mode (BAM), in which data are transferred with communication peripherals, while the rest of the device is in Low-power mode.

This is achieved by entering Sleep or Low-power sleep mode with this configuration:

- only the DMA, the communication peripheral(s) and the SRAM1 or SRAM2 clocks are enabled in Sleep (or Low-power sleep) mode;

- if the RF sub-system is not in use and system clock can be limited to 2 MHz, the main regulator is switched off (to enter Low-power sleep). In this case the Flash memory can be powered off.

In Low-power sleep mode, the I2C and USART/LPUART peripherals can still be clocked with HSI at 16 MHz, making it possible to support BAM with I2C or USART at up to 1 Mbps speed.

2.1.2 Stop mode

The STM32WB implement three Stop modes with full SRAM and Peripheral retention capability and capacity to wakeup in 1 µs thanks to the use of the MSI up to 48 MHz.

In these Stop modes all the high speed oscillators (HSE, MSI, HSI) are stopped, while the low speed ones (LSE, LSI) can be kept active. The peripherals can be set active, using the HSI clock when needed, to be able to wakeup the device on some specific events (such as UART character reception or I2C address recognition).

2.1.3 Standby mode

In Standby mode the BOR is always enabled, ensuring that the device will reset if the supply voltage drops below the selected functional threshold.

Standby mode with RAM2a retention is the lowest mode allowing the use of the RF sub-system.

Pull-up and pull-down can individually be applied on each I/O during the Standby mode, allowing external devices configuration to be kept.

Wakeup from this mode is done thanks to one of the five wakeup pins, the reset pin or the independent watchdog. The RTC clocked by the low-speed oscillators (LSE or LSI) is also functional in this mode, with wakeup capability. Wakeup from this mode can also be performed by the Radio sub-system.

2.1.4 Shutdown mode

The Shutdown mode is implemented in the STM32WB devices to lengthen even more the battery life of battery-powered applications.

This mode allows the lowest consumption, by switching off the internal voltage regulators, and by disabling the voltage power monitoring. Wakeup from this mode is done thanks to one of the five wakeup pins or to the reset pin. The RTC clocked by the low-speed external oscillator (LSE) is also functional in this mode, with wakeup capability. Wakeup from shutdown is equivalent to a POR.

Note: In this mode the RF sub-system cannot be used as all the BLE and 802.15.4 link parameters will have been lost.

Table 3. STM32WB55 modes overview

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA & Peripherals	Wakeup source	Consumption	Wakeup time(1)
Run	Range 1	Yes	ON(2)	ON	Any	All	N/A	107 µA/MHz	N/A
	Range2					All except True RNG and USB-FS(3)		100 µA/MHz	
LPRun	LPR	Yes	ON(5)	ON	Any except PLL	All except RF, True RNG and USB-FS	N/A	110 µA/MHz	19.5 µs
Sleep	Range 1	No	ON	ON(4)	Any	All	Any interrupt or event	41 µA/MHz	6 cycles
	Range 2					All except True RNG and USB-FS(3)		46 µA/MHz	
LPSleep	LPR	No	ON(5)	ON(4)	Any except PLL	All except RF, True RNG and USB-FS	Any interrupt or event	45 µA/MHz	6 cycles
Stop 0	Range 1	No	OFF	ON	LSE, LSI, HSE(6), HSI16(7)	RF(3), BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1(8) LPUART1(8) I2Cx (x=1, 3)(9) LPTIMx (x=1, 2), SMPS All other peripherals are frozen.	Reset pin, all I/Os, RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB	100 µA	1.7 µs
	Range 2								
Stop 1	LPR	No	OFF	ON	LSE, LSI, HSE(6), HSI16(7)	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1(14) LPUART1(14) I2Cx (x=1, 3)(15) LPTIMx (x=1, 2) All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB	9.0 µA w/o RTC 9.3 µA w RTC	4.7 µs

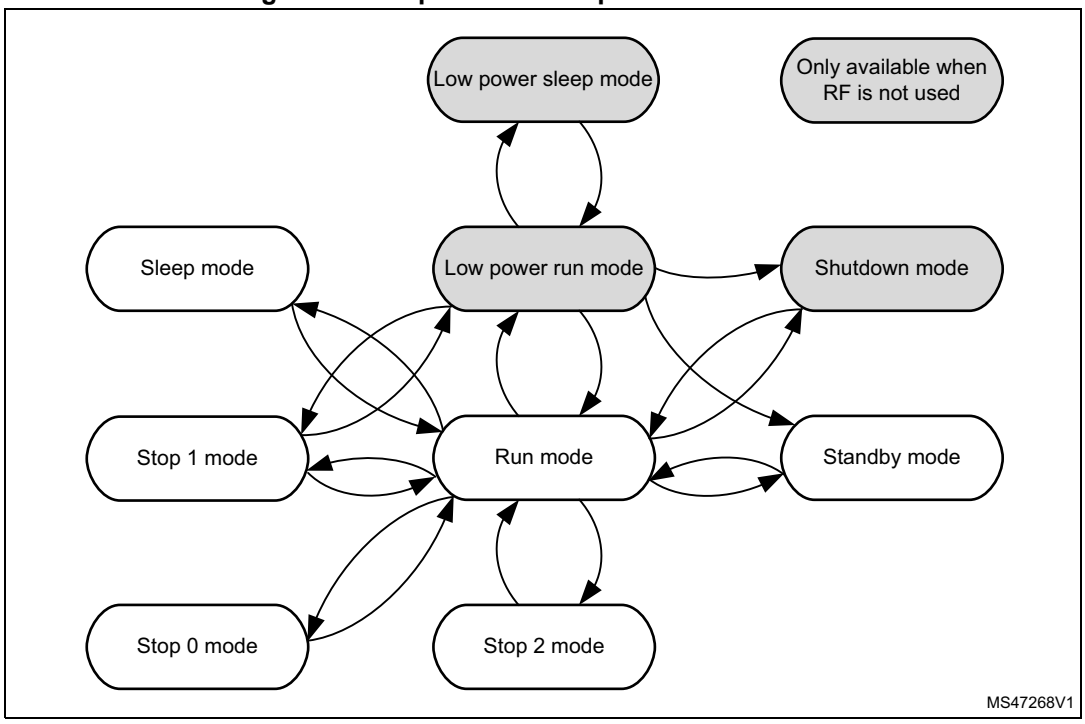
Table 3. STM32WB55 modes overview (continued)

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA & Peripherals	Wakeup source	Consumption	Wakeup time(1)
Stop 2	LPR	No	OFF	ON	LSE, LSI	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1(14) LPUART1(14) I2C3(9) LPTIM1 All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) LPUART1 I2C3 LPTIM1	1.8 µA w/o RTC 2.1 µA w RTC	5.1 µs
Standby	LPR	No	OFF	SRAM2a ON(10)	LSE, LSI	RF, BOR, RTC, IWDG All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down	RF, Reset pin 5 I/Os (WKUPx)(11) BOR, RTC, IWDG	0.72 µA w/o RTC 0.85 µA w RTC	52 µs
	OFF			OFF				0.61 µA w/o RTC 0.74 µA w RTC	
Shutdown	OFF	No	OFF	OFF	LSE	RTC All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down(12)	Reset pin 5 I/Os (WKUPx)(11), RTC	0.03 µA w/o RTC 0.32 µA w/ RTC	250 µs

1. Add 12 µs (max 100 µs) when using SMPS, except Sleep, LPSleep and Stop 0 where the SMPS is not stopped.
2. Flash memory programming is only possible in Range 2 voltage.
3. The RF subsystem is unable to operate in BLE mode.
4. The SRAM1 and SRAM2 clocks can be gated off independently.
5. The Flash memory controller can be placed in power-down mode if the RF subsystem is not in use and all the program is run (LPrun mode) from the SRAM.
6. HSE (32 MHz) automatically used when RF activity is needed by the RF subsystem.
7. HSI16 (16 MHz) automatically used by some peripherals.
8. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, Address match or Received frame event.
9. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
10. SRAM1 and SRAM2b are OFF.
11. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PC12, PA2, PC5.
12. I/Os can be configured with internal pull-up, pull-down or floating but the configuration is lost immediately when exiting the Shutdown mode.

Figure 5 describes the allowed transition between the different power states. Grey cells represent the states in which the RF sub-system cannot be used.

Figure 5. Low-power modes possible transitions



2.2 Multi-supply and battery backup domain

The STM32WB devices require a 1.71 to 3.6 V V_{DD} operating voltage supply.

Independent supplies (V_{DDA}, V_{DDUSB}), can be provided for specific peripherals, thus removing the constraint to supply all product at high voltage when analog or USB functions are used. Supplying the MCU with low V_{DD} voltage allows to reduce the consumption in the low power modes. When the peripherals supplied by the independent power supplies are not used in the application, those supplies should be connected to V_{DD}.

- V_{DD} and V_{DDSMPS} = 1.71 to 3.6 V

  V_{DD} is the external power supply for the I/Os, the RF sub-system, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
- V_{DDRF} = 1.71 to 3.6 V

  Supplies the RF reference voltage
- V_{DDA} minimum voltage:
  - 1.62 V if ADC or COMPs are used;
  - 2.4 V if the built-in Reference source need to be used for V_{REF}.

  V_{DDA} is the external analog power supply for A/D converters and comparators.
- V_{DDUSB} = 3.0 to 3.6 V (USB used)

  V_{DDUSB} is the external independent power supply for USB transceivers.

In addition the STM32WB devices support two voltage reference supplies:

- V_{LCD} = 2.5 to 3.6 V

  The voltage reference for the LCD (V_{LCD}) is used to control the contrast of the glass LCD. It can be provided either from external supply voltage or by embedded voltage step-up converter, independently of V_{DD} voltage (up to 3.6 V if V_{DD} > 2.0 V). VLCD is multiplexed with PC3 or with PB2, which can be used as GPIO when the LCD is not used.

- V_{REF+}

  V_{REF+} is the input reference voltage for the ADC. It is also the output of the internal voltage reference buffer when enabled. VREF+ pin, and thus internal voltage reference, is not available on all packages. When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disable (refer to datasheet for packages pinout description).

To retain the content of the Backup registers and supply the RTC function when V_{DD} is turned off, the VBAT pin can be connected to an optional backup voltage supplied by a battery or by another source:

- V_{BAT} = 1.55 to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz LSE oscillator and backup registers (through power switch) when V_{DD} is not present. When V_{DD} is present these peripherals (RTC, LSE) are automatically supplied by V_{DD}, and it is possible to charge the external battery on VBAT through an internal resistance.

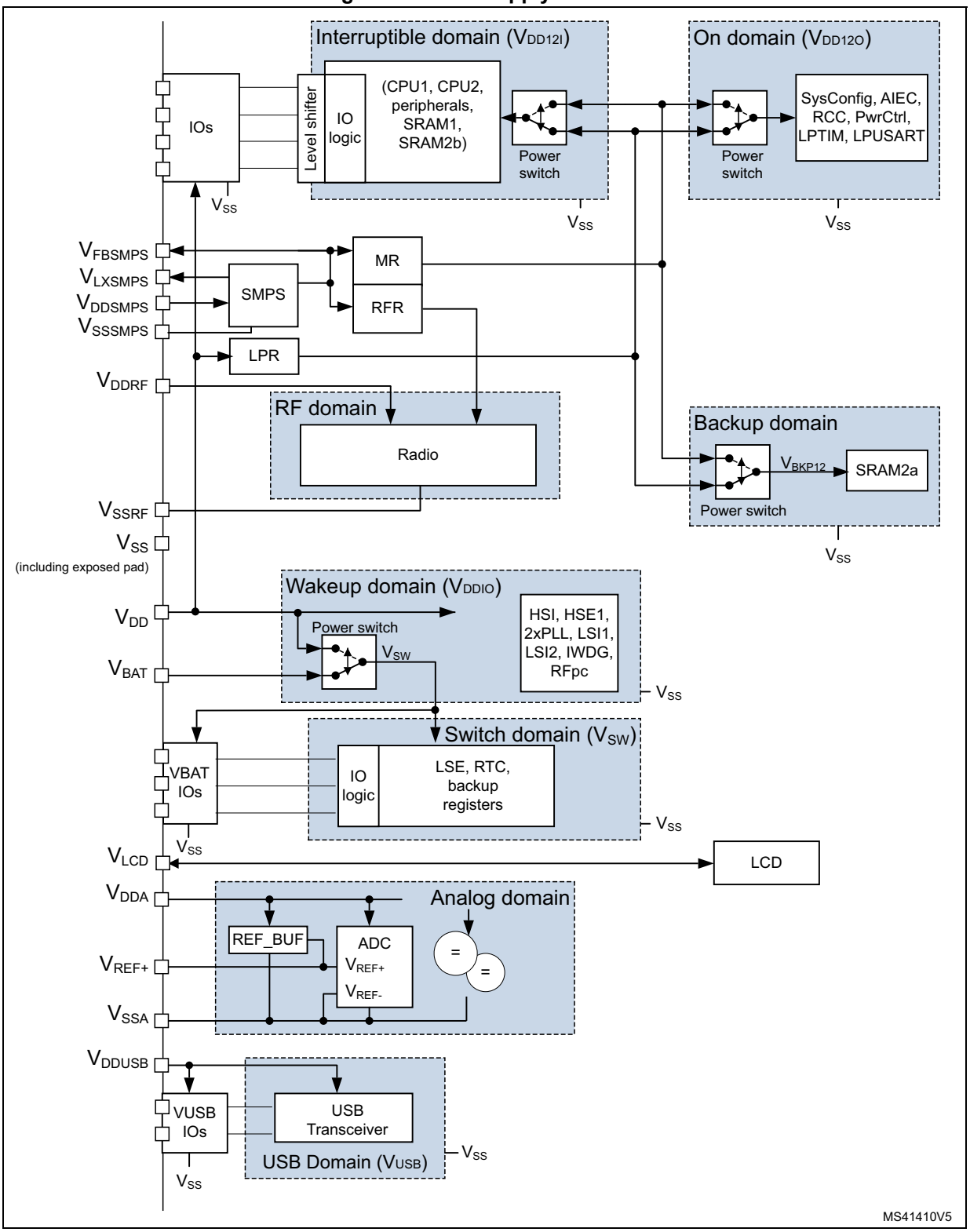
The STM32WB microcontrollers include a built-in SMPS to convert V_{DD} to a lowest voltage used by both the RF transceiver and the digital. This SMPS voltage (V_{FBSMPS}) is programmable, to adapt to the desired performance of both the RF Transmitter and the digital logic requirements.

An embedded linear voltage regulator is used to supply the internal digital power V_{CORE}, the power supply for digital peripherals and memories. Thanks to the internal voltage regulator and voltage scaling, the power consumption in active modes is kept at a minimum, whatever the supply voltage.

Note: Not all supply pins are present on all packages, refer to the datasheet for details.

Note: When using independent voltage sources for V_{DDA}, V_{DDUSB}, V_{DDLCD} and V_{DDRF}, the power-on and power-off supply sequence must be compliant with the constraints specified in each device datasheet.

Figure 6. Power supply overview



2.2.1 SMPS

The STM32WB feature a Switched Mode Power Supply (SMPS) to improve power performance when the supply voltage if high. This SMPS supplies all the logic and RF power stages. The SMPS is designed so that the RF sensitivity performance is not degraded, by using the same clock as the RF.

In order not to waste energy when commuting from Run to Low power states, the SMPS implements an Open mode that maintains the load into its output capacitance in Stop1/2 and Standby. This results in an improved wakeup time too.

The STM32WB also feature an automatic mechanism to disable the SMPS if the V_{DD} voltage drops below a given level, programmable using BORH detector. In that case, the application needs to restart the SMPS if the V_{DD} voltage increases again.

This SMPS can be switched ON/OFF on the fly, for examples if some analog task (e.g. an ADC acquisition) requires a very clean and stable supply.

The SMPS output voltage V_{FBSMPS} is monitored and a Reset is automatically generated if the voltage drops below a level that does not allow the digital section to work properly over the whole voltage and temperature range.

2.3 Ultra-safe supply monitoring

The STM32WB microcontrollers include a sophisticated supply supervisor module with several programmable options. This module is active during both power-on/down and run-time phases.

The power-up is a critical phase where the various parts of the internal circuitry must be sequentially started and critical parameters (such as factory trimming values or options) retrieved from the non-volatile memory to perform MCU initialization, even before the user reset phase. It is also during this period that V_{DD} can be altered with glitches coming from the battery insertion or because of a weak power source.

The ultra-safe BOR circuitry guarantees that the reset is released only if the V_{DD} is above the selected threshold, whatever the slope of the V_{DD} ramp-up phase, so that the circuit is within its guaranteed operating conditions when the program execution starts. A reset is generated when V_{DD} falls down below the selected threshold. Five thresholds can be selected depending on the value stored in Flash memory option byte. The BOR minimum threshold is 1.71 V, guaranteeing that the device exits reset above 1.71 V, enabling to supply the MCU with 1.8 V $\pm$5%.

The BOR is enabled in all modes except Shutdown mode. In Shutdown mode the power monitoring is disabled, as a consequence the switch to V_{BAT} domain when V_{DD} is not present (and vice-versa) is not supported in Shutdown mode.

The SMPS output voltage is monitored, to guarantee that the device has a proper voltage to sustain operation. If the V_{FBSMPS} falls below 1.2 V, in operating mode (except than SHUTDOWN, STANDBY and STOP2) a HW reset will be generated.

In addition, a 7-level programmable voltage detector (PVD) is available to generate an early interrupt in case of a voltage drop.

Finally, the independent power supplies (V_{DDA} and V_{DDUSB}) can be monitored by comparison with a fixed voltage threshold, and generate an interrupt in case power is below the threshold.

The PVD and PVM can wakeup from Stop modes.

2.4 A set of peripherals tailored for low power

Some peripherals require special attention, either because of their intrinsic high consumption, or because they are always powered up.

- The STM32WB include an RF subsystem that automatically interfaces with the power modes selection. At predefined times, driven by the LSI2 or LSE low power oscillator, the RF-sub-system wakes up the device to perform RF link operation. Once completed it automatically goes back to the previous low power mode.
- The STM32WB embed a multiple 12-bit / 4.26 Msps ADC. This very fast and accurate converter can jeopardize the battery lifetime if left powered-up. As the ADC consumption is roughly proportional to the acquisition frequency (around 200 µA / Msps), from consumption standpoint the application can choose between two solutions, i.e. either performing the acquisition at low speed to limit maximum current, or doing it at maximum speed to switch in ultra-low power mode quickly.

  When the acquisition is performed slowly, the ADC consumption itself can go down to few tens of µA drastically limiting the maximum current. This can be mandatory when the power source provides a limited current. The drawback, if the CPU has no other task to perform during that time, can be the increased time spent in run or sleep mode (or Low Power run or Low power sleep modes) versus the time spent in ultra-low power mode (Stop or Standby).

Several peripherals have been developed to operate even in Stop mode, when the system clock is stopped, with the main oscillator and memory powered down.

- A pair of ultra-low power comparators is available to monitor analog voltages with a current down to 350 nA. These comparators can wake up the STM32WB as soon as the external voltage reaches the selected threshold and they can be combined together to provide a window comparator. One of these comparators has a rail-to-rail input capability and its output can be redirected to a timer for a general purpose use.
- An RTC peripheral provides a clock/calendar with two alarms, includes a periodic wake-up unit and several application specific functions (such as timestamp, tamper detection). It can remain enabled in the lowest power mode (shutdown), when most of the chip is powered down, and wake up the full MCU circuitry in case of an alarm or tamper detection, for instance. It also contains up to 80 bytes of backup registers to store contextual information when exiting from standby mode, or to store sensitive information as they are protected by tampers detection, and readout memory protection. This peripheral has been designed using asynchronous design techniques to minimize its consumption.

  The RTC can be clocked by two low-power low-speed clocks:
  - LSE: the external 32.768 kHz quartz oscillator supports four power consumption modes, combined with drive capability;
  - LSI1: when deep accuracy is not required, the RTC can be clocked by an internal 32 kHz oscillator, with extremely low consumption.
- The glass LCD is one of the most common displays in low power applications, because of its inherently low current consumption, low price and customizing easiness. The STM32WB microcontrollers include a versatile LCD controller, which can drive displays with up to 8 common lines and 40 segments (or 4 lines, 44 segments), with the capability of selecting individually the I/O ports assigned to the LCD for an optimal use of the chip alternate functions. It also controls an optional internal step-up converter to

maintain the LCD contrast on a wide range of V_{DD} values with consumptions as low as 5 µA (LCD consumption not included).

- The Low power timer (LPTIM) is a 16-bit timer that benefits from the ultimate developments in power consumption reduction. Thanks to its diversity of clock sources, the LPTIM is able to keep running whatever the selected power mode. Given its capability to run even with no internal clock source, the LPTIM can be used as “Pulse Counter” which can be useful in some applications. Also, the LPTIM capability to wake up the system from low power modes, makes it suitable to make “Time-out functions” with extremely low power consumption. The LPTIM introduces a flexible clock scheme that provides the needed functionality and performance, while minimizing the power consumption.
- The low power universal asynchronous receiver transmitter (LPUART) is an UART which allows bidirectional UART communications with a limited power consumption. Only 32.768 kHz LSE clock is required to allow UART communications up to 9600 bauds. Higher baud rates can be reached when the LPUART is clocked by clock sources different from the LSE clock. Even when the MCU is in Stop modes, the LPUART can wait for an incoming UART frame while having an extremely low energy consumption.

  Several sources of wakeup from Stop mode can be selected:
  - wakeup on address match
  - wakeup on Start bit detection
  - wakeup on received byte.
- The I2C is able to wakeup the MCU from Stop modes (APB clock is off), when it is addressed. All addressing modes are supported. The HSI oscillator must be selected as the clock source for I2CCLK in order to allow wakeup from Stop. During Stop mode, the HSI is switched off. When a START is detected, the I2C interface switches the HSI on, and stretches SCL low until HSI is woken up. HSI is then used for the address reception. In case of an address match, the I2C stretches SCL low during MCU wakeup time. The stretch is released when ADDR flag is cleared by software, and the transfer goes on normally. If the address does not match, the HSI is switched off again and the MCU is not woken up.
- The USART is able to wakeup the MCU from Stop0/1 mode when USART clock is HSI or LSE. Several sources of wakeup from Stop0/1 mode can be selected:
  - wakeup on address match
  - wakeup on Start bit detection
  - wakeup on received byte.
- The USB can wakeup from Stop0/1 mode with these events:
  - Resume from Suspend
  - Attach detection protocol event

Table 4 summarizes the peripheral features over all available modes. Wakeup capability is detailed in gray cells.

Table 4. Features over all modes[1]

Peripheral	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
						-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU1	Y		-	Y	-	-	-	-	-	-	-	-	-	-
CPU2	Y		-	Y	-	-	-	-	-	-	-	-	-	-
Bluetooth Low Energy, 802.15.4	Y	Y[2]	Y	-	-	Y	Y	Y	Y	Y[3]	Y[3]	-	-	-
Flash memory (up to 1 MB)	O[4] [5]		O[4]	O[4]	O[4]	R	-	R	-	R	-	R	-	R
SRAM1 (up to 192 KB)	Y		Y[6]	Y	Y[6]	R	-	R	-	-	-	-	-	-
SRAM2a (32 KB)	Y		Y[6]	Y	Y[6]	R	-	R	-	O[7]	-	-	-	-
SRAM2b (32 KB)	Y		Y[6]	Y	Y[6]	R	-	R	-	-	-	-	-	-
Quad-SPI	O		O	O	O	-	-	-	-	-	-	-	-	-
Backup Registers	Y		Y	Y	Y	R	-	R	-	R	-	R	-	R
Brown-out reset (BOR)	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Brown-out SMPS for Bypass (BORH)	O		O	O	O	O	O[8]	-	-	-	-	-	-	-
Programmable Voltage Detector (PVD)	O		O	O	O	O	O	O	O	-	-	-	-	-
Peripheral Voltage Monitor PVMx (x=1, 2)	O		O	O	O	O	O	O	O	-	-	-	-	-
SMPS	O		O	O	O	O[9]	-	-	-	-	-	-	-	-
DMA	O		O	O	O	-	-	-	-	-	-	-	-	-
High Speed Internal (HSI16)	O		O	O	O	(10)	-	(10)	-	-	-	-	-	-
High Speed External (HSE)[11]	O		O	O	O	-	-	-	-	-	-	-	-	-
Low Speed Internal (LSI1 or LSI2)	O		O	O	O	O	-	O	-	O	-	-	-	-
Low Speed External (LSE)	O		O	O	O	O	-	O	-	O	-	O	-	O
Multi-Speed Internal (MSI)[12]	48	24	O	48	O	-	-	-	-	-	-	-	-	-
PLLx VCO maximum frequency	344	128	O	-	-	-	-	-	-	-	-	-	-	-
Clock Security System (CSS)	O		O	O	O	O	O[13]	O	O[13]	-	-	-	-	-
Clock Security System on LSE	O		O	O	O	O	O	O	O	O	O	-	-	-

Table 4. Features over all modes(1) (continued)

Peripheral	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
						-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
RTC / Auto wakeup	O		O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC Tamper pins	3		3	3	3	3	O	3	O	3	O	3	O	3
LCD	O		O	O	O	O	O	O	O	-	-	-	-	-
USB FS	O	-	O	-	-	-	O	-	-	-	-	-	-	-
USART1	O		O	O	O	O(14)	O(14)	-	-	-	-	-	-	-
Low-power UART (LPUART1)	O		O	O	O	O(14)	O(14)	O(14)	O(14)	-	-	-	-	-
I2C1	O		O	O	O	O(15)	O(15)	-	-	-	-	-	-	-
I2C3	O		O	O	O	O(15)	O(15)	O(15)	O(15)	-	-	-	-	-
SPIx (x=1, 2)	O		O	O	O	-	-	-	-	-	-	-	-	-
SAI1	O		O	O	O	-	-	-	-	-	-	-	-	-
ADC1	O		O	O	O	-	-	-	-	-	-	-	-	-
VREFBUF	O		O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1, 2)	O		O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O		O	O	O	-	-	-	-	-	-	-	-	-
Timers TIMx (x=1, 2, 16, 17)	O		O	O	O	-	-	-	-	-	-	-	-	-
Low-power Timer 1 (LPTIM1)	O		O	O	O	O	O	O	O	-	-	-	-	-
Low-power Timer 2 (LPTIM2)	O		O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O		O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O		O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O		O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O		O	O	O	-	-	-	-	-	-	-	-	-
True random number generator (True RNG)	O	-	O	-	-	-	-	-	-	-	-	-	-	-
AESx (x=1, 2) hardware accelerator	O		O	O	O	-	-	-	-	-	-	-	-	-

Table 4. Features over all modes(1) (continued)

Peripheral	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
						-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
PKA	O		O	O	O	-	-	-	-	-	-	-	-	-
CRC calculation unit	O		O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O		O	O	O	O	O	O	O	(16)	5 pins	(17)	5 pins	-

1. Legend: Y = Yes (Enabled). O = Optional (Disabled by default, can be enabled by software), R = Data retained, - = Not available.
2. BLE not possible in this mode.
3. Standby with SRAM2a Retention mode only.
4. The Flash memory can be configured in Power-down mode. By default, it is not in Power-down mode.
5. Flash memory programming only possible in Range 1 voltage, not in Range 2 and not in Low Power mode.
6. The SRAM clock can be gated on or off.
7. SRAM2a content is preserved when the bit RRS is set in PWR_CR3 register.
8. Only in STOP0 if SMPS is enabled.
9. Stop 0 only. SMPS is automatically switched to Bypass or Open mode during Low power operation.
10. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
11. The HSE can be used by the RF subsystem according with the need to perform RF operation (Tx or Rx).
12. MSI maximum frequency.
13. In case RF will be used and HSE will fail.
14. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
15. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
16. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
17. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

2.5 A versatile clock management

A reset and clock controller (RCC) peripheral manages the seven possible clock sources of the STM32WB microcontrollers.

Two external oscillators can be used for applications requiring high precision:

- The HSE clock (32 MHz high speed external clock), mandatory for RF operation, typically used to feed the PLL and to generate a CPU clock frequency of up to 64 MHz, and independent required frequencies for the USB controller and the audio clocks.
- The LSE (typically 32.768 kHz low speed external clock) normally used to provide a low power clock source to the real time clock (RTC), the RF sub-system and can also be used as LCD clock.

Five internal oscillators can be selected for various tasks:

- The LSI1 clock (32 kHz low speed internal clock) is a ultra-low power source that can feed the real time clock (with a limited accuracy), the LCD controller and the independent watchdog
- The LSI2 can be used as replacement for the LSE for RF framing, in low constraints applications. This oscillator has inaccurate frequency but very low jitter characteristics, suitable for RF protocols.
- The HSI clock (16 MHz high speed internal clock) is a high speed voltage-compensated oscillator.
- The MSI clock (100 kHz to 48 MHz multi speed internal clock) is an oscillator with adjustable frequency and low current consumption. It is designed to operate with a current proportional to the frequency, so as to minimize the internal oscillator consumption overhead for the low CPU frequencies. This oscillator can provide high-accuracy when configured in PLL-mode, where it is auto-calibrated using the LSE.
- The RC48, when available, with clock recovery system (HSI48): the internal 48 MHz clock source (HSI48) can be used to drive the USB or the True RNG peripheral. This clock can be output on the MCO.

Table 5 summarizes the characteristics and uses of the various oscillators.

Table 5. STM32WB clock source characteristics(1)

Clock source	Use	Frequency	Consumption (typical)	Accuracy	Trimming	
					Factory	User
HSE	Master clock for RF, CPUs, LCD and RTC	32.000 MHz	260 µA	Crystal dependent, down to few ppm	NA	Yes (option)
LSE	RTC and LCD USART, LPUART, LPTIM independent clock	32.768 kHz(typical)	250 nA	Crystal dependent, down to a few ppm	Not applicable	
HSI	Master clock Peripheral independent clock	16 MHz	150 µA	± 0.8 % typical over -10 to +85 °C +0.1 / -0.2 % typical over 1.62 to 3.6 V	Yes	Yes

Table 5. STM32WB clock source characteristics[1] (continued)

Clock source	Use	Frequency	Consumption (typical)	Accuracy	Trimming	
					Factory	User
MSI	Master clock	100 kHz 200 kHz 400 kHz 800 kHz 1 MHz 2 MHz 4 MHz 8 MHz 16 MHz 24 MHz 32 MHz[2] 48 MHz[2]	0.6 µA 0.8 µA 1.2 µA 1.9 µA 4.7 µA 6.5 µA 11 µA 18.5 µA 62 µA 85 µA 110 µA 155 µA	Default mode: +1.5/-1 % typical over -10 to +85 °C +1.5/-5.5 % typical for 16 to 48 MHz over 1.62 to 3.6 V PLL-mode: better than 0.25 %	Yes	Yes
LSI1	RTC, LCD and IWDG	32 kHz	110 nA	±1.5 % typical over -40 to +125 °C +0.5/-1.5 % typical over 1.62 to 3.6 V	Yes	No
LSI2	RF	~32 kHz	200 nA	Low jitter	Yes	No
HSI48	USB, RNG	48 MHz	380 nA	±3 % max over 15 to 85 °C V_{dd} 3.0 to 3.6 V ±4.5 % max over -40 to +125 °C V_{dd} 1.65 to 3.6 V	Yes	USB PLL

1. Preliminary characteristics, for information only. See product datasheet for detailed electrical characteristics.
2. Only possible in Range 1.

In addition, the STM32WB microcontrollers embed two PLLs, each of them provides up to three independent outputs and can be fed by the HSI, the HSE or the MSI. The six outputs can be configured independently for:

- the system clock
- the ADC interface clock
- the USB, True RNG clock
- the Serial Audio Interface SAI1 clock

This removes the peripheral constraints on the system clock. Many other peripherals can be clocked independently from the system clock: USART, LPUART, I2Cx (x=1, 3) and LPTIMx (x=1, 2) receive an independent clock. This makes it possible, as an example, to reduce the system and APB bus frequencies and keep the communication peripheral baud rate constant, independent from the system clock frequency.

All peripherals clock can be individually enable or disable in Run and Low-power run modes.

The peripheral clocks can also be individually enable or disable in Sleep and Low-power sleep modes.

Although HSI and MSI are factory trimmed, they can be further trimmed by 0.5% steps during run time to compensate for frequency deviations due to temperature and voltage changes.

When LSE is present in the application, the MSI can be automatically calibrated using the LSE (PLL-mode configuration), making it possible to reach long-term LSE accuracy. This mode can provide the USB clock, with the accuracy required to operate in device mode.

Moreover the system clock when the MCU exits from Stop modes can be configured to be either HSI or MSI at any frequency range. This enables to exit from Stop mode directly at 48 MHz, without waiting for a PLL starting time.

3 Conclusion

The main features of the STM32WB devices presented in this application note demonstrate the benefits offered by this microcontroller family in reducing the current consumption in embedded communication systems.

Besides having the same characteristics of the STM32L4 ultra-low power Series, the STM32WB microcontrollers offer high processing performance without compromising the power consumption. They complement the STM32 portfolio, keeping compatibility with other STM32 devices.

The STM32WB rich set of peripherals, associated with the RF proprietary low power subsystem allows the user to cover a wide range of applications, while the available low power modes give full flexibility to adjust on-the-fly the consumption for any task.

This results is an extended operating lifetime for today and tomorrow always greener applications.

4 Revision history

Table 6. Document revision history

Date	Revision	Changes
14-Sep-2018	1	Initial release.
21-Feb-2019	2	Changed document classification, from ST restricted to Public.