Introduction

The STM32WB Series microcontrollers are built using an innovative architecture to reach best-in-class, ultra-low-power consumption with their high flexibility, powerful radio and advanced set of peripherals. They can operate up to 64 MHz and achieve 80 DMIPS performances at 64 MHz, thanks to the integration of the ART Accelerator with the lowest possible dynamic power consumption.

The STM32WB Series microcontrollers include a proprietary low-power RF subsystem, with its own dedicated Arm® Cortex®-M0+ to offload all the real-time RF communication tasks from the Cortex®-M4, resulting in best power efficiency distribution between the user and the communication tasks.

The STM32WB Series microcontrollers feature the FlexPowerControl, which increases flexibility in the power modes management while at the same time reducing the overall application consumption.

The STM32WB Series microcontrollers embed a large number of smart and high performance peripherals, a large set of advanced and low-power analog features, and several peripherals tuned for Low-power modes. By using the batch acquisition sub-mode (BAM), they optimize the power consumption when data is transferred using the communication peripherals, while the rest of the device is kept in Low-power mode.

Based on the solid foundations of the STM32L4 Series, already embedding several power efficient innovations minimizing the power consumption in the different modes while maintaining most of the existing peripherals, the STM32WB Series microcontrollers enable an easy migration from a dual chip solution (STM32L4 + Bluetooth Low Energy / 802.15.4) to that of a single chip, with almost the same power budget.

The STM32WB Series microcontrollers (except the STM32WBx0) include an embedded SMPS that further improves the power consumption figures in applications where the supply voltage is high, as well as the overall consumption.

Thanks to their built-in internal voltage regulator and voltage scaling (except the STM32WBx0), device consumption in active modes is kept at a minimum, whatever the external supply voltage. This makes these devices particularly suited for handheld battery-powered products, down to 1.71 V (2 V for the STM32WBx0). In addition, their multi-voltage domains (except the STM32WBx0) supplies the product at low voltage (further reducing consumption) while the analog-to-digital converters operate with a higher supply and reference voltage, up to 3.6 V.

STM32WB Series microcontrollers support a battery backup domain to keep the RTC running, and a set of 20 32-bit wide, registers, that can be retained in case of power loss. This optional backup battery can be charged when the main supply is present.

The STM32WB Series microcontrollers support many Low-power modes, each of them with several submode options. This allows the designer to achieve the best compromise between low-power consumption figures, shorter startup time, available set of peripherals and maximum number of wake-up sources.
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1 Energy-efficient processing

STM32WB Series microcontrollers are based on an Arm®(a) Cortex®-M4 with FPU and DSP instruction set.

The high processing performance in Run mode (expressed in DMIPS/MHz) is achieved thanks to the use of a Cortex®-M4 core associated with its memory interfaces. To ensure full operating performance up to 64 MHz, STM32WB Series microcontrollers embed the ART Accelerator, which masks the Flash memory access wait state, and makes it possible to achieve 1.25 DMIPS/MHz, whatever the system clock frequency.

The high energy efficiency, expressed as mA/DMIPS, is obtained by dynamically adapting the internal supply voltage to the operating frequency. This method is called “undervolting”.

STM32WB Series microcontrollers offer two dynamically selectable voltages and frequency ranges:
1. Range 1 for a system frequency up to 64 MHz
2. Range 2 for a system frequency up to 16 MHz with improved efficiency (up to 15% higher than Range 1).
   Range 2 is not supported by the STM32WBx0.

When the RF is not used, a dedicated Low-power run mode (LPRun) allows the core to operate at frequencies inferior or equal to 2 MHz, with improved efficiency, up to 20% higher compared to Range 2. Note that in this case the RF cannot be used, as it requires at least 32 MHz to operate.

Figure 1 shows the typical current consumption of the STM32WB55, as a function of system frequency, for different run modes.

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a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
Figure 1. Current consumption versus Cortex®-M4 system frequency (25 °C)
Figure 2 shows the power distribution from the internal LDO regulator in the different Run modes.

Figure 2. Power distribution architecture

STM32WB Series microcontrollers allow the CPU1 Cortex®-M4 to execute code either from the internal Flash memory, the SRAM1 and SRAM2, or from the external Quad-SPI.

Running from internal SRAM, consumes the least current. When running from the internal Flash memory, the ART Accelerator reduces the number of memory accesses thus reducing the overall current consumption. Note that when the RF subsystem is in use, the ART Accelerator cannot be disabled, as the Cortex®-M0+ and the Cortex®-M4 share the same Flash memory.

Figure 3 shows the consumption of the STM32WB55 for two main memory configurations:
- Execution from the internal Flash memory, ART Accelerator enabled
- Execution from the internal SRAM1, Flash memory disabled.
The location of the executable code and data within the memory system impacts not only the current consumption but also the overall computation performance. As an example, Table 1 details the overall performances measured on a STM32WB55 with the system clock running at 64 MHz, executing a complex algorithm, such as CoreMark® from EEMBC® organization.

Table 1. STM32WB55 performance with system clock at 64 MHz

<table>
<thead>
<tr>
<th>Configuration</th>
<th>mA/MHz</th>
<th>CoreMark® per MHz</th>
<th>CoreMark® per mA</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLASH ART On</td>
<td>0.125</td>
<td>3.25</td>
<td>26</td>
<td>Cache On, Prefetch buffer Off</td>
</tr>
<tr>
<td>SRAM1</td>
<td>0.117</td>
<td>2.40</td>
<td>20</td>
<td>Code and Data in SRAM1</td>
</tr>
</tbody>
</table>

The ART Accelerator allows the Cortex®-M4 core to run almost at the maximum efficiency as defined in the figures published by Arm®. Table 2 gives the impact of the SMPS on the same figures.

Table 2. STM32WB55 performance with SMPS

<table>
<thead>
<tr>
<th>Configuration</th>
<th>mA/MHz</th>
<th>CoreMark® per MHz</th>
<th>CoreMark® per mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLASH ART On</td>
<td>0.077</td>
<td>3.25</td>
<td>42</td>
</tr>
<tr>
<td>SRAM1</td>
<td>0.073</td>
<td>2.40</td>
<td>33</td>
</tr>
</tbody>
</table>

Selection of the SMPS, when possible, improves the efficiency (CoreMark® per mA) by almost 40%.
Figure 4 shows the STM32WB Series microcontrollers’ Flash memory latency (number of wait states to be programmed in the Flash memory access control register), depending on regulator voltage scaling range and system clock frequency.

Figure 4. STM32WB Series microcontrollers’ Flash memory latency versus V\textsubscript{CORE} range

Note:
- Range 2 is not supported by the STM32WBx0
- VDD between 2 V and 3.6 V for STM32WBx0
2 FlexPowerControl description

FlexPowerControl reduces the application power consumption thanks to high flexibility in the power management, smart peripherals and architecture.

The STM32WB Series microcontrollers feature an independent power management state by the RF sub-system and the Cortex®-M4 application CPU. A dedicated hardware mechanism selects the lowest possible power consumption state.

2.1 Available low-power modes

The STM32WB Series microcontrollers implement many different power modes, seven of them are low-power.

On top of these modes, the power consumption can be modulated by selecting different clock sources and frequencies, as well as clocking off peripherals not in use.

In all these modes, except Shutdown, the safe power monitoring brown out reset (BOR) and the IWDG can stay active to guarantee safe execution.

Table 3 summarizes the features available for each mode and provides an indication of the current consumption, while Figure 5 shows the possible transitions between low-power modes.

2.1.1 Low-power run and Low-power sleep modes

When the RF sub-system is not in use and when the application CPU can run below 2 MHz, the low-power run mode and low-power sleep mode result in the best power performance.

They offer Run and Sleep mode functionality for applications with extremely low current consumption where some peripherals cannot be switched off, or where the CPU is processing continuously at low speed to minimize current variations.

Several features are implemented to reduce the current consumption:

- The core logic is supplied by the low-power voltage regulator to reduce the quiescent current;
- The Flash memory can be switched off (power-down mode and clock gating) in Low-power sleep mode. It can also be switched off in Low-power run when the application processor is executing from SRAM1;
- The system clock is limited to 2 MHz. The MSI internal RC oscillator can be selected as it supports several frequency ranges, with a small MCU total consumption as low as 48 µA in Low-power sleep Flash memory off at 100 kHz.

Batch acquisition sub-mode (BAM)

The STM32WB Series microcontrollers support the power efficient batch acquisition sub-mode (BAM), in which data are transferred using communication peripherals, while the rest of the device is in Low-power mode.

This is achieved by entering Sleep or Low-power sleep mode with this configuration:

- Only the DMA, the communication peripheral(s) and the SRAM1 or SRAM2 clocks are enabled in Sleep (or Low-power sleep) mode;
If the RF sub-system is not in use and system clock can be limited to 2 MHz and the main regulator is switched off (to enter Low-power sleep). In this case the Flash memory can be powered off.

In Low-power sleep mode, the I2C and USART/LPUART peripherals can still be clocked with HSI at 16 MHz, making it possible to support BAM with I2C or USART at speeds up to 1 Mbps.

2.1.2 Stop mode

The STM32WB Series microcontrollers implement three Stop modes with full SRAM and peripheral retention capability and a capacity to wakeup in 1 µs by using the MSI running at a frequency up to 48 MHz.

In these Stop modes all the high speed oscillators (HSE, MSI, HSI) are stopped, while the active low speed oscillators (LSE and / or LSI) are kept active. The peripherals are set active using the HSI clock when needed, to wake the device up on a specific events (such as UART character reception or I²C address recognition).

2.1.3 Standby mode

In Standby mode the BOR is always enabled, ensuring that the device will reset if the supply voltage drops below the selected functional threshold.

Standby mode with RAM2a retention is the lowest mode allowing the use of the RF sub-system.

Individual pull-ups and pull-downs can be applied on each I/O during the Standby mode, preserving any external device configuration.

Wakeup from this mode is done by using one of the five wakeup pins, the reset pin or the independent watchdog. The RTC clocked by the low-speed oscillators (LSE or LSI) is also functional in this mode, with wakeup capability. Wakeup from this mode can also be performed by the Radio sub-system.

2.1.4 Shutdown mode

The Shutdown mode is implemented in the STM32WB Series microcontrollers to further lengthen the battery autonomy of battery-powered applications.

This mode provides the lowest power consumption, by switching off the internal voltage regulators and by disabling the voltage power monitoring. Wakeup from this mode is done with one of the five wakeup pins or the reset pin. The RTC clocked by the low-speed external oscillator (LSE) is also functional in this mode, with wakeup capability. Wakeup from shutdown is equivalent to a POR.

Note: In this mode the RF sub-system cannot be used as all the BLE and 802.15.4 link parameters will have been lost.
<table>
<thead>
<tr>
<th>Mode</th>
<th>Regulator</th>
<th>CPU1</th>
<th>Flash</th>
<th>SRAM</th>
<th>Clocks</th>
<th>DMA &amp; Peripherals</th>
<th>Wakeup source</th>
<th>Consumption</th>
<th>Wakeup time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Run</td>
<td>Range 1</td>
<td>ON</td>
<td>ON(2)</td>
<td>ON</td>
<td>Any</td>
<td>All</td>
<td>N/A</td>
<td>107 µA/MHz</td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td>Range 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>All except True RNG and USB-FS(3)</td>
<td>N/A</td>
<td>100 µA/MHz</td>
<td></td>
</tr>
<tr>
<td>LPRun</td>
<td>LPR</td>
<td>Yes</td>
<td>ON(5)</td>
<td>ON</td>
<td>Any</td>
<td>All except RF, True RNG and USB-FS</td>
<td>N/A</td>
<td>103 µA/MHz</td>
<td>19.5 µs</td>
</tr>
<tr>
<td>Sleep</td>
<td>Range 1</td>
<td>No</td>
<td>ON</td>
<td>ON(4)</td>
<td>Any</td>
<td>All</td>
<td>Any interrupt or event</td>
<td>41 µA/MHz</td>
<td>9 cycles</td>
</tr>
<tr>
<td></td>
<td>Range 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>All except True RNG and USB-FS(3)</td>
<td>Any interrupt or event</td>
<td>46 µA/MHz</td>
<td></td>
</tr>
<tr>
<td>LPSleep</td>
<td>LPR</td>
<td>No</td>
<td>ON(5)</td>
<td>ON(4)</td>
<td>Any</td>
<td>All except RF, True RNG and USB-FS</td>
<td>Any interrupt or event</td>
<td>45 µA/MHz</td>
<td>9 cycles</td>
</tr>
<tr>
<td>Stop 0</td>
<td>Range 1</td>
<td>No</td>
<td>OFF</td>
<td>ON</td>
<td></td>
<td>RF(3), BOR, PVD, PVM RTC, LCD, IWDG, COMPx (x=1, 2) USART1(8) LPUART1(6) I2Cx (x=1, 3)(9) LPTIMx (x=1, 2), SMPS All other peripherals are frozen.</td>
<td>Reset pin, all I/Os, RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB</td>
<td>100 µA</td>
<td>1.7 µs</td>
</tr>
<tr>
<td></td>
<td>Range 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>All other peripherals are frozen.</td>
<td>Reset pin, all I/Os, RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB</td>
<td>9.2 µA w/o RTC</td>
<td>4.7 µs</td>
</tr>
<tr>
<td>Stop 1</td>
<td>LPR</td>
<td>No</td>
<td>OFF</td>
<td>ON</td>
<td></td>
<td>RF, BOR, PVD, PVM RTC, LCD, IWDG, COMPx (x=1, 2) USART1(14) LPUART1(14) I2Cx (x=1, 3)(15) LPTIMx (x=1, 2) All other peripherals are frozen.</td>
<td>Reset pin, all I/Os, RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB</td>
<td>9.6 µA w RTC</td>
<td></td>
</tr>
</tbody>
</table>
### Table 3. STM32WB55 modes overview (continued)

<table>
<thead>
<tr>
<th>Mode</th>
<th>Regulator</th>
<th>CPU1</th>
<th>Flash</th>
<th>SRAM</th>
<th>Clocks</th>
<th>DMA &amp; Peripherals</th>
<th>Wakeup source</th>
<th>Consumption</th>
<th>Wakeup time (μs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stop 2</td>
<td>LPR</td>
<td>No</td>
<td>OFF</td>
<td>ON</td>
<td>LSE, LSI</td>
<td>RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1(^{14}) LPUART1(^{14}) I2C3(^9) LPTIM1</td>
<td>Reset pin, all I/Os RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) LPUART1 I2C3 LPTIM1</td>
<td>1.85 μA w/o RTC 2.1 μA w RTC</td>
<td>5.71 μs</td>
</tr>
<tr>
<td>Standby</td>
<td>LPR</td>
<td>No</td>
<td>OFF</td>
<td>SRAM2a ON(^{(10)})</td>
<td>LSE, LSI</td>
<td>RF, BOR, RTC, IWDG All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down</td>
<td>RF, Reset pin 5 I/Os (WKUPx)(^{(11)})</td>
<td>0.32 μA w/o RTC 0.6 μA w RTC</td>
<td>51 μs</td>
</tr>
<tr>
<td>Shutdown</td>
<td>OFF</td>
<td>No</td>
<td>OFF</td>
<td>OFF</td>
<td>LSE</td>
<td>RTC All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down(^{(12)})</td>
<td>Reset pin 5 I/Os (WKUPx)(^{(11)}) RTC</td>
<td>0.028 μA w/o RTC 0.315 μA w RTC</td>
<td>-</td>
</tr>
</tbody>
</table>

1. Add 12 μs (max 100 μs) when using SMPS, except Sleep, LPSleep and Stop 0 where the SMPS is not stopped.
2. Flash memory programming is only possible in Range 2 voltage.
3. The RF subsystem is unable to operate in BLE mode.
4. The SRAM1 and SRAM2 clocks can be independently gated.
5. The Flash memory controller can be placed in power-down mode if the RF subsystem is not in use and the whole program is run (LPrun mode) from the SRAM.
6. HSE (32 MHz) automatically used when RF activity is needed by the RF subsystem.
7. HSI16 (16 MHz) automatically used by some peripherals.
8. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, Address match or Received frame event.
9. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
10. SRAM1 and SRAM2b are OFF.
11. The I/Os with wakeup from Standby / Shutdown capability are: PA0, PC13, PC12, PA2, PC5.
12. I/Os can be configured with internal pull-up, pull-down or floating but the configuration is immediately lost when exiting the Shutdown mode.
Figure 5 describes the available power stated transitions. Grey cells represent the states in which the RF sub-system cannot be used.

![Figure 5. Low-power modes possible transitions](image)

### 2.2 Multi-supply and battery backup domain

The STM32WB Series microcontrollers require a $V_{DD}$ operating voltage supply between 1.71 V (2 V for STM32WBx0) to 3.6 V. $V_{DDSMPS}$, $V_{DD USB}$, $V_{DD LCD}$ and $V_{REF+}$ are not available for the STM32WBx0.

Independent supplies ($V_{DDA}$, $V_{DDUSB}$), can be provided for specific peripherals, thus removing the need to supply the whole system with high voltage when analog or USB functions are used. Supplying the MCU with low $V_{DD}$ voltage reduces the power consumption in the low-power modes. When the peripherals supplied by the independent power supplies are not used in the application, those supplies should be connected to $V_{DD}$.

- $V_{DD}$ and $V_{DDSMPS} = 1.71$ to $3.6$ V (2 V to 3.6 V for the STM32WBx0)
  - $V_{DD}$ is the external power supply for the I/Os, the RF sub-system, the internal regulator and the system analog functions such as reset, power management and internal clocks. It is provided externally through VDD pins.
  - $V_{DDRF} = 1.71$ to $3.6$ V (2 V to 3.6 V for the STM32WBx0)
    - Supplies the RF reference voltage

- $V_{DDA}$ minimum voltage (except STM32WBx0):
  - 1.62 V if ADC or COMPs are used;
  - 2.4 V if the built-in Reference source needs to be used for $V_{REF}$.

$V_{DDA}$ is the external analog power supply for A/D converters and comparators.

- $V_{DDA} = 2$ V to 3.6 V: external analog power supply for ADC (STM32WBx0)
- \( V_{DDUSB} = 3.0 \) to \( 3.6 \) V (if USB is used)
  \( V_{DDUSB} \) is the independent external power supply for USB transceivers.

In addition, the STM32WB Series microcontrollers support two voltage reference supplies:
- \( V_LCD = 2.5 \) to \( 3.6 \) V
  The voltage reference for the LCD \( (V_{LCD}) \) is used to control the contrast of the glass LCD. It can be provided either from an external supply voltage or by the embedded voltage step-up converter, independently of the \( V_{DD} \) voltage (up to \( 3.6 \) V if \( V_{DD} > 2.0 \) V). \( V_{LCD} \) is multiplexed with PC3 or with PB2, which can be used as GPIO when the LCD is not used.
- \( V_{REF+} \)
  \( V_{REF+} \) is the input reference voltage for the ADC. It is also the output of the internal reference voltage buffer when enabled. \( V_{REF+} \) pin, and thus internal reference voltage, is not available on all packages. When the \( V_{REF+} \) is double-bonded with \( V_{DDA} \) in a package, the internal reference voltage buffer is not available and must be kept disabled (refer to datasheet for packages pinout description).

To retain the content of the Backup registers and supply the RTC function when \( V_{DD} \) is turned off, the \( V_{BAT} \) pin can be connected to an optional backup voltage supplied by a battery or by another source:
- \( V_{BAT} = 1.55 \) to \( 3.6 \) V
  \( V_{BAT} \) is the power supply for the RTC, the external clock 32 kHz LSE oscillator and the backup registers (through power switch) when \( V_{DD} \) is not present. When \( V_{DD} \) is present these peripherals (RTC, LSE) are automatically supplied by \( V_{DD} \), and it is possible to charge the external battery on \( V_{BAT} \) through an internal resistance.

The STM32WB Series microcontrollers (except STM32WBx0) include a built-in SMPS to convert \( V_{DD} \) to the lowest voltage used by both the RF transceiver and the digital logic. This SMPS voltage \( (V_{FBSMPS}) \) is programmable, to adapt to the desired performance of both the RF Transmitter and the digital logic requirements.

An embedded linear voltage regulator is used to supply the internal digital power \( V_{CORE} \), the power supply for digital peripherals and memories. Thanks to the internal voltage regulator and voltage scaling, the power consumption in active modes is kept at a minimum, whatever the supply voltage.

**Note:** Not all supply pins are present on all packages, refer to the datasheet for details.

**Note:** When using independent voltage sources for \( V_{DDA}, V_{DDUSB}, V_{DDLCD} \) and \( V_{DDRF} \), the power-on and power-off supply sequence must be compliant with the constraints specified in each device datasheet.
Figure 6. STM32WB55 power supply overview
2.2.1 SMPS

The STM32WB Series microcontrollers feature a Switched Mode Power Supply (SMPS) to improve power performance at the high voltage (not included in STM32WBx0). This SMPS supplies all the logic and RF power stages. The SMPS is designed so that the RF sensitivity performance is not degraded by using the same clock as the RF.

In order not to waste energy when commuting from Run to Low-power states, the SMPS implements an Open mode that maintains the load on its output capacitance in Stop1/2 and Standby. This also results in an improved wakeup time.

The STM32WB Series microcontrollers also features an automatic mechanism to disable the SMPS if the \( V_{DD} \) voltage drops below a given level, programmable using the BORH detector. In that case, the application needs to restart the SMPS when the \( V_{DD} \) voltage increases again.

This SMPS can be switched ON/OFF on the fly, for examples if an analog task (such as an ADC acquisition) requires a very clean and stable supply.

The SMPS output voltage \( V_{FBSMPS} \) is monitored and a Reset is automatically generated if the voltage drops below a level that does not allow the digital section to operate correctly over the whole voltage and temperature range. (except in the STM32WBx0)

2.3 Ultra-safe supply monitoring

The STM32WB Series microcontrollers include a sophisticated supply supervisor module with several programmable options. This module is active during both power-on/down and run-time phases.

The power-up is a critical phase where the various parts of the internal circuitry must be sequentially started and critical parameters (such as factory trimming values or options) are retrieved from the non-volatile memory to perform MCU initialization, even before the user reset phase. It is also during this period that \( V_{DD} \) can be impacted by glitches coming from the battery insertion or due to a weak power source.

The ultra-safe BOR circuitry guarantees that the reset is released only if the \( V_{DD} \) is above the selected threshold, whatever the slope of the \( V_{DD} \) ramp-up phase, so that the circuit is within its guaranteed operating conditions when the program execution starts. A reset is generated when \( V_{DD} \) falls below the selected threshold. Five thresholds can be selected depending on the value stored in Flash memory option byte. The BOR minimum threshold is 1.71 V, guaranteeing that the device exits reset above 1.71 V, supplying 1.8 V \( \pm \) 5% to the MCU.

The BOR is enabled in all modes except Shutdown mode. In Shutdown mode, the power monitoring is disabled, as a consequence the switch to \( V_{BAT} \) domain when \( V_{DD} \) is not present (and vice-versa) is not supported.

The SMPS output voltage is monitored (except in the STM32WBx0), to guarantee that the device has a proper voltage to sustain operation. If the \( V_{FBSMPS} \) falls below 1.2 V, in operating mode (other than Shutdown, Standby and Stop2) a hardware reset will be generated.

In addition, a 7-level programmable voltage detector (PVD) is available to generate an early interrupt in case of a voltage drop.
Finally, the independent power supplies (\(V_{DDA}\) and \(V_{DDUSB}\)) can be monitored by comparing them with a fixed voltage threshold. An interrupt is generated when the voltage falls below the threshold (except STM32WBx0).

The PVD and PVM can wakeup from Stop modes.

2.4 A set of peripherals tailored for low-power

Some peripherals require special attention, either because of their intrinsic high consumption, or because they are always powered up.

- The STM32WB Series microcontrollers include an RF subsystem that automatically interfaces with the power mode selection. At predefined times, driven by the LSI2 or LSE low-power oscillator, the RF-sub-system wakes the device up to perform an RF link operation. Once completed it automatically goes back to the previous low-power mode.

- The STM32WB Series microcontrollers embed a multiple 12-bit / 4.26 Msps (2.13 Msps for STM32WBx0) ADC. This very fast and accurate converter can jeopardize the battery lifetime if left powered-up. As the ADC consumption is roughly proportional to the acquisition frequency (around 200 \(\mu\)A / Msps), from consumption standpoint the application can choose between two solutions, i.e. either performing the acquisition at low speed to limit maximum current, or doing it at maximum speed to switch back to ultra-low-power mode quickly.

When the acquisition is performed slowly, the ADC consumption itself can go down to few tens of a \(\mu\)A drastically, limiting the maximum current. This is be mandatory when the power source provides a limited current. The drawback, if the CPU has no other task to perform during that time, it will increase the increased time the system spends in run or sleep mode (or Low-power run or Low-power sleep modes) versus the time spent in ultra-low-power mode (Stop or Standby).

Several peripherals have been developed to operate even in Stop mode, when the system clock is stopped, with the main oscillator and memory powered down.

- A pair of ultra-low-power comparators are available (except in the STM32WBx0) to monitor analog voltages with a current as low as 350 nA. These comparators can wake the STM32WB Series microcontrollers up as soon as the external voltage reaches the selected threshold and they can be combined together to provide a window comparator. One of these comparators has a rail-to-rail input capability and its output can be redirected to a timer for a general purpose use.

- An RTC peripheral provides a clock / calendar with two alarms, includes a periodic wake-up unit and several application specific functions (such as timestamp and tamper detection). It can remain enabled in the lowest power mode (shutdown), when most of the chip is powered down, and wake up the full MCU circuitry in case of an event such as an alarm or tamper detection, for instance. It also contains up to 80 bytes of backup registers to store contextual information when exiting from standby mode, or to store sensitive information as they are protected by tamper detection mechanism, and readout memory protection. This peripheral has been designed using asynchronous design techniques to minimize its consumption.

The RTC can be clocked by two low-power low-speed clocks:

- LSE: the external 32.768 kHz quartz oscillator supports four power consumption modes, combined with drive capability;
- LSI1: when high accuracy is not required, the RTC can be clocked by an internal 32 kHz oscillator, with extremely low consumption.

- The glass LCD is one of the most common displays in low-power applications, because of its inherently low current consumption, low price and simple customization. The STM32WB Series microcontrollers (except for the STM32WBx0) include a versatile LCD controller, which can drive displays with up to 8 common lines and 40 segments (or 4 lines, 44 segments), with the capability of individually selecting the I/O ports assigned to the LCD for an optimal use of the chip alternate functions. It also controls an optional internal step-up converter to maintain the LCD contrast on a wide range of $V_{DD}$ values with a current as low as 5 µA (LCD consumption not included).

- The low-power timer (LPTIM) is a 16-bit timer that benefits from the ultimate developments in power consumption reduction. With its clock source diversity, the LPTIM is able to keep running whatever the selected power mode. Given its capability to run even with no internal clock source, the LPTIM can be used as "Pulse Counter" which can be useful in some applications. Also, the LPTIM capability to wake up the system from low-power modes, makes it suitable with extremely low-power consumption "Time-out functions". The LPTIM introduces a flexible clock scheme that provides the required functionality and performance, while minimizing the power consumption.

- The low-power universal asynchronous receiver transmitter (LPUART) available in the STM32WB Series microcontrollers (except in the STM32WBx0) is a UART which allows bidirectional UART communications with a limited power consumption. Only 32.768 kHz LSE clock is required to allow UART communications up to 9600 bauds. Higher baud rates can be reached when the LPUART is clocked by sources other than from the LSE clock. Even when the MCU is in Stop mode, the LPUART can wait for an incoming UART frame while having an extremely low energy consumption.

Several sources of wakeup from Stop mode can be selected:
- wakeup on address match
- wakeup on Start bit detection
- wakeup on received byte.

- The $I^2C$ is able to wakeup the MCU from Stop modes (APB clock is off), when it is addressed. All addressing modes are supported. The HSI oscillator must be selected as the clock source for $I^2C$CLK in order to allow wakeup from Stop. During Stop mode, the HSI is switched off. When a START is detected, the $I^2C$ interface switches the HSI on, and stretches SCL low until HSI is woken up. HSI is then used for the address reception. In case of an address match, the $I^2C$ stretches SCL low during MCU wakeup time. The stretch is released when ADDR flag is cleared by software, and the transfer goes on normally. If the address does not match, the HSI is switched off again and the MCU is not woken up.

- The USART is able to wakeup the MCU from Stop0/1 mode when USART clock is HSI or LSE. Several sources of wakeup from Stop0/1 mode can be selected:
  - wakeup on address match
  - wakeup on Start bit detection
  - wakeup on received byte.

- The USB can wakeup from Stop0/1 mode with these events (not available in the STM32WBx0):
  - Resume from Suspend
  - Attach detection protocol event
Table 4 summarizes all the available peripheral feature modes. Wakeup capability is detailed in the gray cells.
### Table 4. STM32WB55 features over all modes(1)

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Run Range 1</th>
<th>Run Range 2</th>
<th>Sleep</th>
<th>Low-power run</th>
<th>Stop0/Stop1</th>
<th>Stop 2</th>
<th>Standby</th>
<th>Shutdown</th>
<th>Wakeup capability</th>
<th>Wakeup capability</th>
<th>Wakeup capability</th>
<th>Wakeup capability</th>
<th>VBAT</th>
</tr>
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<tbody>
<tr>
<td>CPU1</td>
<td>Y</td>
<td>-</td>
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<td>-</td>
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<td>-</td>
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<tr>
<td>CPU2</td>
<td>Y</td>
<td>-</td>
<td>Y</td>
<td>-</td>
<td>-</td>
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<td>-</td>
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</tr>
<tr>
<td>Bluetooth Low Energy, 802.15.4</td>
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<td>Y(2)</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y(3)</td>
<td>Y(3)</td>
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<tr>
<td>Flash memory (up to 1 MB)</td>
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<td>O(4)</td>
<td>O(4)</td>
<td>O(4)</td>
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<td>R</td>
<td>R</td>
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<tr>
<td>SRAM1 (up to 192 KB)</td>
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<td>Y(6)</td>
<td>Y</td>
<td>Y</td>
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<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
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<td>Y</td>
</tr>
<tr>
<td>SRAM2a (32 KB)</td>
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<td>Y(6)</td>
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<td>Y</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
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<tr>
<td>SRAM2b (32 KB)</td>
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<td>Y(6)</td>
<td>Y</td>
<td>Y</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
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<td>Quad-SPI</td>
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<tr>
<td>Backup Registers</td>
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<td>Y</td>
<td>Y</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
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<tr>
<td>Brown-out reset (BOR)</td>
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<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
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<td>Brown-out SMPS for Bypass (BORH)</td>
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<td>High Speed External (HSE)(11)</td>
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<td>Low Speed Internal (LSI1 or LSI2)</td>
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<td>O</td>
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<tr>
<td>Low Speed External (LSE)</td>
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<td>O</td>
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<tr>
<td>Multi-Speed Internal (MSI)(12)</td>
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<td>24</td>
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<td>48</td>
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<td>PLLx VCO maximum frequency</td>
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<td>128</td>
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<td>Clock Security System (CSS)</td>
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<td>O</td>
<td>O</td>
<td>O(13)</td>
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<tr>
<td>Clock Security System on LSE</td>
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<td>O</td>
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</tbody>
</table>

(1) Compatibility and features depend on the specific device variant.
### Table 4. STM32WB55 features over all modes (continued)

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Run Range 1</th>
<th>Run Range 2</th>
<th>Sleep</th>
<th>Low-power run</th>
<th>Low-power sleep</th>
<th>Stop0/Stop1</th>
<th>Stop 2</th>
<th>Standby</th>
<th>Shutdown</th>
<th>VBAT</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTC / Auto wakeup</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
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<tr>
<td>Number of RTC Tamper pins</td>
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<td>3</td>
<td>3</td>
<td>0</td>
<td>3</td>
<td>0</td>
<td>3</td>
<td>0</td>
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<tr>
<td>LCD</td>
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<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
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<tr>
<td>USB FS</td>
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<td>-</td>
<td>-</td>
<td>O</td>
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<tr>
<td>USART1</td>
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<td>O</td>
<td>O</td>
<td>O</td>
<td>O(14)</td>
<td>O(14)</td>
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<tr>
<td>Low-power UART (LPUART1)</td>
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<td>O</td>
<td>O</td>
<td>O</td>
<td>O(14)</td>
<td>O(14)</td>
<td>O(14)</td>
<td>O(14)</td>
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<tr>
<td>I2C1</td>
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<td>O(15)</td>
<td>O(15)</td>
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<td>I2C3</td>
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<td>O</td>
<td>O</td>
<td>O(15)</td>
<td>O(15)</td>
<td>O(15)</td>
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<tr>
<td>SPIx (x=1, 2)</td>
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<td>-</td>
<td>-</td>
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<td>ADC1</td>
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<td>VREFBUF</td>
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<tr>
<td>COMPx (x=1, 2)</td>
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<tr>
<td>Temperature sensor</td>
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<td>Timers TIMx (x=1, 2, 16, 17)</td>
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<td>Low-power Timer 1 (LPTIM1)</td>
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<td>Low-power Timer 2 (LPTIM2)</td>
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<td>O</td>
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<tr>
<td>Independent watchdog (IWDG)</td>
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<td>O</td>
<td>O</td>
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<td>Window watchdog (WWDG)</td>
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<td>SysTick timer</td>
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<td>True random number generator (True RNG)</td>
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<td>AESx (x=1, 2) hardware accelerator</td>
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</table>
### Table 4. STM32WB55 features over all modes\(^{(1)}\) (continued)

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Run Range 1</th>
<th>Run Range 2</th>
<th>Sleep</th>
<th>Low-power run</th>
<th>Low-power sleep</th>
<th>Stop0/Stop1 Wakeup capability</th>
<th>Stop 2 Wakeup capability</th>
<th>Standby Wakeup capability</th>
<th>Shutdown Wakeup capability</th>
<th>VBAT</th>
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<tbody>
<tr>
<td>PKA</td>
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<td>GPIOs</td>
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<td>(16) 5 pins</td>
<td>(17) 5 pins</td>
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</tbody>
</table>

1. Legend: Y = Yes (Enabled), O = Optional (Disabled by default, can be enabled by software), R = Data retained, - = Not available.
2. BLE not possible in this mode.
3. Standby with SRAM2a Retention mode only.
4. The Flash memory can be configured in Power-down mode. By default, it is not in Power-down mode.
5. Flash memory programming only possible in Range 1 voltage, not in Range 2 and not in Low-power mode.
6. The SRAM clock can be gated on or off.
7. SRAM2a content is preserved when the bit RRS is set in PWR_CR3 register.
8. Only in STOP0 if SMPS is enabled.
9. Stop 0 only. SMPS is automatically switched to Bypass or Open mode during Low-power operation.
10. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically turned off when the peripheral does not need it anymore.
11. The HSE can be used by the RF subsystem with the need to perform RF operation (Tx or Rx).
12. MSI maximum frequency.
13. In case RF will be used and HSE will fail.
14. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
15. I²C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
16. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
17. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.
2.5 A versatile clock management

A reset and clock controller (RCC) peripheral manages the STM32WB Series microcontrollers' seven clock sources.

Two external oscillators can be used for applications requiring high precision:

- The HSE clock (32 MHz high speed external clock), mandatory for RF operation, typically used to feed the PLL and to generate a CPU clock frequency of up to 64 MHz, and independent frequencies required for the USB controller and the audio clocks.
- The LSE (typically 32.768 kHz low speed external clock) normally used to provide a low-power clock source to the real time clock (RTC) and the RF sub-system, can also be used as LCD clock.

Five internal oscillators can be selected for various tasks:

- The LSI1 clock (32 kHz low speed internal clock) is a ultra-low-power source that can feed the real time clock (with a limited accuracy), the LCD controller and the independent watchdog.
- The LSI2 can be used as replacement for the LSE for RF framing, in low constraint applications. This oscillator has an inaccurate frequency but very low jitter characteristics, suitable for RF protocols.
- The HSI clock (16 MHz high speed internal clock) is a high speed voltage-compensated oscillator.
- The MSI clock (100 kHz to 48 MHz multi speed internal clock) is an oscillator with an adjustable frequency and low current consumption. It is designed to operate with a current proportional to the frequency, so as to minimize the internal oscillator consumption overhead for the low CPU frequencies. This oscillator can provide a high-accuracy signal when configured in PLL-mode, where it is auto-calibrated using the LSE.
- The RC48, when available, with clock recovery system (HSI48): the internal 48 MHz clock source (HSI48) can be used to drive the USB (except for the STM32WBx0) or the True RNG peripheral. This clock can be output on the MCO.

Table 5 summarizes the characteristics and uses of the various oscillators.
### Table 5. STM32WB Series microcontrollers clock source characteristics

<table>
<thead>
<tr>
<th>Clock source</th>
<th>Use</th>
<th>Frequency</th>
<th>Consumption (typical)</th>
<th>Accuracy</th>
<th>Trimming</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSE</td>
<td>Master clock for RF, CPUs, LCD and RTC</td>
<td>32.000 MHz</td>
<td>260 µA</td>
<td>Crystal dependent, down to few ppm</td>
<td>NA</td>
</tr>
<tr>
<td>LSE</td>
<td>RTC and LCD USART, LPUART, LPTIM</td>
<td>32.768 kHz( typical)</td>
<td>250 nA</td>
<td>Crystal dependent, down to a few ppm</td>
<td>Not applicable</td>
</tr>
<tr>
<td>HSI</td>
<td>Master clock</td>
<td>16 MHz</td>
<td>150 µA</td>
<td>± 0.8 % typical over -10 to +85 °C</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>Peripheral independent clock</td>
<td></td>
<td></td>
<td>+0.1 / -0.2 % typical over 1.62 to 3.6 V</td>
<td>Yes</td>
</tr>
<tr>
<td>MSI</td>
<td>Master clock</td>
<td>100 kHz</td>
<td>0.6 µA</td>
<td>Default mode: +1.5/-1 % typical over -10 to +85 °C</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>200 kHz</td>
<td>0.8 µA</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz</td>
<td>1.2 µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>800 kHz</td>
<td>1.9 µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz</td>
<td>4.7 µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 MHz</td>
<td>6.5 µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 MHz</td>
<td>11 µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8 MHz</td>
<td>18.5 µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16 MHz</td>
<td>62 µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>24 MHz</td>
<td>85 µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>32 MHz(2)</td>
<td>110 µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LSI1</td>
<td>RTC, LCD and IWDG</td>
<td>32 kHz</td>
<td>110 nA</td>
<td>±1.5 % typical over -40 to +125 °C</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+0.5/-1.5 % typical over 1.62 to 3.6 V</td>
<td>No</td>
</tr>
<tr>
<td>LSI2</td>
<td>RF</td>
<td>~32 kHz</td>
<td>200 nA</td>
<td>Low jitter</td>
<td>Yes</td>
</tr>
<tr>
<td>HSI48</td>
<td>USB, RNG</td>
<td>48 MHz</td>
<td>380 nA</td>
<td>±3 % max over 15 to 85 °C V&lt;sub&gt;dd&lt;/sub&gt; 3.0 to 3.6 V</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±4.5 % max over -40 to +125 °C V&lt;sub&gt;dd&lt;/sub&gt; 1.65 to 3.6 V</td>
<td>USB PLL</td>
</tr>
</tbody>
</table>

1. Preliminary characteristics, for information only. See product datasheet for detailed electrical characteristics.
2. Only possible in Range 1.
In addition, the STM32WB Series microcontrollers embed two PLLs (one PLL is available for the STM32WBx0), each of them provides up to three independent outputs and can be fed by the HSI, the HSE or the MSI. The six outputs can be configured independently for:

- The system clock
- The ADC interface clock
- The USB, true RNG clock
- The serial audio interface SAI1 clock

This removes the peripheral constraints on the system clock. Many other peripherals can be clocked independently from the system clock: USART, LPUART, I2Cx (x=1, 3) and LPTIMx (x=1, 2) receive an independent clock. This makes it possible, for instance, to reduce the system and APB bus frequencies and keep the communication peripheral baud rate constant, independently of the system clock frequency.

All peripheral clocks can be individually enable or disable in Run and Low-power run modes. The peripheral clocks can also be individually enable or disable in Sleep and Low-power sleep modes.

Although HSI and MSI are factory trimmed, they can be further trimmed in 0.5% steps during run time to compensate for frequency deviations due to temperature and voltage changes.

When LSE is present in the application, the MSI can be automatically calibrated using the LSE (PLL-mode configuration), making it possible to reach long-term LSE accuracy. This mode can provide the USB clock, with the accuracy required to operate in device mode.

Moreover the system clock when the MCU exits from Stop modes can be configured to be either HSI or MSI at any frequency range. This enables the exit from Stop mode directly at 48 MHz, without waiting for a PLL starting time.
3 Conclusion

The main features of the STM32WB Series microcontrollers presented in this application note demonstrate the benefits offered by this microcontroller family in reducing the current consumption in embedded communication systems.

Besides having the same characteristics of the STM32L4 ultra-low-power Series, the STM32WB Series microcontrollers offer high processing performance without compromising the power consumption. They complement the STM32 portfolio, maintaining compatibility with other STM32 devices.

The STM32WB Series microcontrollers rich set of peripherals, associated with the proprietary low-power RF subsystem enable the user to cover a wide range of applications, while the available low-power modes give full flexibility to adjust, on-the-fly, the consumption for any task.

This results in an extended operating lifetime for today and tomorrow’s constantly greener applications.
4 Revision history

Table 6. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>14-Sep-2018</td>
<td>1</td>
<td>Initial release.</td>
</tr>
<tr>
<td>21-Feb-2019</td>
<td>2</td>
<td>Changed document classification, from ST restricted to Public.</td>
</tr>
</tbody>
</table>
| 17-Oct-2019 | 3        | Added: Throughout the document: the exception for the STM32WBx0 in:  
  – **Introduction**: include the 2V support on STM32WBx0.  
  – **Section 1**: the STM32WBx0 support exclusion.  
  – **Section 2.2**: the supported voltages and exceptions for the STM32WBx0.  
  – **Section 2.2.1**: the exception for the STM32WBx0.  
  – **Section 2.4**: 2.13Msps support for the STM32WBx0, added the support restriction for the LCD display USB wake up.  
  – **Section 2.5**: USB support restriction and the available PLLs for the STM32WBx0.  
  Updated:  
  – **Table 3**: corrected consumption and wake up time figures.  
  – **Figure 6**: Specified the illustrated device reference.  
  – **Table 4**: Specified the device reference. |
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