life.augmented

AN6060

Application note

VIPower M0-9 motor drivers for automotive DC motor control

Introduction

The VIPower M0-9 DC motor drivers family are fully integrated and protected devices designed to drive low or medium power automotive DC motors.

Each device in the family contains the monolithic double high-side driver and two low-side chips.

The following features render these devices ideal for numerous DC motor applications (for example, door locks, washer pumps, fans, mirrors, etc.).

- Integrated logic for driving each MOSFET according to clockwise or anticlockwise motor rotation and braking.
- The possibility of employing PWM at 20 kHz for speed control.
- Embedded electrical or thermal protection against stress.
- Nondissipative current sensing.
- “MultiSense” diagnostic in ON and OFF state.
- Phase_Out functionality to monitor OUT status in ON and OFF state.

The purpose of this hardware design guide is to provide a comprehensive tool kit for design engineers to better understand M0-9 motor drivers behavior and the application usage context, as well as to facilitate embedding the design.

1 General items

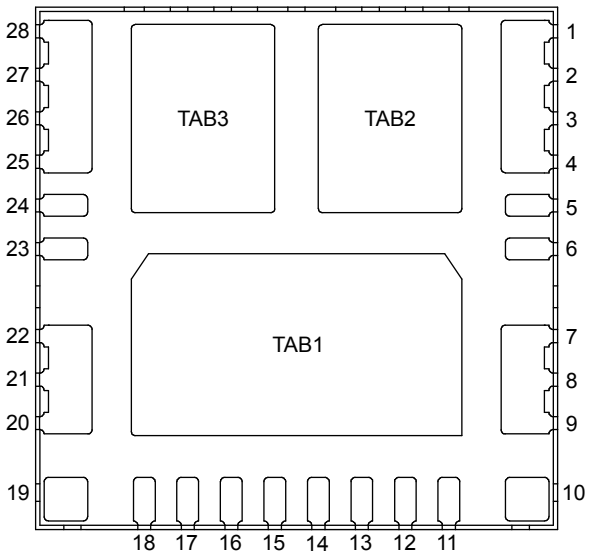
VIPower M0-9 DC motor drivers are built with the same technology blocks and feature several common properties. Depending on the load to be powered, the set of products has different $R_{DS(on)}$ (sum of RONHS and RONLS). The main representative devices are:

- VNH9030AQ: 30 mΩ typical per leg
- VNH9045AQ: 45 mΩ typical per leg
- VNH9090AQ: 90 mΩ typical per leg

1.1 Pin description

All M0-9 DC motor drivers designed for mid and low power applications are hosted in a specifically designed package QFN 6x6 triple pad with 28 leads and three exposed pads on the surface that create a further thermal path besides the leads resulting in a high thermic conductivity to the PCB. This significantly increases the power managed by the device. All the devices have the same pin out allowing an advanced pin to pin compatibility among the family, granting the customer a high flexibility for layout and software reuse.

Figure 1. Configuration diagram (bottom view)



GADG310320221022GT

Table 1. Pin definition and function

Pin	Symbol	Function
1, 2, 3, 4	GNDB	Source of low-side switch B.
5, 6, TAB2	DRAIN_LSB	Drain of low-side switch B.
7, 8, 9	SOURCE_HSB	Source of high-side switch B.
10, 19, TAB1	VCC	Power supply voltage.
11	INB	Counterclockwise input.
12	PH_OUT	Output of phase OUT diagnostic feedback.
13	SEL1	Address the MultiSense multiplexer.
14	SEL0	Address the MultiSense multiplexer.
15	MSense	Output of current sense and diagnostic feedback.
16	PWM	PWM input. Voltage controlled input pin with hysteresis, CMOS compatible. Gates of low-side power MOSFETs. Active high.

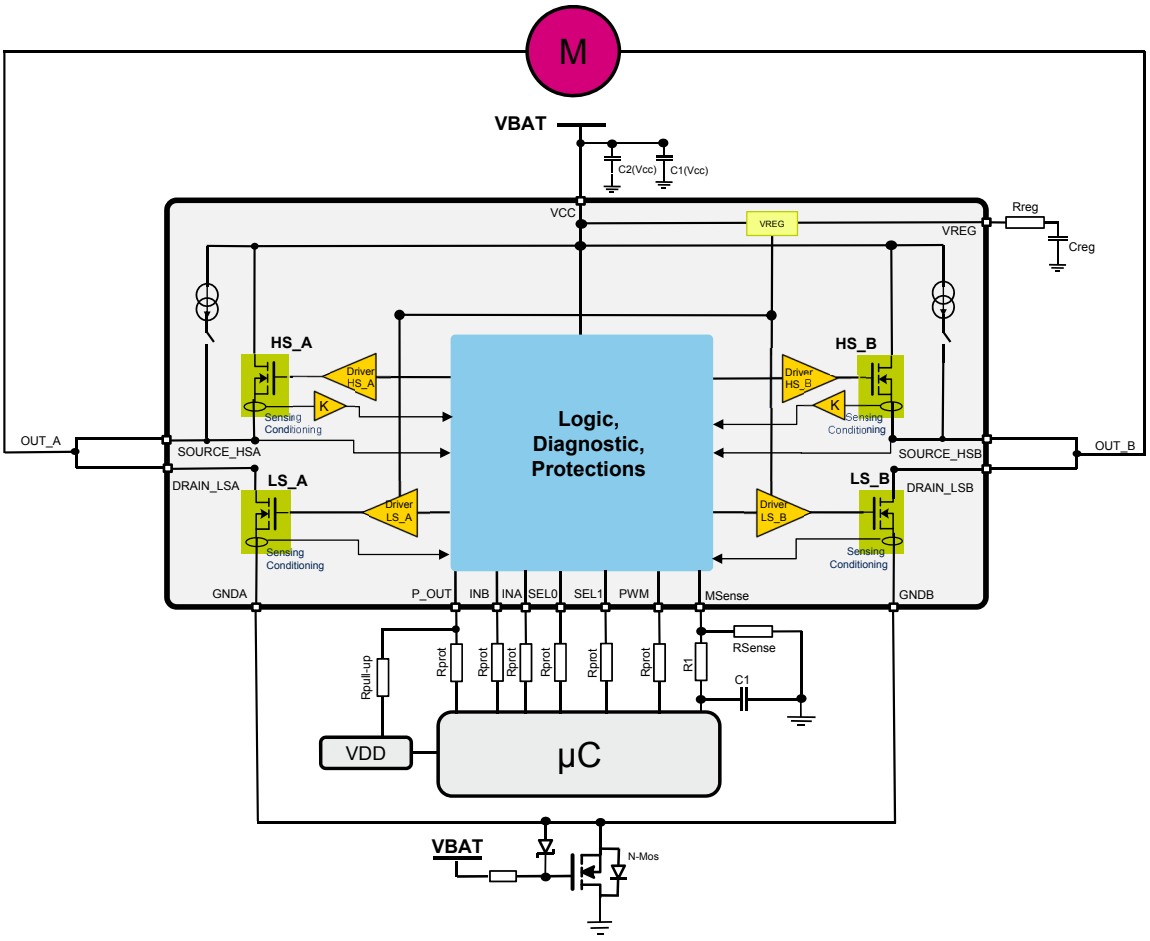
Pin	Symbol	Function
17	VREG	Internal voltage regulator that provides the supply for the gates of the internal low-side switches.
18	INA	Clockwise input.
20, 21, 22	SOURCE_HSA	Source of high-side switch A.
23, 24, TAB3	DRAIN_LSA	Drain of low-side switch A.
25, 26, 27, 28	GNDA	Source of low-side switch A.

Description of QFN 6x6 TRIPLE PAD pinout:

- **INA, INB:** Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. A logic high level on INA turns the high-side A (HSA) on, a logic high level on INB turns the high-side B (HSB) on.
- **PWM**: Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. A logic high level turns on one or both the low-side drivers, depending on selector PIN (SEL0 and SEL1) and INA and INB configuration (see Table 5. Truth table: operative condition and diagnostic). This can allow an advanced PowerMOSFET control, also for diagnostic features. In normal driving operation allows to perform a motor speed control, applying a square wave signal up to 20 kHz frequency.
- **VCC**: Power leads are connected internally to the two HS drains. Those leads must be connected to the battery track of the application.
- **GNDA, GNDB**: Those pins are connected internally to the LSA, LSB sources and they also represent the ground reference of the device's logic.
- **DRAIN_LSA, SOURCE_HSA** (respectively **DRAIN_LSB, SOURCE_HSB**): Those outputs are power pins that must be short-circuited together on the PCB and connected to one terminal of the external load. This connection is the clockwise terminal (respectively counter clockwise) of the bidirectional DC motor or, in the case of device employed in two half H-bridges topology, the positive terminal of the mono-directional motor is placed on branch A (respectively branch B).
- **SEL0, SEL1**: Voltage controlled input pins with hysteresis, compatible with 3 V and 5 V CMOS outputs. They act as multiplexer input pins in the following way(see Table 5. Truth table: operative condition and diagnostic):
  - In on state: they allow to sense, through the MultiSense output, the current flowing in the HSA (HSB) or a fault relevant to the output A (output B).
  - In off state: to check the voltage level of DRAIN_LSA, SOURCE_HSA (DRAIN_LSB, SOURCE_HSB) to detect and signalize, through the MultiSense output, an open load or an output stuck to V_{CC}.
  - In both ON and OFF states they allow to monitor the status of selected OUT through the PH_OUT pin.
  - Allow the MultiSense pin to develop a warning signal for high-side driver chip temperature (SEL0=high, SEL1=high)
- **MSense:** Multiplexed analogue sense output pin. This pin has three functions:
  - Delivers a current proportional to the HSA or HSB output current (according to respectively proper SEL0 and SEL1 settings see Table 5. Truth table: operative condition and diagnostic)
  - It develops a voltage flag in case of fail on the relevant output in on state as well as in off state
  - It develops a voltage flag in case of warning of high-side chip temperature
- **VREG:** Pin for the internal voltage regulator that provides the supply for the gates of the low-side switches. A capacitor of 100 nF vs. Ground and a series resistor R_{reg} of 220 Ω has to be connected on this pin.
- **P_OUT**: Phase OUT pin, it provides a digital signal to let an external uC the read of the OUT phase according to truth Table 5. Truth table: operative condition and diagnostic. It allows the system to detect if a single PowerMOSFET remains permanently ON or OFF independently from input state in both ON state & OFF state. The pin is an open collector.

1.2 Basic application schematic

Figure 2. **Typical application schematic**



GADG270620231443GT

Rprot: serial resistors are needed on digital inputs (INA, INB, SEL0, SEL1, PWM) to limit the current in the input structures as well as in the microcontroller output structures to a safe value during transient and reverse battery conditions. A proper value for such resistors is 1 kΩ.

R_{sense}: R_{sense} resistor converts the current sense output current, which is a copy proportional to the load current, into a voltage that can be read by the A/D converter of the microcontroller. The R_{sense} should be dimensioned to ensure proper resolution range and granularity to monitor nominal current as well as detecting open load or overload events. The typical value of R_{sense} is in the range of 1 kΩ (for hints on how to dimension the sense resistor please read Section 5.1.3: Dimensioning the R_{sense} resistor.)

R1, C1: A low pass-filter, such as an RC filter, can be placed across the Rsense resistor to suppress HF noise. The time constant of this filter (time constant is R*C) should be long enough to effectively suppress the noise and short enough to allow MultiSense signal stabilization considering multiplexer delay and settling times in case of a shared microcontroller A/D port. C1 should be placed close to the MCU's A/D input. Also, the ground connection for C1 should be at the same potential as the ground of the A/D reference. The filter resistor R1 (suggested value 10 kΩ) is also used to limit the A/D's input pin current.

C1(V_{CC}): this capacitor is used to suppress high energetic voltage transients originally, for example, when the motor rotates and the OUTPUTs go in tristate conditions due to a battery line cutoff (for details about dimensioning of C1(V_{CC}) please refer to Section 4: Load and device compatibility)

C2(V_{CC}): the C2 capacitor helps to suppress voltage transients that originate from other actuators connected in parallel and sharing the same battery line. This capacitor is capable to suppress only low energetic short transient pulses and HF noise at the V_{CC} pin (for details please refer to Section 4: Load and device compatibility)

Rreg and Creg: compensation network to properly polarize the internal Vreg

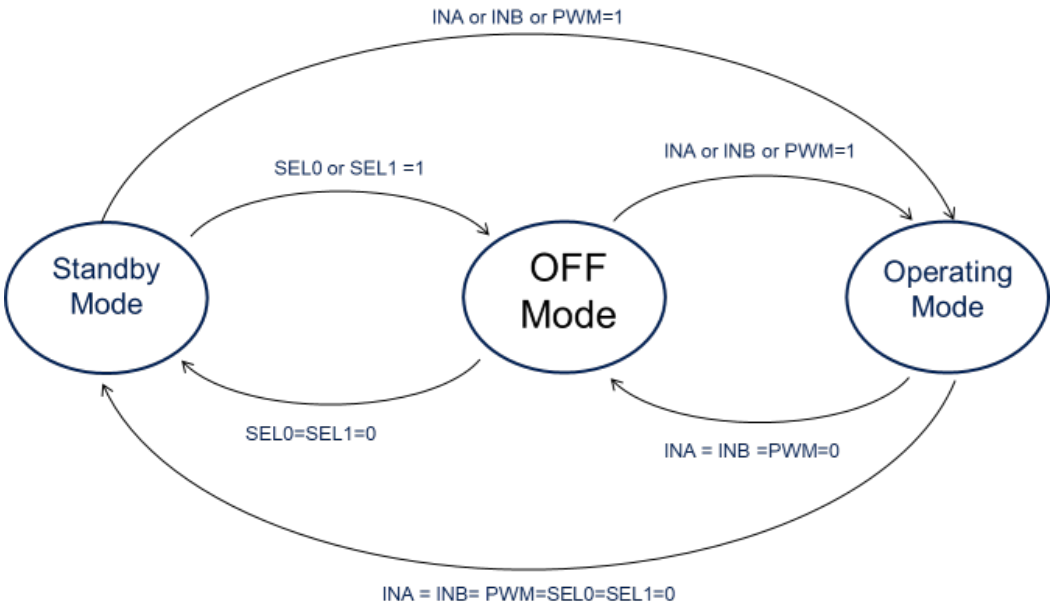
N-MOSFET, Rrev and Z illustrate the reverse battery network. The N-MOSFET with drain connected to the ground pins of VNH9XXX and source on power GND acts as reverse battery and battery negative fast transient protection. Its gate needs to be connected through a Rrev= 100 kΩ resistor to the battery track. A detailed description of this as well as other methods to protect the device against reverse battery is given in Section 4: Load and device compatibility.

1.3 Operating modes

The VNH9xxx H-bridges have three main states (as shown in the figure below):

- **Operating mode**: The device enters in this state when at least one of the input signals (INA, INB, PWM) is set to logic level high. This mode includes a motor driven in clockwise and counterclockwise directions, brake to GND/V_{CC} conditions.
- **OFF state** (no standby) device enters in this state when SEL0 or SEL1 are set to logic level high, whereas INA, INB and PWM are set to logic level low. In this mode the OUT Power MOSFETs are settled at high impedance and diagnostic in off state can be performed.
- **Standby mode**: this condition occurs when all input signals pins (INA, INB, PWM, SEL0, SEL1) are set to low. In standby mode the current drained by the bridge is 1 µA maximum in the temperature range from -40 °C to 85 °C. After the last input pin has been set to zero the H-bridge goes into standby mode with a delay of t_{D_stby} (reported in the datasheets). This delay has the purpose of avoiding entering standby mode during a fast commutation of all input pins to zero level, so no accidental standby can occur. The device exits the standby condition as soon as anyone of INx, PWM, SELx pins is set high (please see figure below).

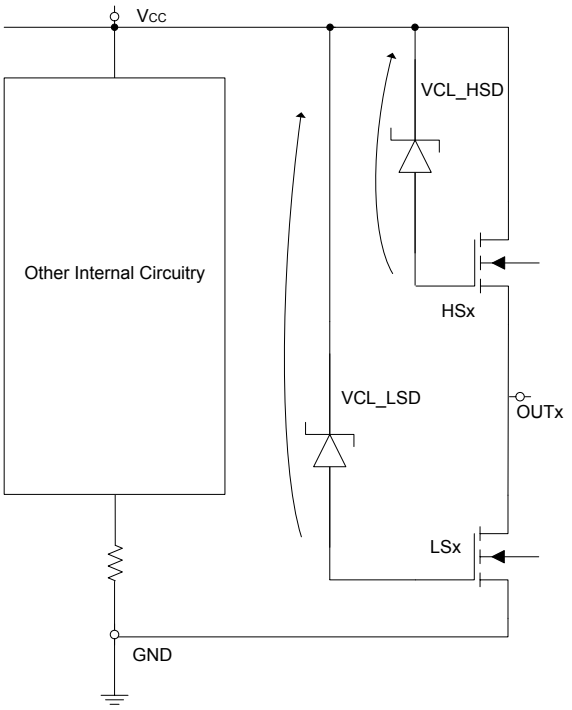
Figure 3. H-bridges operating modes



2 Embedded protections

The structure V_{CC} to GND of Typical VNH9xxx is commonly protected against the high voltage transients with a special circuit shown in Figure 2. Typical application schematic.

Figure 4. Voltage clamp block diagram



2.1 Protection against overvoltage

2.1.1 Overvoltage clamp

The device is protected against voltage transients on V_{CC} (for example: ISO7637/2 transients) via the combination of the HS and LS power clamps (indicated in the datasheet as VCL_HSD and VCL_LSD respectively). As soon as a voltage transient higher than VCL_HSD = VCL_LSD occurs on V_{CC}, the LS is forced to work in the ohmic region while the HS is forced to work in the saturation region. Therefore, the component subjected to the highest dissipation is the HSDx.

For negative transients applied across the device supply pin terminals, most of the current flows through the PowerMOS body diodes. It is not limited by anything other than the pulse generator intrinsic resistance.

External circuitry is normally used to protect the device against such events.

2.2 Undervoltage protection

This function shuts down the device when battery voltage V_{BAT} is lower than V_{USD} (given in the datasheet) with an active high signal acting directly on the LS and HS gates, turning them off.

This protection validates the internal supply as soon as it can supply all logic blocks appropriately:

- For V_{CC} decreasing from 13.5 V, the device is turned off at about 2.7 V; current sense is disabled from about 3.4 V of V_{CC}.
- Normal behavior resumes when V_{BAT} reaches V_{USD} + $V_{USDHYST}$.

Note: The undervoltage condition is not considered a fault condition so it is not reported by the diagnostic.

As V_{CC} rises, the device is typically turned on at 2.8 V. Current sense starts to operate at about 3.4 V.

Parameters that represent undervoltage behavior are given in the datasheet:

- V_{USD} is the maximum shutdown voltage when V_{CC} is decreasing.
- V_{USD_RESET} is the level which turns on the bridge when V_{CC} is increasing.
- V_{USD_HYST} is the typical hysteresis of the two voltages.

2.2.1 Device behavior with respect to ISO7637-2:2011(E) and ISO16750 standards

The table below describes the device performance with tests applied to VNH9XXX only, without components and accessed through V_{CC} and GND terminals only.

Status II is defined in ISO 7637-1 function performance status classification (FPSC) as: *"The function does not perform as designed during the test but returns automatically to normal operation after the test"*.

During negative pulses (1 and 3a) the energy is transmitted through the series of body diodes of the HS and LS and the body diode of the clamp signal circuit.

Table 2. ISO 7637-2 – electrical transient conduction along supply line

Test pulse 2011 (E)	Test pulse severity level with status II functional performance status		Minimum number of pulses or test time	Burst cycle/ pulse repetition time		Pulse duration and pulse generator internal impedence
	Level	U_S(1)		Min.	Max.	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
4(2)	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2: 2010						
Test B(3)		35 V	5 pulses	1 min.		400 ms, 2 Ω

1. *US is the peak amplitude as defined for each test pulse in ISO 7637-2: 2011 (E).*
2. *Test pulse from ISO 7637-2: 2004 (E).*
3. *With 35 V external suppressor referred to ground (-40 °C < T_J < 150 °C).*

2.2.2 Device behavior after a load dump

Load dump refers to the disconnection of the vehicle battery from the alternator while the battery is being charged. The bridges are subjected to pulses simulating this condition, according to ISO165750-2 (see Figure 6. Example of waveforms relevant to ISO pulse 5b (load dump) applied to a VNH9xxx).

Figure 5. Pulse waveform for ISO165750-2 test

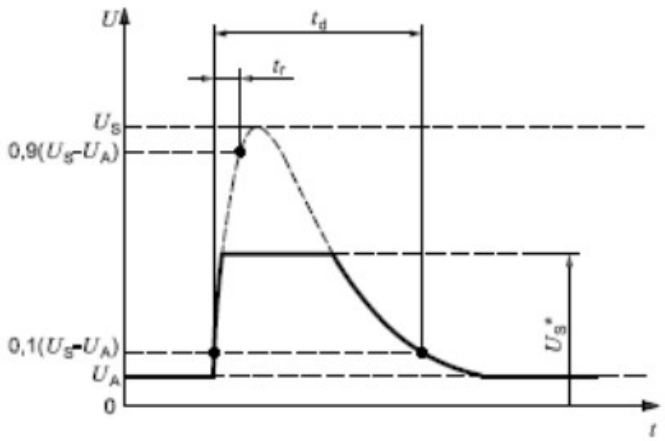
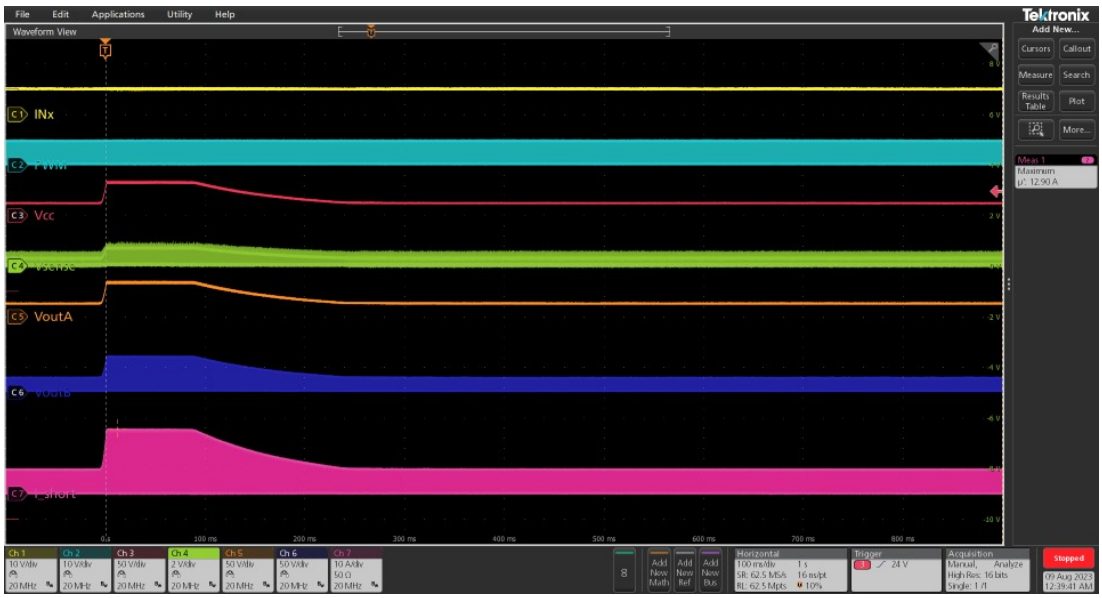


Figure 6. **Example of waveforms relevant to ISO pulse 5b (load dump) applied to a VNH9xxx**



The PowerMOSFET energy of the LS and HS is not given in the datasheet since the device is intended to be used in H-bridge driver configuration. The inductive energy of the load in fact normally recirculates in the PowerMOSFET body diodes.

External components like filtering capacitors on V_{CC} are necessary to smooth the effect of the battery transient listed in the tables for ISO7637-2 and ISO 16750-2 (see Section 3: External protections).

2.3 Loss of V_{CC} and loss of GND

2.3.1 GND disconnection

Following GND disconnection, the device can stop normal operation (motor rotation control) but it must end up in a safe operating state with no motor activation.

2.3.1.1 Device GND pin disconnection

This can occur due to physical defects in PCB soldering.

Any H-bridge in an QFN 6x6 triple pad 26+2L package has eight different GND pins. These are split in two groups of four pins each, where each is connected to the relevant LS source.

A soldering issue causing all GND pins to be disconnected from the PCB is quite unlikely and, even if does occur, all four PowerMOSFETs are switched off.

The device resumes normal operation once GND is reconnected.

2.3.1.2 Disconnection of the module GND line

If the module GND line that supplies the VNH9xxx is disconnected, the device switches off immediately, as shown in the following figure.

As the H-bridge Power elements are OFF, any residual motor energy is dissipated in the external IC components, especially the capacitor on the V_{CC} pin. This is charged and must be properly dimensioned

Note: External precautions are necessary to avoid the load energy increasing voltage V_{CC} above V_{CLAMP}, which may damage the device.

Figure 7. **GND loss, clockwise case (CH1=INA, CH2=PWM, CH3=V_{CC}, CH5=V_{outA}, CH6= V_{outB}, CH7=Iload)**

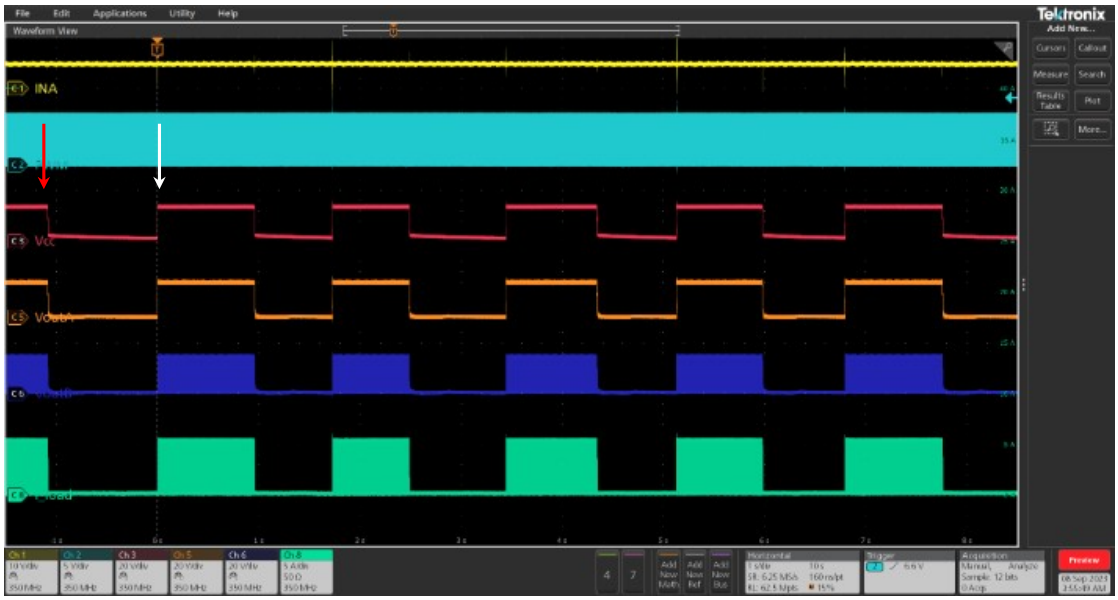
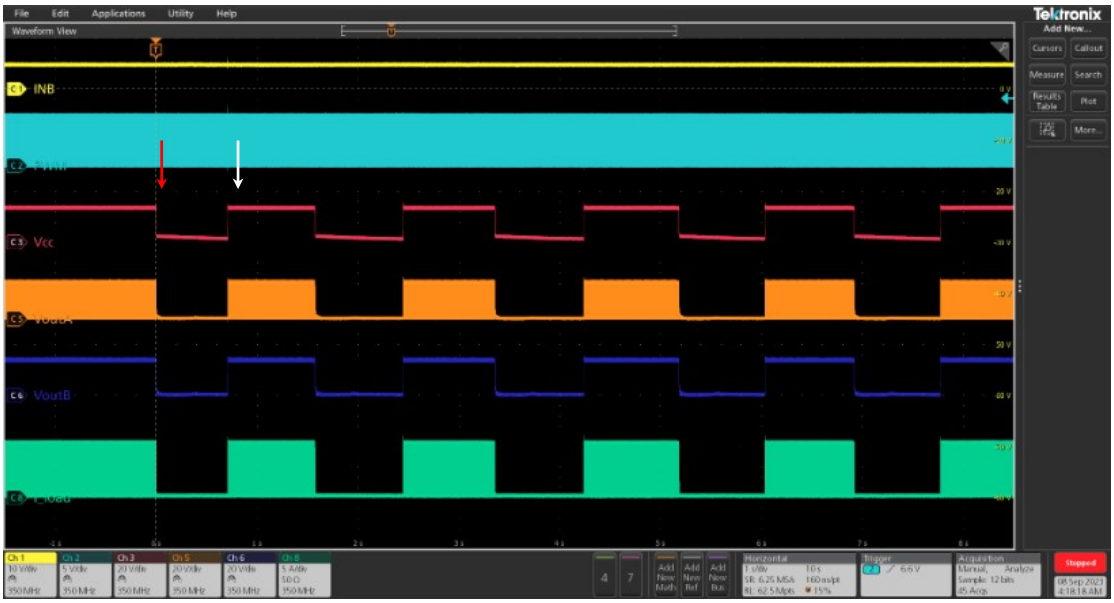


Figure 8. **GND loss, counterclockwise case (CH1=INB, CH2=PWM, CH3=V_{CC}, CH5=V_{outA}, CH6= V_{outB}, CH7=Iload)**



In the figure above, where the device is alternatively driven clockwise and counter clockwise:

- red arrow: the device stops operation immediately after GND disconnection
- white arrow: device restarts normal operation as the GND line is reconnected.

2.3.2 Loss of battery connection

Similar considerations are applicable to the battery where multiple pins (exposed pad included for QFN 6x6 triple pad 26+2L package) are connected to the V_{CC} signal.

2.3.2.1 Battery line disconnection

When battery disconnection occurs, the device V_{CC} voltage starts to decrease since the bulk capacitor energy is used to supply the motor.

Figure 9. **Battery loss (CH1=INA, CH2=PWM, CH3=V_{CC}, CH5=V_{outA}, CH6= V_{outB}, CH7=Iload)**

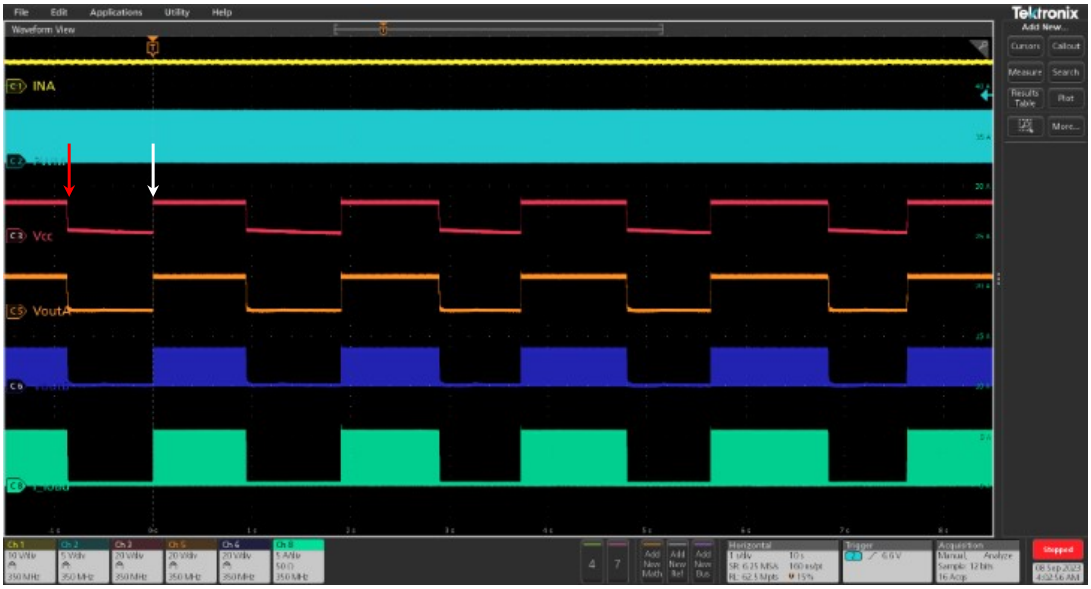
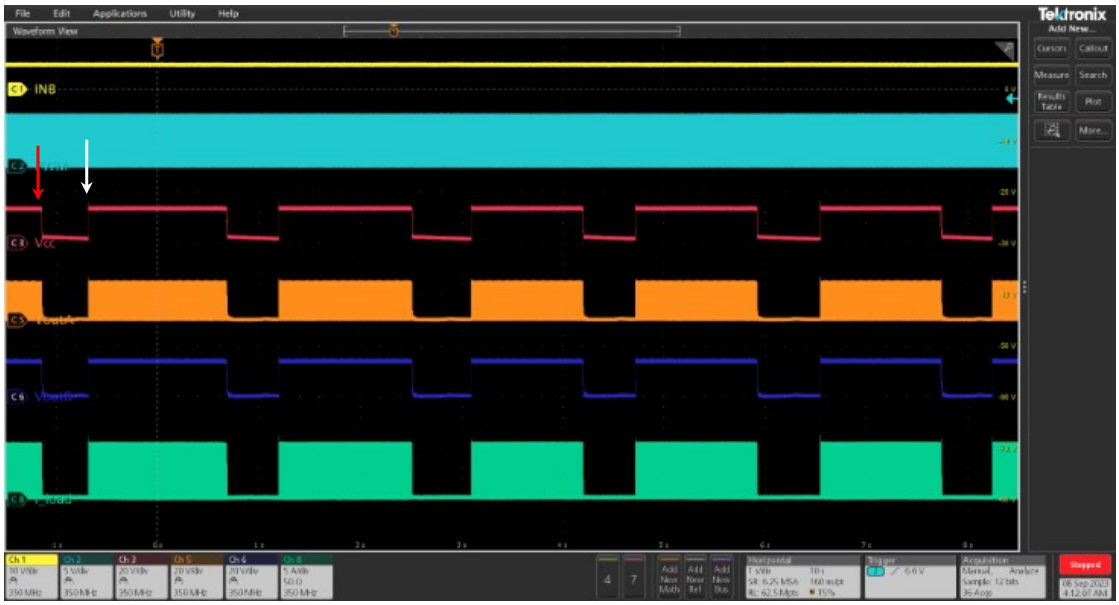


Figure 10. **Battery loss (CH1=INB, CH2=PWM, CH3=V_{CC}, CH5=V_{outA}, CH6= V_{outB}, CH7=Iload)**



- red arrow: motor operation stops as the V_{CC} undervoltage threshold is reached
- white arrow: operation restarts once battery is reconnected.

Note: External precautions are necessary to avoid the load energy increasing voltage V_{CC} above V_{CLAMP}, which may damage the device.

2.4 Short-circuit protection

Short-circuit events are signaled by the diagnostic MSense pin (output of current sense and diagnostic feedback in VNH9030AQ). In fault conditions, V_{MSense} is pulled high to V_{SENSEH} on the selected leg (when SEL0 and SEL1 are properly configured).

2.4.1 Short-circuit on device outputs to car ground

For output shorted to GND, the high-side in the ON state is the stressed element in the VNH9xxx and the drain current rises well above nominal levels.

When the I_{LIM_HSD} threshold is reached, an embedded current limiter intervenes to protect the high-side PowerMOSFET against dangerous current density.

In this condition, the high-side PowerMOSFET works in the saturation region and dissipates high power due to simultaneous high voltage and high current.

At this point, the power limitation block circuit, designed to limit the fast thermal transients in the device to improve device lifetime, intervenes by latching the concerned high-side PowerMOSFET. This protection monitors the difference between the temperature read by a case temperature sensor embedded in the logic and the junction temperature measured by a sensor in the PowerMOSFET.

The HS is also protected against absolute maximum junction temperature (datasheet symbol T_{TSD}) by the overtemperature thermal shutdown block.

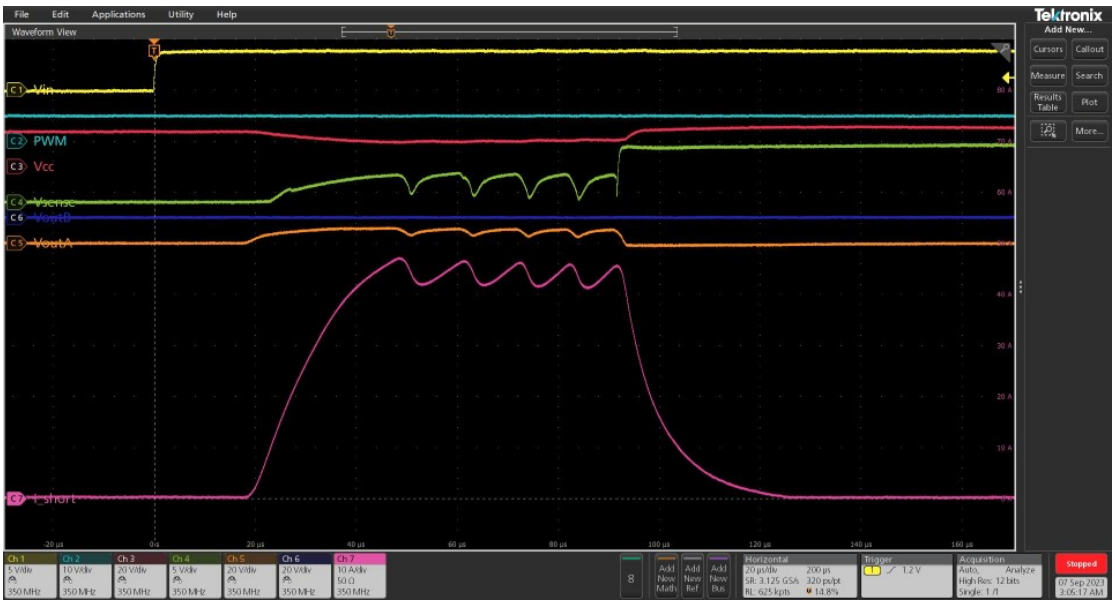
In case of low thermal transients (soft short-circuits), the temperature rises to the HS thermal shutdown level (typically 175 °C), causing the device to switch off and latch; this fault is signaled through the MSense pin by pulling it to V_{SENSEH} (when SEL0 and SEL1 are properly configured).

In summary, the HS has the following protection circuits:

- Current limitation: the triggering of this protection is not signaled by MSense (MultiSense) and does not cause device latch off
- Power limitation circuit: the triggering of this protection is signaled by MSense (MultiSense) and causes device latch off
- Overtemperature shutdown circuit: the triggering of this protection is signaled by MSense (MultiSense) and causes device latch off

In the figure below, the device terminal A is shorted to GND and then switched on.

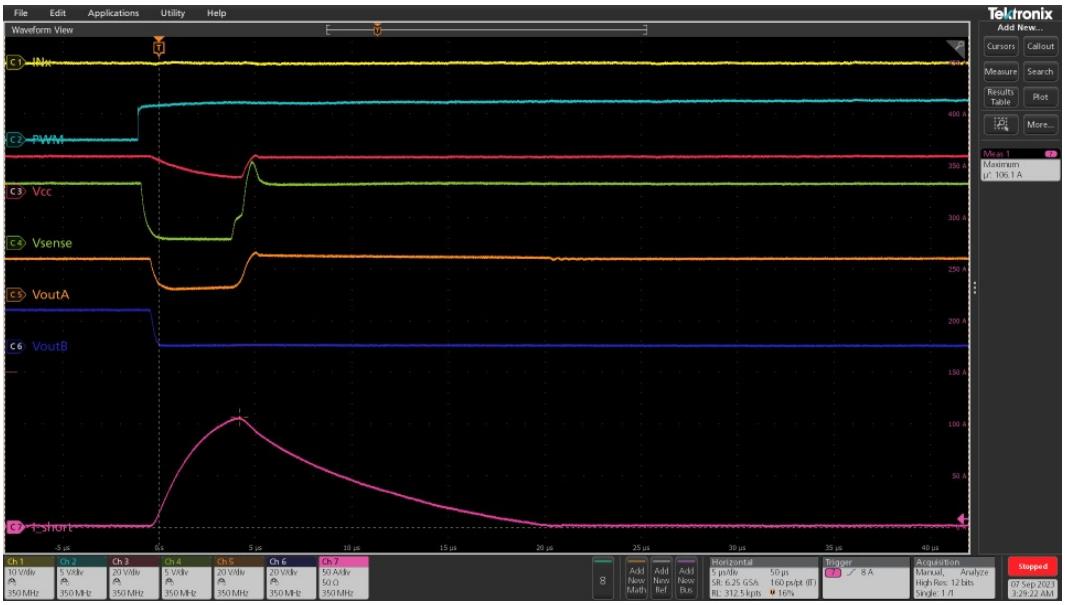
Figure 11. Power limitation event, terminal condition (CH1=INA, CH2=PWM, CH3=V_{CC}, CH4=V_{Sense}, CH5=V_{outA}, CH6= V_{outB}, CH7=IShort)



2.4.2 Hard short-circuit

In a hard short-circuit (few mΩ resistance), as soon as the current through the low-side MOSFET exceeds the I_{SD_LSD} shutdown current, the device is switched off after a certain filtering time (indicated as t_{SD_LSD} in the datasheets) and it latches. The fault condition is then detected by the diagnostic.

Figure 12. VNH9030AQ short to V_{CC} event (CH1=INA=INB, CH2=PWM, CH3=V_{CC}, CH4=V_{Sense}, CH5=V_{outA}, CH6= V_{outB}, CH7=I_{Short})



A filtering time (datasheet symbol t_{SD_LSD}) after the LS current reaches its threshold helps to avoid unwanted low-side latching at switch-on when, for example, filtering capacitors are placed on the VNH9xxx OUTPUTs.

Just before LSx switch-on, the corresponding OUTx is at battery voltage. When the LSx is switched on, the output filtering capacitor is subjected to rapid voltage variation and a consequent current spike.

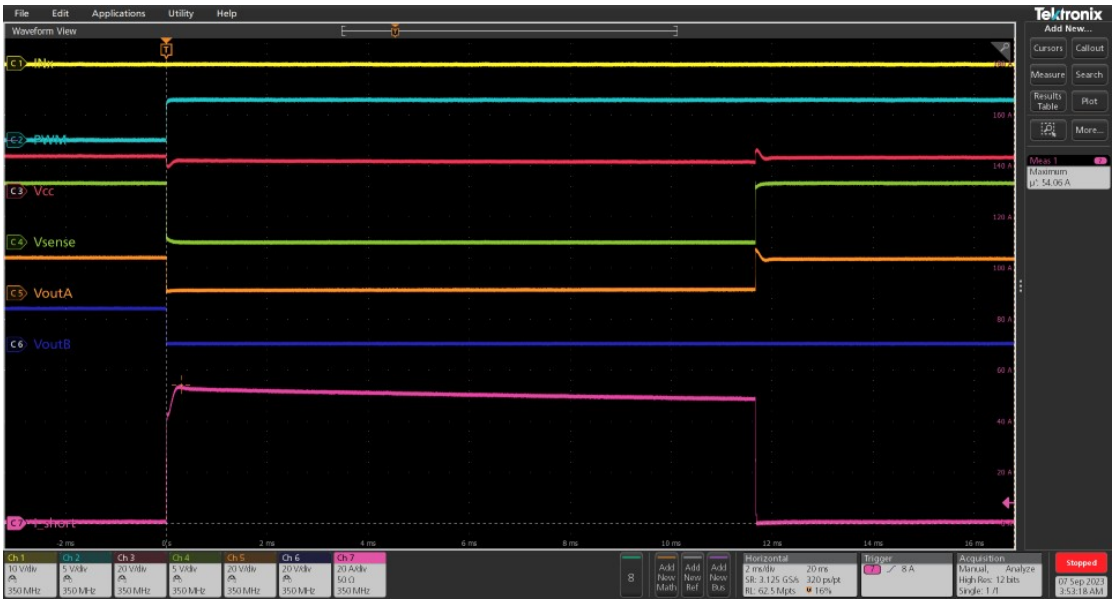
Depending on capacitor size and LS switch-on time (t_f in datasheet), this current spike can reach I_{SD_LSD}, which is why this protection needs to be filtered out.

2.4.3 Resistive (soft) short-circuit–overload

In a resistive short-circuit, the current through the low-side MOSFET does not reach I_{SD_LSD}, but the temperature rises to the LS thermal shutdown level (datasheet symbol T_{TSD}, typically 175 °C), causing the device to switch off and latch; this fault is detected by the diagnostic indication on MultiSense.

In the figure below, the device terminal A is before shorted to V_{BAT} and then the LSA is switched on.

Figure 13. **VNH9030AQ short to V_{CC} event (CH1=INA, CH2=PWM, CH3=V_{CC}, CH4=V_{Sense}, CH5=V_{outA}, CH6=V_{outB}, CH7=I_{Short})**



In summary, the low-side has the following protection circuits:

- Shutdown low-side current: triggering of this protection is signaled by MSense (MultiSense) and causes the device latch off
- Overtemperature shut down circuit: triggering of this protection is signaled by MSense (MultiSense) and causes the device latch off

Note: The VNH9xxx enters standby mode if all logic pins (INA, INB, SEL0, SEL1 and PWM) are at low logic level. The aim of standby is to minimize the device current consumption while the module is idle.

Note: At device power on from standby mode, it is recommended to toggle either INA, INB, SEL0, SEL1 out of STBY mode and then toggle PWM with a delay of at least 20 µs. This avoids overly stressing the LS in the case of permanent short-to-battery.

The device behavior in the case of short-circuit to VBAT is influenced by the initial state:

- Starting from the STBY condition, the internal logic needs around 20 µs to detect the short to V_{Bat} and turn off the LS, during which time the device operating current is well above I_{SD_LSD}. The characteristics of the short-circuit (stray inductance and resistance) play a key role in limiting the current slope and following the max peak current.
- Starting from a condition other than STBY, the internal logic detects the fault immediately after the built-in filtering time (tSD_LSD), turning off the LS at a lower peak current.

2.4.4 Short-circuit across the load

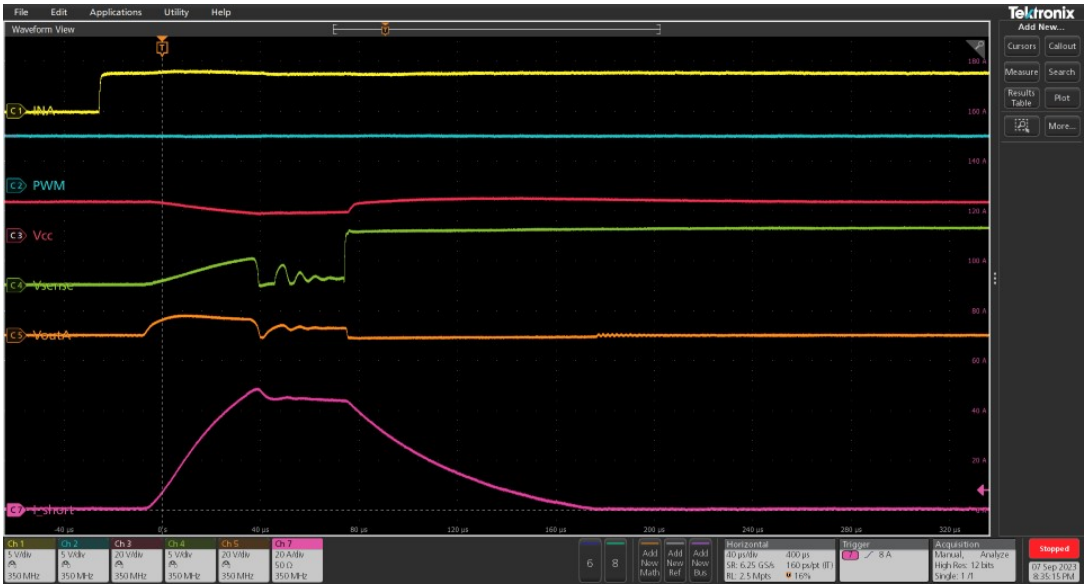
A hard short-circuit across the load triggers the overload current shutdown protection of the PowerMOSFET with the lowest value, by latching the concerned PowerMOSFET. The VNH9xxx bridges are designed with the high-side current limitation (I_{LIM_HSD}) lower than the low-side shutdown current (I_{SD_LSD}).

2.4.4.1 Short-circuit is applied so that HSA is switched on while the LSB is already on

In the following figure, at the HS switch on V_{DS_HS}= V_{CC} – V_{outA} ~ V_{BAT}, meaning that the whole battery voltage is across the HS terminals. In this condition, the HS dissipates a lot of power deriving from I_{LIM_HSD} x V_{BAT}, while the power dissipation inside the LS is much less as the LS V_{DS} is well below 1 V.

As the HS is in high dissipation, either power limitation or thermal shut down circuit will latch the device off.

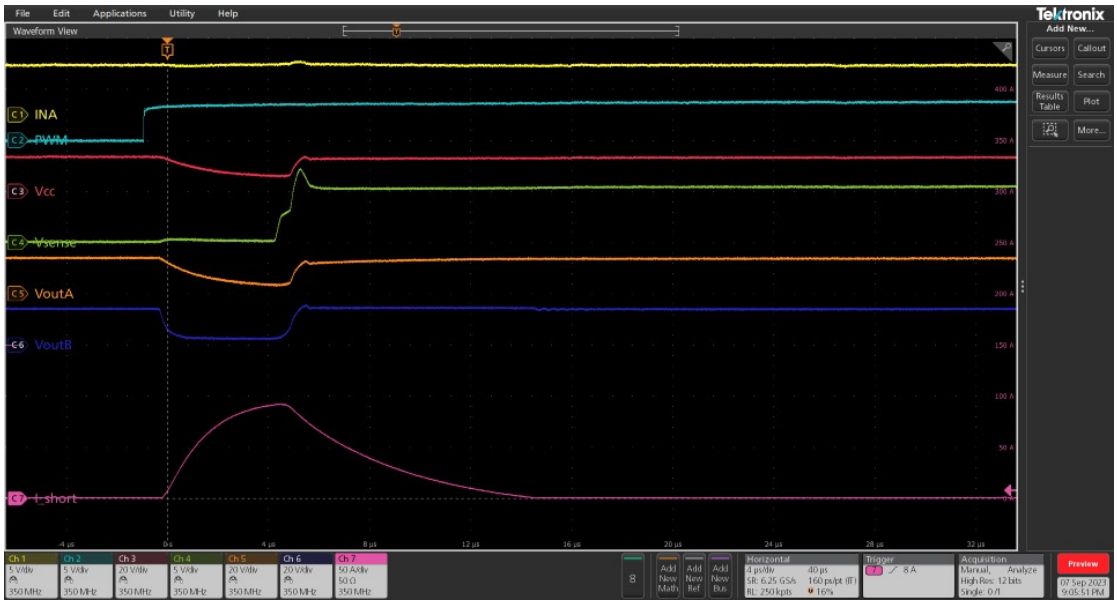
Figure 14. **VNH9030AQ short across load event (HSA switched on while LSB is already ON)**



2.4.4.2 *Short-circuit is applied so that LSB is switched on while the HSA is already on*

In this second case, the device latches due to LS protection triggering (I_{SD_LSD} reached).

Figure 15. **VNH9030AQ short across the load event (LSB switched on while HSA is ON)**



2.4.4.3 *Short circuit occurs when HSA and LSB are both on*

In this third case, the overshoot of the HSA current limiter lets the LSB reach its shutdown current protection I_{SD_LSD} and cuts the short-circuit current by latching the device off.

2.5 Cross conduction suppression

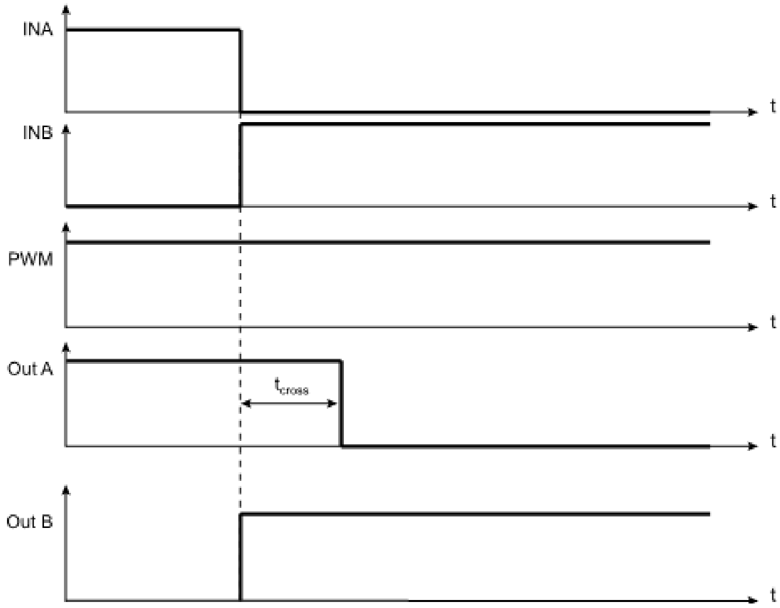
In normal operation, an H-bridge drives a motor in two directions: clockwise (HSA on, LSB on) and counter clockwise (HSB on, LSA on). It cannot switch both PowerMOSFET of the same leg on at the same time as this causes a short to GND battery event (cross conduction event).

To avoid this behavior, the VNH9xxx ICs implements specific logic:

- When INA is toggled high, the complemented signal immediately turns off the LSA MOSFET before the charge pump circuitry has had the time to switch on the HS MOSFET; like for INB and LSB. This protection takes advantage of the switching time difference between the low-side MOSFET and the high-side MOSFET; due to the charge pump circuitry, the HS switch has slower turn-on/turn-off times compared to the LS MOSFET.
- When INA is toggled low, HSA switch off is slower than LSA switch on, so a delay (t_{cross} of about 160 μs) is added to ensure LSA switch on after HSA switch off; like, for INB, HSB and LSB. Therefore, t_{cross} is longer than the HS switch off time (t_{off}).

The figure below shows a change of direction from HSA and LSB in on state to HSB and LSA in on state, and indicates the t_{cross} delay before the LSA is turned on (delay time for turning on of HSB is not shown).

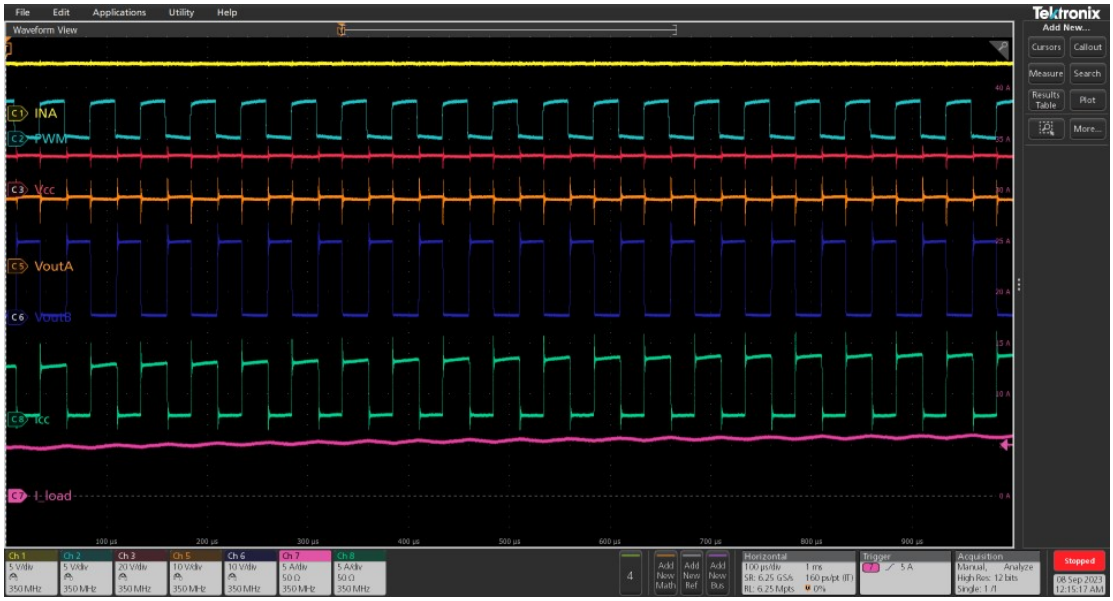
Figure 16. Cross current delay



The M0-9 H-bridge drivers are designed to avoid shoot-through during operation in PWM, even in adverse ambient conditions.

In the figure below, the high-side is in the DC condition (HSA is on, HSB is off), while the low-side is toggling as per the PWM signal.

Figure 17. V_{batt}=13.5 V, T_J=25 °C, duty cycle 50%, (CH1=INA, CH2=PWM, CH3=V_{CC},CH5=V_{outA}, CH6= V_{outB}, CH7=Iload, CH8=I_{CC})



The current peaks on I_{CC} are due to the intrinsic HS diode recovery time.

The VNH9xxx devices are immune to shoot-through, a typical dynamic issue in bridge topology. As soon as any LS is switched on by a PWM signal, a negative dv/dt is applied to the high-side of the same leg output.

Potentially, the dv/dt on output could be coupled through the high-side capacitance to its gate (C_{GD} and C_{GS}). Depending on the HS gate-source pull down impedance, current may flow from battery to ground, resulting in extra power dissipation (the impact of which can be significant at high frequencies) and hazardous conditions for the device. This problem is avoided by design in the VNH9xxx bridge.

3 External protections

3.1 Reverse polarity protection

A common problem in the automotive environment is damage when car battery terminals are connected incorrectly.

H-bridge ICs in VIPower technology include two parasitic p-n diodes from GND to the supply voltage pin V_{CC} (2 x V_f ~ 1.5 V). An inverse supply voltage would allow high current to flow through these diodes and damage the device.

Electronic safeguards involving passive or active reverse polarity protection need to ensure that any reverse current flow and reverse bias voltage is low enough to prevent damage to internal electronics.

Reverse polarity protection strategies can be:

- active or passive
- on battery line (V_{CC} terminal) or on GND line (GND terminal)

Four possible reverse battery protection solutions are summarized in the following table.

Table 3. Reverse battery protection designs

Reverse battery protection concept	Active or passive	Connection of protection	PROs	CONs
Schottky diode	Passive	V_{CC}	Reduced circuit complexity	Lower system efficiency, especially for high power applications
P-channel MOSFET	Active	V_{CC}	Reduced circuit complexity Higher system efficiency Suited for high power applications	
Reverse FET	Active	V_{CC}	Reduced circuit complexity thanks to embedded gate charge pump Much higher system efficiency Suited for high power applications	
N-channel MOSFET	Active	GND	Reduced circuit complexity Much higher system efficiency Suited for high power applications	Shift of GND level
N-channel MOSFET	Active	V_{CC}	Much higher system efficiency Suited for high power applications	Increased circuit complexity due to gate charge pump requirement

3.1.1 Diode in series with battery line

3.1.1.1 Protection behavior

Normal operation (positive battery voltage)

All load current flows through the diode, which must be chosen in order not to allow the junction temperature to exceed the maximum. Here it is the formula to apply:

$$DTj = Tj(D)max - Tamb, \max < P{*}R_{thj\_amb} \quad (1)$$

Where:

- $T_{amb,max}$ is the maximum ambient temperature
- R_{thj_amb} is the thermal resistance (junction to ambient) for the device and mounting use.

Power dissipation is given by:

$$P = V_{TO}{*}I_{F(AV)} + rd{*}I^2_{F(ac,rms)} \quad (2)$$

Where:

- $I_{F(AV)}$ = average value of the forward current (DC component)
- $I_{F(ac,rms)}$ = RMS value of the AC component of the forward current
- rd (small signal diode resistance) and V_{TO} depend on the special characteristics of the diode and can be extracted from the diode datasheet.

Behavior during reverse battery polarity

The diode is off once polarity is inverted; no current can flow in this state other than the rated leakage reverse current.

The diode breakdown voltage V_z must be higher than the reverse battery voltage value (typ.: 16 V).

Another important aspect is the peak reverse voltage limit of the Schottky diode (V_{RRM}). If we consider the maximum repetitive reverse voltage of the diode, it must be:

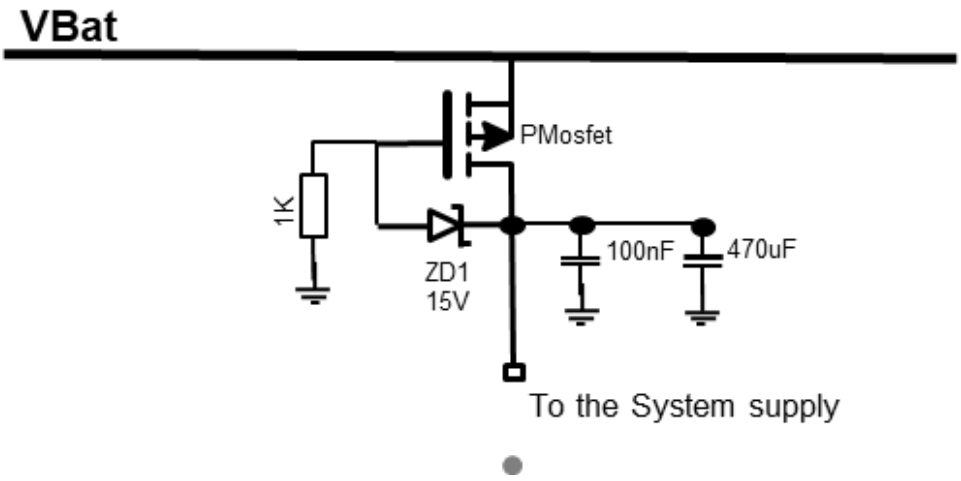
- V_{RRM} > 150 V for “ISO 7637-2:2011(E)” pulse 1 test level IV.

During the negative ISO7637-2 transients, the motor is supplied by the electrolytic filtering capacitor on V_{CC}.

The advantage of a Schottky diode over a standard diode is a very low voltage drop in the forward direction, hence power dissipation is reduced. This solution can be used for low current motors.

3.1.1.2 *P-channel MOSFET in the V_{CC} line*

Figure 18. Reverse battery protection with P-channel MOSFET



3.1.1.2.1 Protection behavior

Normal operation (positive battery voltage)

After the power-up phase when the P channel MOSFET body diode is forward-biased, a negative gate-source voltage switches on the P channel MOSFET.

Behavior during reverse battery polarity

The P channel MOSFET is switched off since its gate-source voltage is positive (voltage drop over the Zener diode); no current can flow in this state.

3.1.1.2.2 External component selection

The Zener diode ZD1 is dimensioned based on:

- V_z above the nominal battery voltage to avoid high module standby current;
- V_z must be below the P- Ch PowerMOSFET gate-source voltage absolute maximum rating;
- Power rating enough to handle the current in case of a load dump event.

The resistor between gate and GND limits the current through the Zener diode at supply voltages higher than the Zener voltage and limits the charging or discharging current of the gate.

This resistor, together with the gate capacitance of the P-channel MOSFET, also determines the turn-off time when exposed to fast negative transients or abrupt reverse polarity according to LV 124: 2013-06 standard.

1 kΩ appears to be a good compromise between minimizing the charging/discharging current and ensuring a fast turn-off time.

As the P-channel MOSFET also carries the load current, it needs to be properly dimensioned to handle the whole load current.

A capacitor could be placed between the gate and the source of the P-channel MOSFET.

The RC filter composed of the 1 kΩ resistor and the capacitor can be dimensioned to be transparent against the fast negative pulses ISO 7637-2:2011(E) pulse 1 test level IV, keeping the reverse polarity protection circuitry switched ON.

The main PowerMOSFET parameters to be considered are:

$V_{(BR)DSS}$, V_{gs_th}, $R_{DS(on)}$

- The P channel MOSFET breakdown voltage ($V_{(BR)DSS}$) must be higher than the reverse battery voltage value (typ. 16 V).
- The maximum gate-source threshold voltage (absolute value) of the P-channel MOSFET must be lower than the minimum battery voltage.
- The P channel $R_{ds(on)}$ must be such that power dissipation is kept low enough to keep the junction temperature below the rated maximum (150 °C).

$$|V_{gs\_th(max)}| < V_{batt(min)} \quad (3)$$

$$DTj = Tj_{Pch\_max} - T_{amb\_max} = R_{DS(ON)max} * I^2_{motor\_RMS\_max} * R_{thj\_amb} \quad (4)$$

Where:

- $T_{amb,max}$ is the maximum ambient temperature;
- $I_{motor\_RMS\_max}$ is the RMS motor current calculated at the maximum battery voltage.

If no low pass filter is placed on the P channel gate, any negative ISO transient opens the P channel MOSFET.

The motor is then supplied by the electrolytic filtering capacitor on the V_{CC}.

A standard logic MOSFET is normally recommended for noise immunity issue.

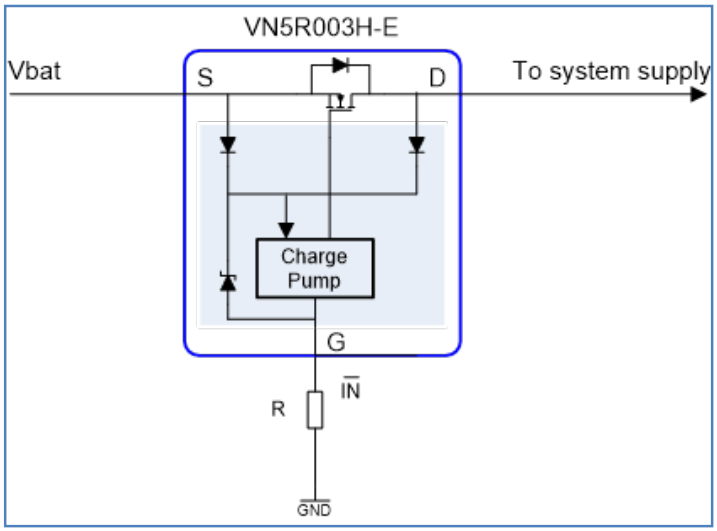
The Zener diode clamps the gate of the MOSFET to its Zener voltage and protects it against overvoltage.

The same reverse battery protection can be shared among several bridges connected to the battery.

3.1.1.3 *Dedicated ST reverse FET solution*

The VN5R003H-E device uses VIPower™ technology by ST to provide reverse battery protection for an electronic module. It consists of an N-channel MOSFET and driver circuit, two power pins (drain and source) and a control pin (IN_NOT).

Figure 19. Reverse polarity protection – reverse FET protection

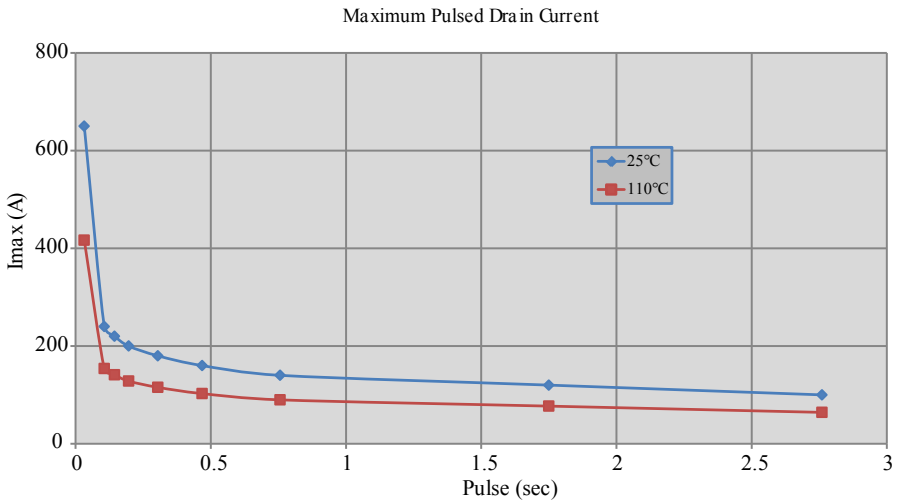


Once the IN_NOT voltage is pulled low, the device is turned ON. The internal charge pump allows the PowerMOSFET gate to rise above the battery voltage to make it function in ohmic region. When IN_NOT is left open, the device is in the OFF state and behaves like a power diode between the source and drain pins.

During a reverse battery polarity event, the charge pump stops operation, causing the PowerMOSFET to switch off. In normal operation, the VN5R003H-E dissipates power given by the battery current multiplied by its $R_{DS(on)}$.

The figure below shows the safe operating area and the maximum pulsed drain current the device can manage during normal operation (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 mm, Copper areas: minimum pad lay-out and 2 cm²)

Figure 20. Maximum current versus duration time of VN5R003H-E



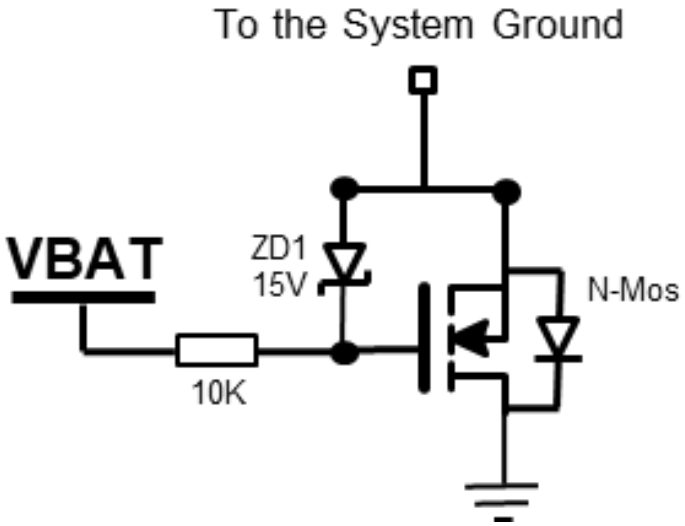
Note:
PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 mm,
Copper areas: minimum pad lay-out and 2 cm²

GAPGCFT00444

The VN5R003H-E can handle ISO 7637-2 2004 pulses with R (IN_NOT) > 5 Ω. Its performance was evaluated using the circuit schematic above.

3.1.1.4 *N-channel MOSFET connected to module ground*

Figure 21. Reverse battery protection with N-channel MOSFET



3.1.1.4.1 Protection behavior

Normal operation (positive battery voltage)

After the power-up phase, when the N channel MOSFET body diode provides the GND to the motor control IC, the zener diode ZD1 plus the resistor will allow to switch on the N-MOSFET.

Reverse battery polarity condition

The N-Channel is switched off since its gate voltage is low; no current can flow in this state.

The series resistor R_g between V_{CC} and N-channel MOSFET gate (10 kΩ in Figure 21. Reverse battery protection with N-channel MOSFET) limits the current through the Zener diode at supply voltages higher than the Zener voltage and limits the charging/discharging current of the gate.

This resistor, together with the gate capacitance of the N-channel Power MOSFET, determines the turn-off time when the module is exposed to fast negative transients or abrupt reverse polarity according to the LV 124: 2009-10 standards.

A good tentative value for R_g could be a few tens of kilo Ohm, considering that a long turn-off time could cause high power dissipation for both the LS and this N-channel Power MOSFET used as reverse battery.

A capacitor, C_g, might be placed between Gate and Source of the N channel Power MOSFET. The RC filter formed by R_g and C_g can be dimensioned to be transparent against the fast negative pulses ISO 7637-2:2011(E) 3a, keeping the reverse polarity protection circuitry switched on.

The time constant (R_gxC_g) must be longer than the pulse 3a length (0.1 µs) but smaller than the pulse 1 length (2 ms).

3.1.1.4.2 External component selection

The zener diode must be dimensioned based on the following considerations:

- V_Z above the nominal battery voltage to avoid high module standby current;
- V_Z must be below the N-Channel PowerMOSFET gate-source voltage absolute maximum rating;
- Power rating enough to handle the current in case of load dump event.

The main PowerMOSFET parameters to be considered are $V_{(BR)DSS}$, V_{gs_th}, $R_{DS(on)}$:

- The N-channel PowerMOSFET breakdown voltage (V(BR)DSS) should be higher than the maximum negative transient peak voltage of ISO 7637:2-2011(E) or its energy capability in avalanche must be high enough to handle the ISO7637/2 pulse 1 level IV energy.
- The maximum gate-source threshold voltage Vgs_th(max) of the N-channel MOSFET must be lower than the minimum battery voltage.

$$V_{gs\_th(max)} < V_{batt(min)} \quad (5)$$

- The N-Channel $R_{DS(on)}$ must be such that power dissipation is kept low enough to ensure that the junction temperature remains below the rated maximum (150 °C).

$$DTj = Tj_{Nch\_max} - T_{amb\_max} = R_{DS(ON)max} * I^2_{motor\_RMS\_max} * R_{thj\_amb} \quad (6)$$

Where:

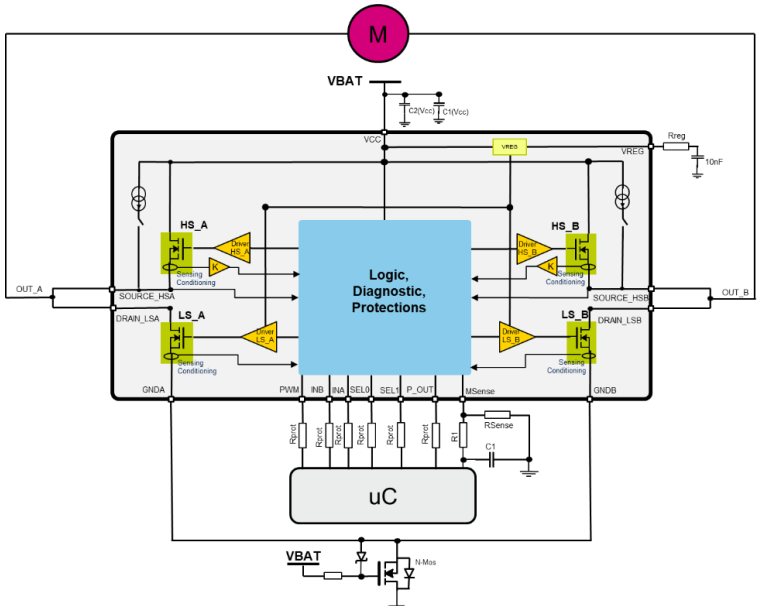
- $T_{amb,max}$ is the maximum ambient temperature.
- $I_{motor\_RMS\_max}$ is the RMS motor current calculated at the maximum battery voltage.

A standard logic MOSFET is normally recommended for noise immunity issue.

3.2 DC motor control application considerations

The typical application schematic of a M0-9 H-bridge is given in the Figure 22. Typical application schematic of a VNH9XXX.

Figure 22. **Typical application schematic of a VNH9XXX**



3.2.1 H-bridge device application considerations

Mechanically commutated motors with brushes (DC motors) are driven by half-bridge or by full-bridge (H-bridge) power switch configurations.

High-current and high-frequency applications like motor control need to address the effect of parasitic inductors.

Inappropriate handling of these inductors can lead to EMC issues (conducted and radiated high RF noise emission), erratic behavior and IC device failure.

Any interconnection inside the device (wire bonding) of the car wiring and in the module (vias, PCB traces) introduces stray inductances. Switching of inductive current causes overvoltage across its terminals as per the formula:

$$VL = -L\frac{dIL}{dt} \quad (7)$$

Where:

- V_L is the voltage across the inductor
- L the inductance itself
- I_L is the current flowing through the inductor

Any high current variation leads to an overvoltage.

Moreover, according to the formula:

$$EL = 0.5LI^2 \quad (8)$$

The inductive component of the motor stores some energy during normal operation. When the motor is stopped, the energy is discharged or transferred to the structures connected to the motor terminals. This energy must be managed to avoid unexpected failure of the structures connected to the inductor.

3.2.2 Design verification checks

3.2.2.1 C1 (V_{CC}) capacitive filter on the supply line

This electrolytic capacitor keeps the voltage ripple at the V_{CC} pin of the IC below a predefined value during operation in PWM at high frequency. This ripple should be kept below 3 V peak to peak.

The capacitive value of an electrolytic capacitor depends on the V_{CC} DC voltage and the ambient temperature.

Capacitor selection must involve consideration of the ESR value, which can degrade the filtering capability of the capacitor if too high. This capacitor must be placed as close as possible to the device V_{CC} and GND pins to minimize trace inductance.

3.2.2.2 *C2 (V_{CC}) capacitive filter on the IC supply line*

This ceramic capacitor must absorb all fast transients between the V_{CC} pin and GND pin. The value can be determined from CISPR25 conducted emission measurements on the battery line.

This capacitor must be placed as close as possible to the IC supply pin (V_{CC}) and ground terminals with minimal PCB trace length to minimize the trace inductance.

3.2.2.3 *Ripple on V_{CC} caused by motor inductance*

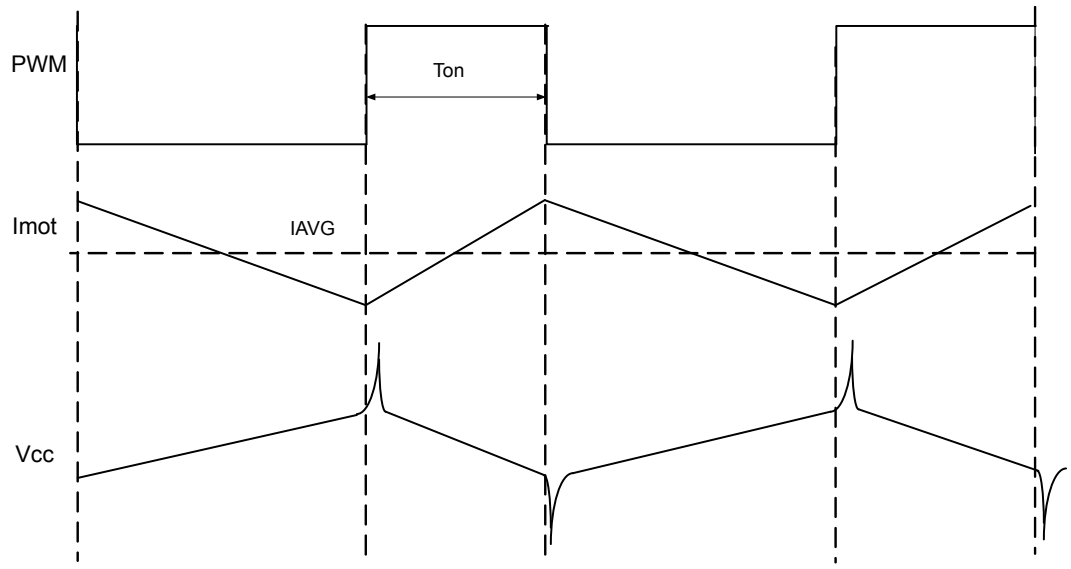
In the steady state with the motor driven by PWM, the motor current is the sum of:

1. An average value (I_{MAVG}) - provided by the car battery
2. A ripple current ($I_{Mripple}$ peak-to-peak) - provided by the bulk capacitor(s) placed across the motor control IC

The battery provides energy to the motor when either HSA /LSB or HSB /LSA are on (T_{on}, on phase of the whole PWM period).

Below are the typical waveforms:

Figure 23. Voltage and current ripple during PWM application



In the following considerations, it is assumed that the motor average current is provided by the battery, whilst the ripple current is provided by the bulk capacitor.

In the worst-case assumption that the system formed by the H-bridge IC and the bulk capacitor is decoupled from the battery by the wire stray inductance, the energy provided by the supply bulk capacitors during Ton is identical to the power provided to the DC motor.

The characteristic equation of a DC motor is:

$$Vbatt = Rmotor*Imotor + Lmotor*\frac{dImotor}{dt} + BEMF = Vmotor,avg + Vmotor,ripple \quad (9)$$

Where:

$$Vmotor,avg = Rmotor*Iavg + BEMF \quad (10)$$

If we neglect the drop on the motor resistance Rmotor in the Equation 7, we derive the following formula:

$$Vmotor,ripple \cong Lmotor*\frac{dImotor}{dt} \quad (11)$$

Therefore, the current ripple during a t_{on} can be simplified according to the following equation:

$$Imotor,ripple = \frac{(Vbatt - Vmotor,avg)}{Lmotor}*Ton \quad (12)$$

Where:

$$Vmotor,avg = \frac{Ton}{T} * Vbatt \quad (13)$$

If we consider a linear increase of the motor current, the charge required by the bulk capacitor to supply the motor is:

$$DQ = 0.5 * Ton * Imotor,ripple \quad (14)$$

At this point, the C(V_{CC}) must be:

$$C1(V_{CC}) > \frac{DQ}{DVcc} \quad (15)$$

This equation helps to define the right C1(V_{CC}) capacitor for the chosen ripple allowed on V_{CC}.

By applying the previous four formulas, we finally derive:

$$C1(V_{CC}) > \frac{0.5 * Ton^2 * Vbatt * \left(1 - \frac{Ton}{T}\right)}{Lmotor * DVcc} \quad (16)$$

The maximum pulse length (T_{on}) is determined by the PWM frequency and duty cycle (in Eq. (15), the maximum C1(V_{CC}) is obtained at 67% duty cycle. The capacitor value in the case of loads which require 20 kHz PWM is relatively low in comparison to the value needed to face other possible applicative conditions described below.

3.2.2.4 *Ripple on V_{CC} caused by stray wiring inductance during sudden current variation*

During motor operation in PWM, the battery current is continuously stopped and restarted.

The ripple on V_{CC} depends on:

- the stray inductance between the IC V_{CC} and the battery itself
- the maximum speed at which the LS is switched on and off
- the maximum motor load current in the worst-case environmental conditions.

The voltage variation across the stray inductance is:

$$DVcc = -L_{stray}\left(\frac{dImotor}{dt}\right) \quad (17)$$

Where L_{stray} is the stray inductance between V_{batt} and device V_{CC} (included any eventual inductance of Pi-filter) and dt is either the t_{fall} or the t_{rise} of the LS working in PWM.

The filtering capacitor on V_{CC} must be dimensioned by taking into account the balance of energy between the one stored in the L_{stray} and the one stored in the C(V_{CC}).

If we consider that the stray inductance energy is transferred instantaneously to the bulk capacitor (thus neglecting the LS switching times), the following equation applies:

$$0.5 * L_{stray} * Imotor^2 = 0.5 * C1(V_{CC}) * DVcc^2 \quad (18)$$

The maximum energy stored in the L_{stray} is reached when the motor is at the Imotor,max.

The transfer of the energy to the bulk capacitor produces an increase in the voltage across the capacitor, its final value must be below the AMR of the device. This condition must be also satisfied at the maximum V_{batt}, therefore:

$$DV_{CC,max} = V_{CC\_AMR} - V_{batt\_max} \quad (19)$$

Where:

- V_{CC_AMR} is given in the datasheet absolute maximum rating table.
- $V_{batt,\ max}$ is the maximum battery voltage

This yields:

$$C1(Vcc) > \frac{L_{stray} * Imotor,max^2}{DVcc,max^2} \quad (20)$$

3.2.2.5 *Ripple on V_{CC} in current switch off due to short to battery and short to ground*

All VIPower H-bridges have the low-side shut-down current (I_{SD_LSD} in datasheets), so in short-circuits to battery, the LS switches off as soon as the LS current reaches the current cut-off value.

Depending on the stray inductance of the short-circuit, the energy stored in it must be dissipated in the structures connected to the stray inductor terminals.

Because of the H-bridge structure, a positive pulse on the LS drain is transferred to the IC supply pin (V_{CC}).

The capacitive filtering on V_{CC} helps to absorb this inductive energy.

Even here, the energy must be balanced:

$$0.5*L_{stray\_sc}*I_{SD\_LSD,max}{}^2 = 0.5*C1(V_{CC})*DVcc,max^2 \quad (21)$$

Where:

- L_{stray_sc} is the short-circuit stray inductance;
- $I_{SD\_LSD,max}$ is the low-side shut-down current;
- $DV_{CC,max} = V_{CC\_AMR} – V_{batt\_max}$ with V_{CC_AMR} representing the absolute maximum rating of the device.

This yields:

$$C1(V_{CC}) > \frac{L_{stray\_sc}*I^2_{SD\_LSD,max}}{DVcc,max^2} \quad (22)$$

The same considerations can be applied in case of short-circuits to ground. In the H-bridge IC, the high-side has both current limitation and thermal shut down features. The worst case energy discharge event is the one that occurs at the maximum current limitation value (I_{LIM_HSD}). The formula is:

$$0.5*L_{stray}*I_{LIM\_HSD,max}{}^2 = 0.5*C1(V_{CC})*DVcc,max^2 \quad (23)$$

Where:

- L_{stray} is the stray inductance from battery to device (included any eventual inductance of pi-filter);
- $I_{LIM\_HSD,max}$ is the maximum high-side current limitation (given in the datasheet);

By imposing that $DV_{cc,max} = V_{cc\_AMR} – V_{batt\_max}$ (V_{cc_AMR} from the datasheet absolute maximum rating table), we derive:

$$C1_{(Vcc)} > \frac{L_{stray}*I^2LIM_{HSD,max}}{DVcc,max^2} \quad (24)$$

3.2.2.6 *Ripple on V_{CC} due to sudden battery disconnection with motor fully energized*

In this condition, the motor energy must be absorbed by the bulk capacitors to avoid reaching the H-Bridge IC breakdown voltage and consequent failure due to excessive energy levels. The applicable formula is:

$$E_{motor} = 0.5*C1(V_{CC})*DV_{CC,max}{}^2 \quad (25)$$

By imposing that $DV_{cc,max} = V_{cc\_AMR} – V_{batt\_max}$ (V_{cc_AMR} from the datasheet absolute maximum rating table), we derive:

$$C1(V_{CC}) > \frac{E_{motor}}{0.5*DV_{CC,max}{}^2} \quad (26)$$

3.2.2.7 *V_{CC} variation because of fast ISO7637/2 ISO transients (pulses 3a, 3b)*

Some reverse battery protection topologies allow transfer of voltage transients directly to device V_{CC}.

The fast transients according to ISO7637/2 are:

- 3a, level IV, max. negative voltage = -220 V, pulse length= 0.1 µs, series resistance= 50 Ω; this pulse causes sudden V_{CC} voltage drop of roughly 100 ns
- 3b, level IV, max. positive voltage = +150 V, pulse length= 0.1 µs, series resistance = 50 Ω; This pulse causes a sudden overvoltage that could trigger the H-bridge IC power clamp in case of no filtering capacitor on the V_{CC} line.

A filtering capacitor $C2_{(VCC)}$ of a few tens of nF is enough to smooth the effect of the above pulses and avoid triggering any protections as well as device malfunction.

3.2.3 Overview of capacitor C1 (V_{CC}) assessment

Table 4. Overview of capacitor C1 (V_{CC}) assessment

Applicative condition	Formula to apply to get C1 (V_{CC})	Applied criteria
Section 3.2.2.3: Ripple on V_{CC} caused by motor inductance	Eq. (15)	DV_{CC} = maximum allowed peak to peak voltage (for example, 3 V)

Applicative condition	Formula to apply to get C1 (V_{CC})	Applied criteria
Section 3.2.2.4: Ripple on V_{CC} caused by stray wiring inductance during sudden current variation	Eq. (20)	L_{stray} is the stray inductance from battery to device (included any eventual inductance of Pi-filter); $DV_{cc,max} = V_{cc\_AMR} - V_{batt\_max}$ (1)
Section 3.2.2.5: Ripple on V_{CC} in current switch off due to short to battery and short to ground	Eq. (22)	L_{stray_sc} is the stray inductance of the short-circuit path (from output to V_{CC}); $I_{SD\_LS,max}$ is the maximum low-side cutoff current (given in the datasheet); $DV_{cc,max} = V_{cc\_AMR} - V_{batt\_max}$ (1)
	Eq. (24)	L_{stray} is the stray inductance from battery to device (included any eventual inductance of Pi-filter); I_{LIM_HSD} is the maximum high-side current limitation (given in the datasheet); $DV_{cc,max} = V_{cc\_AMR} - V_{batt\_max}$ (1)
Section 3.2.2.6: Ripple on V_{CC} due to sudden battery disconnection with motor fully energized	Eq. (26)	E_{motor} is the total energy of the motor (kinetic and inductive). $DV_{cc,max} = V_{cc\_AMR} - V_{batt\_max}$ (1)

Note: *V_{cc_AMR} is given in the datasheet absolute maximum rating table.*

To prevent dangerous overvoltages or undervoltages on the battery connection for the H-bridge, all the above conditions should be fulfilled.

Example: dual washer pump motor driven by VNH9030AQ

During ON state, PWM 20 kHz is applied.

The following VNH9030AQ parameters are applied:

- V_{CC_AMR} = 36 V
- I_{LIM_HSD} = 70 A maximum
- I_{SD_LS} = 84 A maximum
- T_{on}/T=0.67; T_{on} = 33.5 µs

The following DC motor parameters are applied:

- L_{motor} = 550 µH
- I_{motor} = 10 A maximum
- E_{motor} = 23.5 mJ (energy of the motor before battery disconnection)

The following application parameters are applied:

- $V_{batt,min}$ = 7 V
- $V_{batt,max}$ = 26 V (for example jump start)
- DV_{CC} = 3 V (max peak to peak voltage)
- L_{stray} = 5 µH
- L_{stray_sc} = 3 µH

The limitation of V_{CC} ripple during PWM caused by motor inductance Eq. (15) yields:

$$C1(Vcc) > \frac{0.5*Ton^2*Vbatt,max*\left(1-\frac{Ton}{T}\right)}{Lmotor*DVcc} = 2.92\ \mu F$$

Limitation of V_{CC} ripple caused by wiring stray inductance due to sudden current variation Eq. (20) yields:

$$C1(Vcc) > \frac{L_{stray}*Imotor^2}{DVcc,max^2} = 5.0\ \mu F$$

Limitation of V_{CC} peak at LS switch off in the event of short of OUT to battery Eq. (22), yields:

$$C1(Vcc) > \frac{L_{stray\_sc} * I^2_{SD\_LS,max}}{DVcc,max^2} = 211.68\ \mu F$$

Limitation of V_{CC} peak at HS switch off in the event of short of OUT to ground Eq. (24), yields:

$$C1(Vcc) > \frac{L_{stay} * I^2_{SLIM\_HSD,max}}{DVcc,max^2} = 245.0\ \mu F$$

Limitation of V_{CC} peak during sudden battery disconnection with energized motor Eq. (26), yields:

$$C1(Vcc) > \frac{Emotor}{0.5 * DVcc,max^2} = 670\ \mu F$$

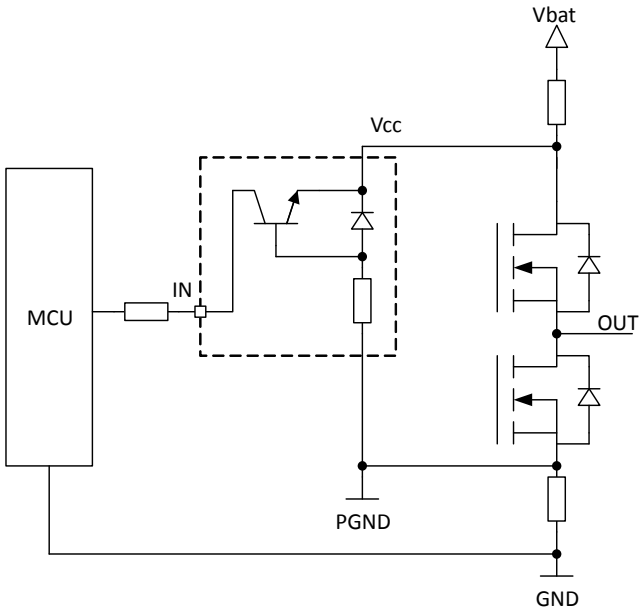
The worst-case condition in this example is the battery disconnection with energized motor, since all other applicative events require a smaller C1(V_{CC}). Every applicative condition, DC motor type and VNH9XX choice should consider the above-mentioned conditions.

3.2.4 Protection resistors (INA, INB, PWM, SEL0 & SEL1)

When negative transients are applied to VCC, the control pins are pulled negative to approximately -2 x Vf ~ -1.5 V where this latter is the voltage drop across the PowerMOSFET antiparallel intrinsic diodes.

During such an event, the npn parasitic bipolar transistor present in each logic pin enters saturation mode (see the following figure).

Figure 24. Simplified internal schematic in negative battery transients



This bipolar saturation current may rise higher than the maximum MCU I/O current and cause MCU failure (latchup event).

VNH9XXX digital input protection resistors (typ. 1 kΩ) are therefore mandatory.

The value of these resistors is a compromise between the current absorbed by the HS I/Os in high logic state and the latch-up limit of microcontroller I/Os:

$$\frac{150V}{I_{latchup}} \leq R_{prot} \leq \frac{V_{OH\mu C,min} - V_{IH,min}}{I_{INHmax}} \quad (27)$$

Where:

- $I_{latchup}$ is the maximum latch-up current of the microcontroller
- $V_{OH\mu C,min}$ is the minimum high state voltage of the microcontroller output
- $V_{IH,min}$ is the minimum input high level voltage of the VNH9XXX (given in the datasheet)
- $I_{INH,max}$ is the maximum input current of VNH9XXX (given in the datasheet)

In summary, the above protection resistors are recommended in case of VNH9XXX failure with potential high voltage in the digital inputs; negative ISO transients (worst case based on the ISO7637/2, ed. 2011 is -150 V) applied to the V_{CC} pin.

This event is heavily influenced by the reverse battery protection topology and it is only applicable when the reverse battery network is connected to the device ground.

3.3 PCB layout considerations

In an H-bridge driver high current paths and low current paths are all near each other. Alternating current (AC) paths carry spikes and noise, high direct current (DC) produces significant voltage drops, and low current paths are sensitive to noise.

We can group the signals thus:

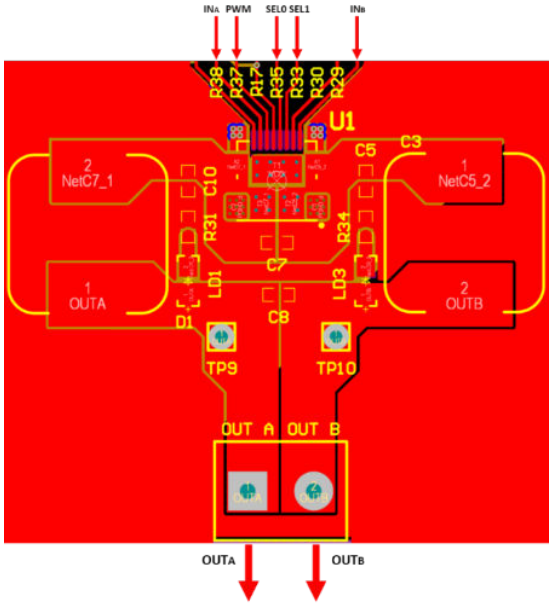
- High frequency and high current (for example, H-bridge outputs);
- Digital at low frequency (INA, INB, SEL0 and SEL1 signals);
- Digital at high frequency (PWM signal).

A PCB floor plan is important to minimize current loop areas and arrange the power components so that the current flows smoothly, avoiding sharp corners and narrow paths. This helps reduce parasitic capacitance and inductance, therefore, eliminating ground bounce.

Another useful procedure to reduce the effect of ground bounce is to connect the several GND planes together applying vias.

Furthermore, in H-bridge drivers it is a good standard to keep the traces of the outputs perfectly symmetrical, so that the intrinsic parasitic effects (resistive, inductive and capacitive) of these paths do not cause ground bounce and therefore lead to incorrect measurements of the output quantities.

Figure 25. Optimized connection between drain LS and source HS and GNDA and GNDB connection (symmetrical connection)



The best performance in terms of parasitic inductance and EMC can be reached with a 3 or 4 layers PCB with a dedicated GND plane that improves filtering efficiency.

All filtering capacitors (mainly C1(V_{CC}) and C2(V_{CC})) must be placed as close as possible to the device terminals to allows keep the parasitic inductance of the PCB-wires as low as possible.

To keep the RF noise from the DC motor low and reach good immunity from ESD, the C(OUT) and C(V_{batt}) capacitors must be placed on the board connector and directly soldered to the module GND usually in star connection with all possible ground signals (Digital GND, analog GND and power GND).

The best ESD performance can be achieved by putting an ESD filtering component like TRANSIL or ceramic capacitor as close as possible to the connector pin and well-grounded via to the ground plane.

A multilayer PCB is better than a 2-layer PCB for heat dissipation. For improved thermal and electrical conduction, a 2 ounces or higher copper thickness may be used in place of the standard 1 ounce.

Figure 26. Proposed schematic for the EV-VNH9xxx boards

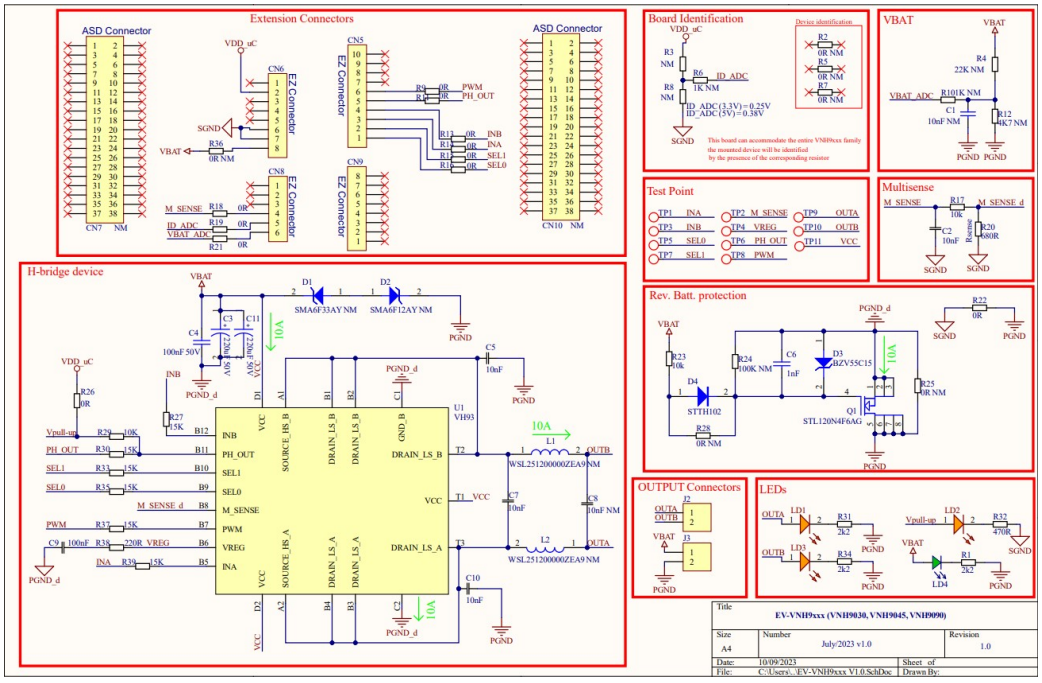
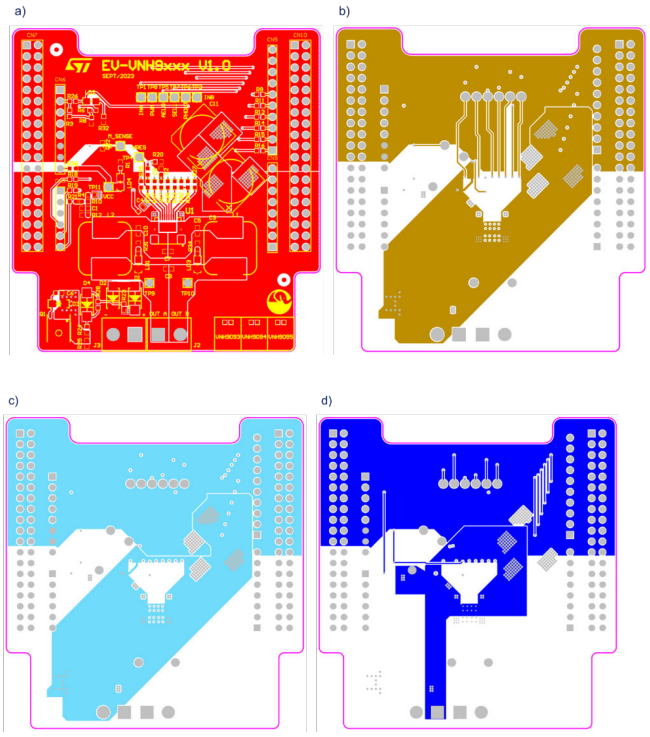


Figure 27. Proposed layout for the EV-VNH9xxx boards



a) top layer, b) layer 1, c) layer 2 and d) bottom layer

4 Load and device compatibility

4.1 Protections summary

4.1.1 High-side Power MOSFET protections

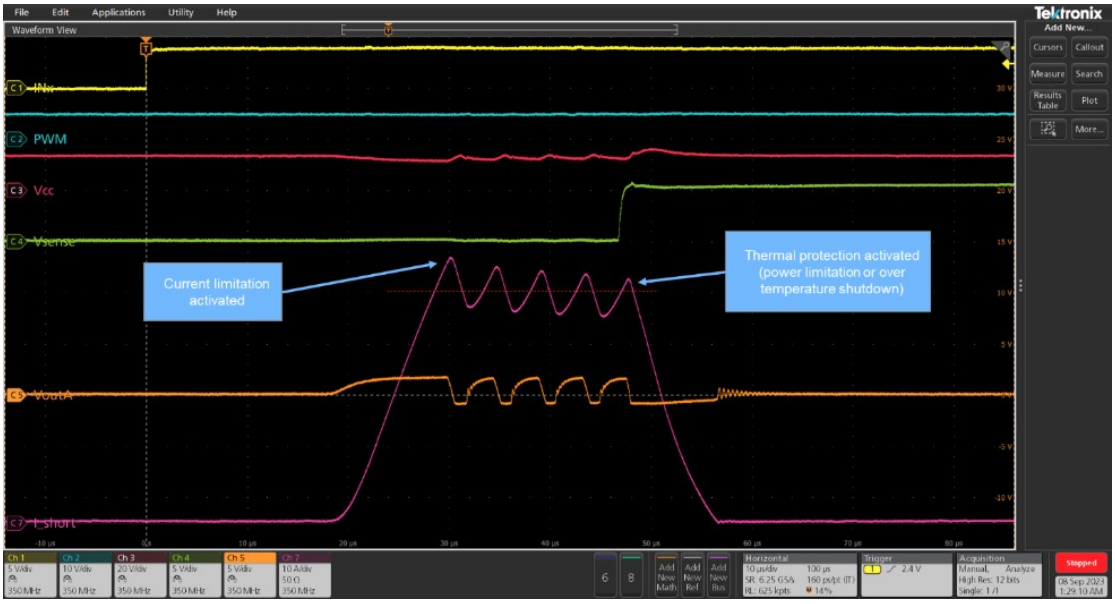
The following embedded protection are implemented to protect the two HS Power MOSFET:

- **Current limitation (I_{LIMH})** – this protection limits the maximum current flowing over the activated Power MOSFET to a safety level.
- **Power limitation** – when the monitored difference between junction and case temperature rises above the threshold, Power MOSFET is shut down.
- **Junction overtemperature** – when the junction temperature (sensor is positioned close to Power MOSFET) threshold is breached, the Power MOSFET is shut down.

The following example depicts motor load switching on the VNH9xxx high-side:

1. the motor inrush current exceeds the threshold limit
2. the high-side Power MOSFET limits the current supplied to the load
3. the high (limited) current flowing though the Power MOSFET increases its temperature to above the threshold
4. a further power limitation or overtemperature protection is triggered
5. the Power MOSFET is deactivated, and fault state is signaled by the V_{SENSEH} level on the MultiSense output

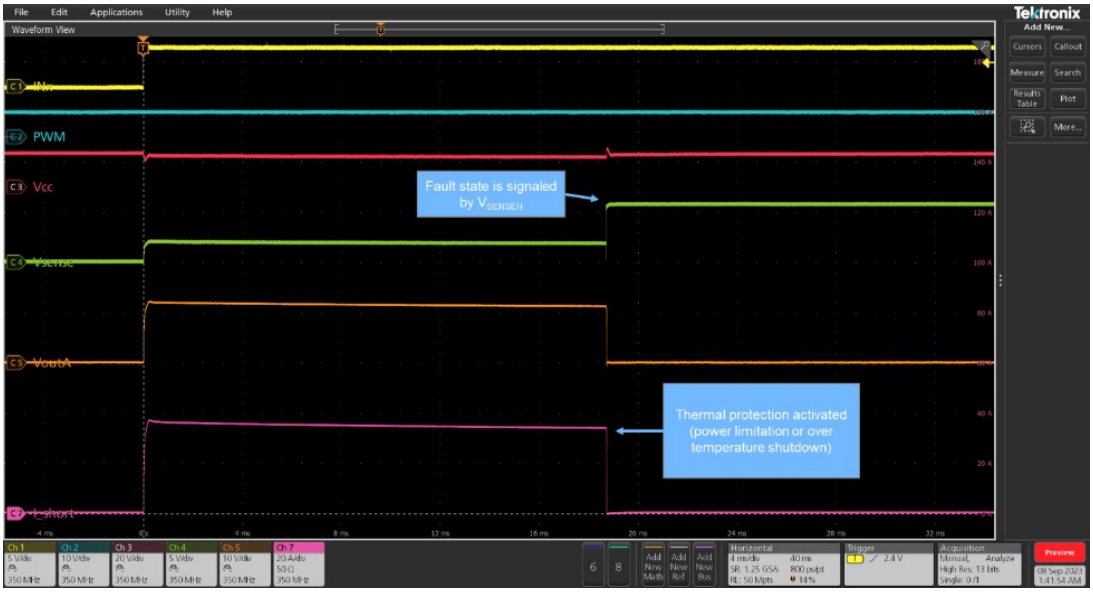
Figure 28. Current limitation on high-side



The next example shows a different case:

1. The current threshold on the high-side Power MOSFET is not reached.
2. The power dissipation on the high-side still triggers the thermal protection triggering.
3. The output is deactivated, and fault state is signaled by V_{SENSEH} level on the MultiSense output.

Figure 29. **Power limitation**



4.1.2 Low-side Power MOSFET protections

The following embedded protection are implemented to protect the two LS Power MOSFET:

1. **Thermal shutdown** – exceeding absolute threshold on junction temperature sensor (positioned close to Power MOSFET) causes low-side Power MOSFET latch off.
2. **Overcurrent detector** – a current exceeding the safety shutdown level (I_{SD_LSD}) flowing through the low-side Power MOSFET causes its latch off.

The following figures show:

1. An overload on the low-side that exceeds I_{SD_LSD} the Power MOSFET is shut down.
2. Thermal protection on low-side.

Figure 30. **Overload on low-side**

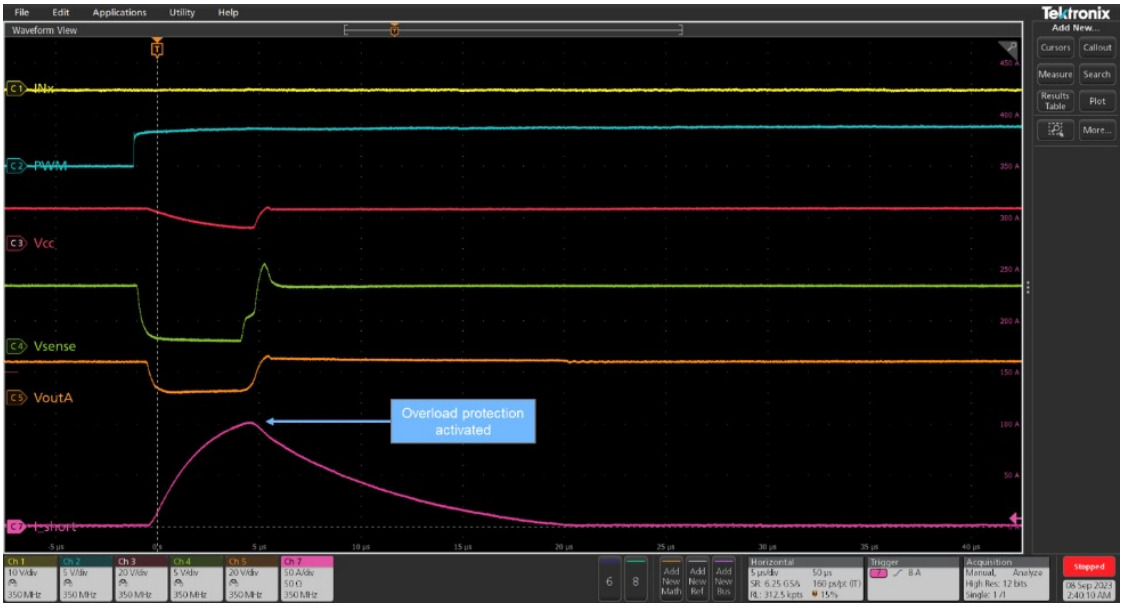
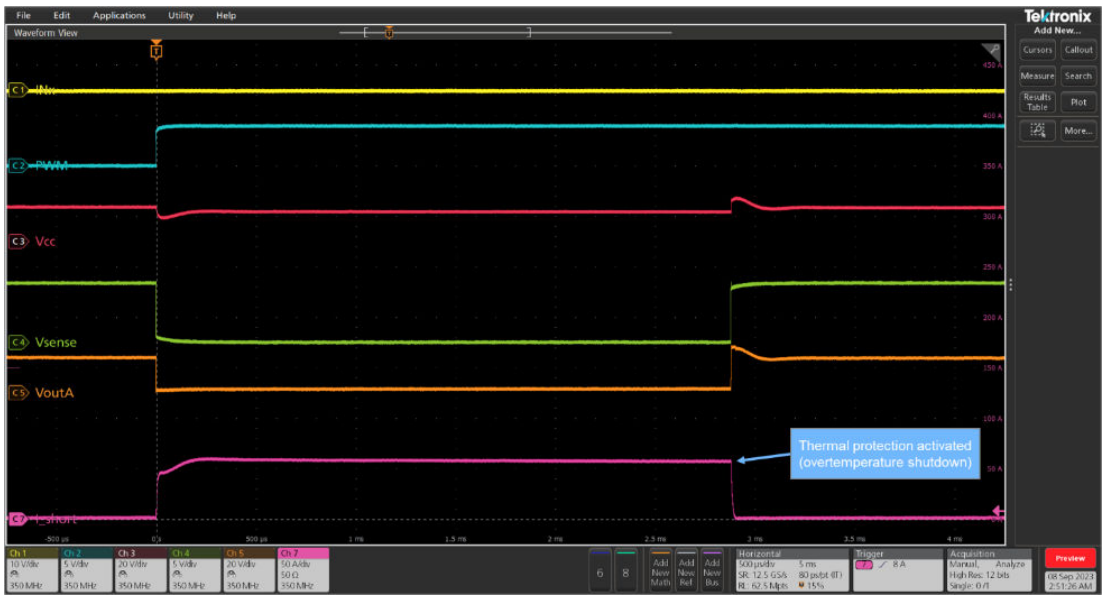


Figure 31. **Thermal protection on low-side**



During the motor inrush and movement phases, none of the protections should be activated. If motor parameters are not compatible with the device and one or more protections are triggered, the device control will be interrupted.

4.1.3 Motor phases and protections

It is possible to individuate 3 different phases during a DC motor activation:

Inrush phase:

During the inrush phase the main parameters to consider are the motor inrush current value and time duration. To proper dimension the application and select the right part number none of the device protection (Power limitation, thermal shutdown and current limitation) should be activated.

During the inrush phase it is possible to limit the inrush current thus obtaining a more moderate motor startup, applying a control of the PWM signal frequency by acting on the PWM input pin of the H-bridge.

Movement phase:

When the motor reaches the movement phase, it typically draws less current than the inrush current. The duration of the movement phase is important because energy dissipated in the high and low-side Power MOSFETs increases overall temperature, which may trigger temperature protections (power limitation or over temperature shutdown).

If speed reduction or regulation is required, a control of the PWM frequency can also be applied (all protections are active during this type of control).

The approximate energy dissipated in the motor driver can be estimated considering the following contributions:

Power dissipation on activated high-side:

$P_{ON}HSW = R_{ON}HS*I_{RMS\_MOT}^2$ (W)

Where:

- $R_{ON}HS$ = static resistance on high-side
- I_{RMS_MOT} = RMS current of activated load (motor)

Power dissipation on activated low-side (active state only while output is driven in PWM mode):

$P_{ON}LS= R_{ON}LS*I_{MOT}^2$ *DutyCycle (W)

Where:

- $R_{ON}LS$ = static resistance on low-side
- I_{MOT} = steady current of activated load (motor)
- DutyCycle = PWM active state of low-side

Switching loss for inductive load on low-side:

Where:

- V_{CC} = power supply voltage
- V_F = high-side free-wheeling diode forward voltage, (Max 0.7 V)
- I_{MOT} = steady current of activated load (motor)
- T_R = datasheet value rise time
- T_F = datasheet value fall time
- F = low-side switching frequency

Power loss in high-side (during free-wheeling):

Where:

- V_F = high-side free-wheeling diode forward voltage typically (0.7 V)
- I_{MOT} = steady current of activated load (motor)
- DutyCycle = PWM active state of low-side

Stall phase:

In the stall phase, the current reaches its maximum level given by the armature winding resistance, leading to increased power dissipation. During this phase, the device is subject to similar stresses as during the inrush phase, so it is desirable to shorten the stall time and thus reduce power dissipation.

It is up to the application to detect stalls (for example, through MultiSense output diagnostics) and turn the outputs OFF.

4.1.4 Other aspects of device and motor load compatibility

To properly match the device with the motor load, additional aspects must be considered:

- In the case of repetitive load activations (for example, door-lock motor control), the number of cycles and the delay between consecutive activations must be considered (influencing the device temperature)
- PWM application influences the inrush current and power loss (switching loss) during activation of the device. A permanent application of PWM at 20 kHz, for example, to modulate the speed, significantly increases the power dissipation in the corresponding low-side as well as in the high-side (due to recirculation of the inductive current in the body diode during OFF state). The PCB layout should be designed to minimize thermal impedance.

ST provide a useful tool to support designers on properly dimensioning the DC motor drivers depending on a specific load profile. The TwisterSIM is a unique electro-Thermal simulator that allows to:

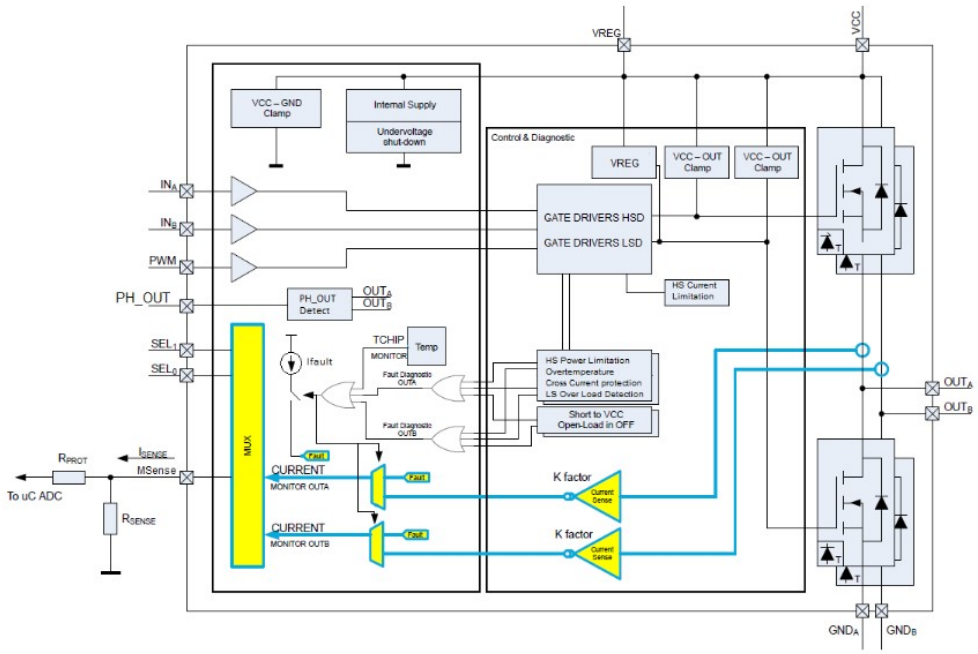
- Perform accurate dynamic simulations of load compatibility.
- Evaluate the impact of fault condition analysis.
- Simulate the diagnostic behavior.
- Simulate dynamic thermal performance
- Optimize wiring Harness

TwisterSIM is available for download at www.st.com/twistersim

5 MultiSense operation

An analog monitoring output called MultiSense is used for M0-9 H-bridge diagnostics. MultiSense pin multiplexes several analogue signals, routed through an analog multiplexer, which is configured and controlled by means of SEL0 and SEL1 pins, according to the address map in Multisense multiplexer addressing table.

Figure 32. M0-9 driver with analog current sense



The following signals are provided through MultiSense pin:

- **Current monitor**: in ON state MultiSense pin delivers a current proportional to the current flowing on the high-side PowerMOSFET (HSA or HSB) according to the selection pin SEL0 (SEL0 = H selects HSA) and SEL1 (SEL1 = H selects HSB). The Sense current is scaled versus the output current as per geometric ratio K (equal to Area_Main_Mos/Area_Sense_Mos). This current can be easily converted into a voltage by using an external sense resistor R_{SENSE}, allowing continuous load monitoring and detection.
- **Chip temperature monitoring**: according to the implemented truth table (SEL0 = SEL1 = H) Multisense pin provides a warning signal when the internal chip temperature Tchip exceed TCASE_Warning (typ. 140 °C). In this case Multisense delivers a current converted into a voltage V_{SENSEH} =R_{SENSE}* I_{SENSEH}. This feedback allows the microcontroller to react before over temperature turn off.
  - **Diagnostic flag in fault conditions**: delivering a current converted to a voltage V_{SENSEH} =R_{SENSE}* I_{SENSEH} in the case of:
    - Fault condition on activated high-side (in ON state) triggered by power limitation, overtemperature protection, where multisense output is selected as per Table 5. Truth table: operative condition and diagnostic to high-side in fault state.
    - Fault condition on activated low-side (in ON state) triggered by overcurrent shutdown, overtemperature protection, where MultiSense output is selected as per Table 5. Truth table: operative condition and diagnostic to the same leg (of high-side) where low-side is in fault state.
    - Short circuit to V_{CC} on OUT in OFF state (INA = INB = PWM = 0).
  - **Diagnostic flag in OFF State:** when output is deactivated (INA = INB = PWM = 0) the diagnostic is performed by reading the MultiSense output (V_{SENSEH} or HIZ). The output to be monitored and internal pull-up are selectively switched trough SEL0 and SEL1 as per Table 5. Truth table: operative condition and diagnostic. It allows to detect short to V_{CC} or open-load conditions before starting the motor (see Section 6: OFF state diagnostic)

The different modes of the MSense pin are given in combination with the other inputs of the device as shown in the Table 5. Truth table: operative condition and diagnostic:

Table 5. Truth table: operative condition and diagnostic

SEL0	SEL1	INA	INB	PWM	HB status	PH_OUT	Multisense	Diagnostic multisense = V_{SENSEH}	Comments
1	0	1	0	1	Clock	MONITOR A	Current sense ON HSA	ON state HSA protection triggered, HSA latched off	
		0	1	1	Counterclock	MONITOR A	HIZ	ON state LSA protection triggered, LSA latched off	
		1	1	0	BRAKE V_{CC}	MONITOR A	Current sense ON HSA	ON state HSA protection triggered, HSA latched off	
		0	0	1	BRAKE GND	MONITOR A	HIZ	ON state LSA protection triggered, LSA latched off	
		1	0	0	HSA ON	MONITOR A	Current sense ON HSA	ON state HSA protection triggered, HSA latched off	
		0	1	0	HSB ON	MONITOR A	HIZ		
		0	0	0	OFF	MONITOR A	HIZ	V_{OUTA} > V_{OL}: NO open-load in full bridge configuration, OUTA shorted to V_{CC} in half bridge configuration	Pull up on OUTB - diagnostic in off state
		1	1	1	BRAKE V_{CC}	MONITOR A	Current sense ON HSA	ON state HSA protection triggered, HSA latched off	
0	1	1	0	1	Clock	MONITOR B	HIZ	ON state LSB protection triggered, LSB latched off	
		0	1	1	Counterclock	MONITOR B	Current sense ON HSB	ON state HSB protection triggered, HSB latched off	
		1	1	0	BRAKE V_{CC}	MONITOR B	Current sense ON HSB	ON state HSB protection triggered, HSB latched off	
		0	0	1	LSB ON/ LSA OFF	MONITOR B	HIZ	ON state LSB protection triggered, LSB latched off	Half bridge on LSB - Pull up on OUTB
		1	0	0	HSA ON	MONITOR B	HIZ		
		0	1	0	HSB ON	MONITOR B	Current sense ON HSB	ON state HSB protection triggered, HSB latched off	
		0	0	0	OFF	MONITOR B	HIZ	V_{OUTB} > V_{OL}: NO open-load in full bridge configuration, OUTB shorted to V_{CC} in half bridge configuration	Pull up on OUTA - diagnostic in off state
		1	1	1	BRAKE V_{CC}	MONITOR B	Current sense ON HSB	ON state HSB protection triggered, HSB latched off	
1	1	1	0	1	Clock	MONITOR A	HIZ	TCHIP WARNING	

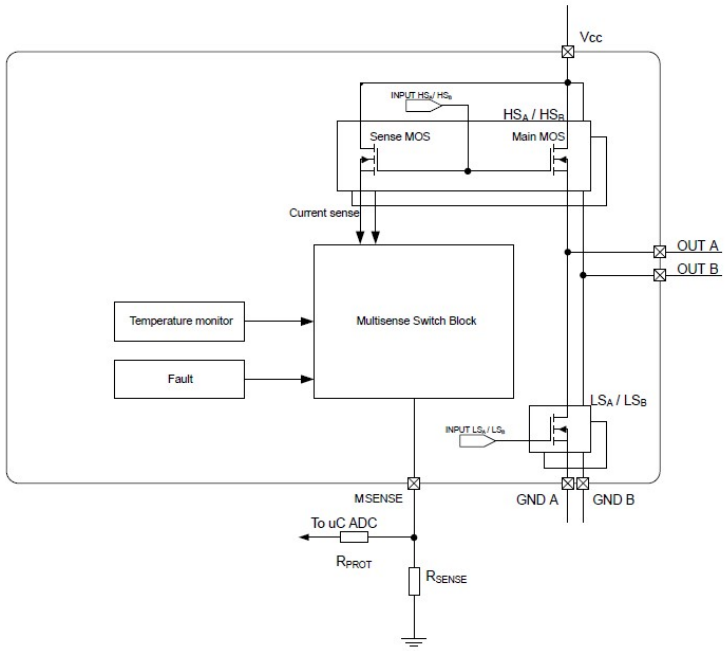
SEL0	SEL1	INA	INB	PWM	HB status	PH_OUT	Multisense	Diagnostic multisense = V_{SENSEH}	Comments
1	1	0	1	1	Counterclock	MONITOR A	HIZ	TCHIP WARNING	
		1	1	0	BRAKE V_{CC}	MONITOR A	HIZ	TCHIP WARNING	
		0	0	1	LSA ON/LSB OFF	MONITOR A	HIZ	ON state protection triggered, LSA latched off	Half bridge on LSA - Pull up on OUTA
		1	0	0	HSA ON	MONITOR A	HIZ	TCHIP WARNING	
		0	1	0	HSB ON	MONITOR A	HIZ	TCHIP WARNING	
		0	0	0	OFF	MONITOR A	HIZ	Full bridge configuration: OUTA shorted to V_{CC}, $V_{OUTA} > V_{OL}$	
		1	1	1	BRAKE V_{CC}	MONITOR A	HIZ	TCHIP WARNING	
0	0	1	0	1	Clock	MONITOR B	HIZ		
		0	1	1	Counterclock	MONITOR B	HIZ		
		1	1	0	BRAKE V_{CC}	MONITOR B	HIZ		
		0	0	1	BRAKE GND	MONITOR B	HIZ	ON state LSB protection triggered, LSB latched off	
		1	0	0	HSA ON	MONITOR B	HIZ		
		0	1	0	HSB ON	MONITOR B	HIZ		
		0	0	0	STAND BY	HIZ	HIZ		
		1	1	1	BRAKE V_{CC}	MONITOR B	HIZ		

Note: In brake to GND condition (INA = INB = L, PWM = H) settling the pin SEL1 = 1 AND SEL0 = 0 or SEL1 = 1 AND SEL0 = 1 it is possible to keep one of the two leg in high-Z for half bridge configuration and diagnostic.

Note: When INA = INB = PWM = SEL0 = SEL1 = 0 the device enters in standby after TDSTBY

5.1 Current sense monitor - principle of MultiSense signal generation

Figure 33. **Structure of MultiSense signal generation**



In general, the MultiSense output signal operates for V_{CC} < 18 V. During normal operation and no fault conditions (V_{OUT} > V_{OUT_MSD}= 5 V typ), the current flowing through the main high-side MOSFET is mirrored through Sense-MOSFET. The Sense-MOSFET is a scaled down copy of the main MOSFET according to a defined geometric ratio. The current is passed through the MultiSense switch block, fully decoupling the MultiSense signal from the output current. The current sense ratio is selected to have a sense current I_{SENSE}=450 µA when the load current reaches its typical value (Iload = Inominal, for example, Iload = 5 A in VNH9030AQ) that can be easily converted into a voltage by using an external sense resistor V_{MSENSE}=R_{SENSE}* I_{SENSE}.

When the device is in ON state, whenever a protection is triggered and the device is in current mode, the internal logic sets the MultiSense output in fault mode, disabling the current monitor circuit and providing a particular internal signal which activates a current generator. In fault condition the Multisense pin supplies a current I_{SENSEH} (typically 8 mA), that can be easily converted into a voltage by using an external sense resistor R_{SENSE} (V_{SENSEH} =R_{SENSE}* I_{SENSEH}); for example, with R_{SENSE} = 0.7 kΩ, V_{SENSEH} voltage is equal to 5.6 V. The maximum voltage on MSense pin is clamped by the ESD protection structure of the pin itself (typically 8.5 V).

The output MultiSense current limitation (Isense_sat) is defined as the highest sense output current the linear relationship I_{SENSE} = I_{OUT}/K is valid at, and it is due to the current output stage power limit.

5.1.1 Normal operation (at least one HS active with corresponding diagnostic through SEL0/1 selected)

When device is operating in normal conditions (no fault intervention), the Multisense pin provides a current proportional to I_{OUT} as per the following equation:

current provided by MultiSense output

$$I_{SENSE} = \frac{I_{OUT}}{K} \quad (28)$$

Hence, connecting a resistor R_{SENSE} to Multisense the current can be converted to a voltage V_{SENSE} as per:

where:

- V_{SENSE} is the voltage measurable on R_{SENSE}
- I_{SENSE} is the current provided from MSense pin in current output mode
- I_{OUT} is the current flowing in the selected high-side
- *K* factor represents the ratio between Power MOSFET cells and sense MOS cells. Its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE}.

The MultiSense IP block has been properly designed to keep the linearity in the whole operating current range.

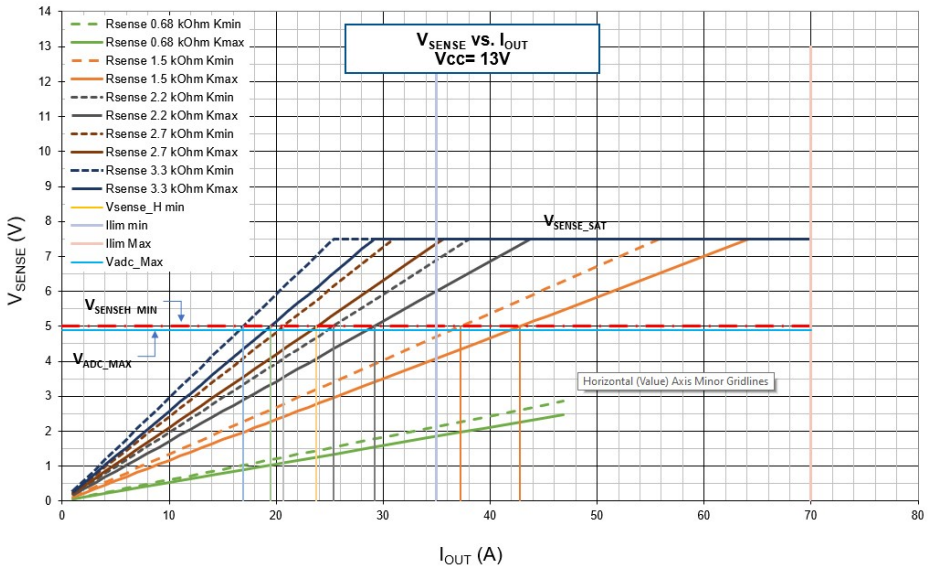
5.1.2 MultiSense voltage saturation

In current sense mode the MultiSense pin has an intrinsic voltage dynamic range that depends on V_{CC} battery voltage. When the MultiSense pin exceeds the V_{SENSE_SAT} value, the current sense loose its linearity behavior and saturates. At V_{CC}=13 V , V_{SENSE_SAT} value is typically ≈ 7.5 V , while the minimum $V_{SENSE_SAT}$is 4.8 V at V_{CC}= 7 V and T_J = -40 °C (defined V_{SENSE_SAT} min. in VNH9x datasheets).

It is fundamental to proper dimensioning the R_{SENSE} value to ensure linearity over the load current range (see Section 5.1.3: Dimensioning the R_{sense} resistor).

A proper R_{SENSE} dimensioning is fundamental to optimize the range of linearity (depending on load profile), optimize the microcontroller ADC range and to properly discriminate a fault condition (V_{SENSE} < V_{SENSEH} in all load conditions).

Figure 34. V_{SENSE} saturation vs I_{LOAD} and R_{SENSE}



The figure above shows the V_{SENSE} behavior for several values of R_{SENSE}, these results represent a real case performed at bench test. Thanks to the high values of K factor, for a battery voltage V_{CC}=13 V, the V_{SENSE_SAT} value is generally higher than the minimum current limitation $ILIM_{MIN}$=35 A (as per datasheet). Hence, for a proper dimensioning at V_{CC}=13 V must be care more focus on $ILIM_{MIN}$.

5.1.2.1 *Maximum output current vs R_{SENSE} and voltage saturation*

This section shows how dimensioning the R_{SENSE} to optimize the multisense working in linear region. R_{SENSE} value will be the right compromise between the I_{OUT_MAX} and the V_{SENSE} in normal current load conditions.

Indeed, as shown in Figure 34. V_{SENSE} saturation vs I_{LOAD} and R_{SENSE}, an higher R_{SENSE} value will reduce the maximum I_{OUT} that can be properly sensed. On the other hand, a lower value of R_{SENSE} will provide a smaller ADC range voltage in normal load conditions. Below example 1 provide a real case of study.

Example 1:

Considering the VNH9030AQ the target is to dimension the R_{SENSE} in order to have V_{SENSE} = 1.2 V at $I_{NOMINAL}$ = 5 A.

Considering a typical value K_2 @ 5 A = 12000, the typical I_{SENSE} will be 416 µA and hence R_{SENSE} = V_{SENSE} / I_{SENSE} ≈ 2.7 kΩ

As shown in Figure 34. V_{SENSE} saturation vs I_{LOAD} and R_{SENSE}, at V_{CC} =13 V for such value of R_{SENSE}, the VNH9030AQ will reach the saturation voltage V_{SENSE_SAT} for I_{LOAD} > 30 A that is fairy near to min value of I_{LIM}. While, assuming a worst condition at V_{CC}=7 V and T_J = 150 °C, the minimum V_{SENSE_SAT} is 4.8 V (see datasheet),in this case the maximum linear sense current I_{SENSE} will be 1.78 mA (=4.8 V / 2700 Ω).

This means that, fixing R_{SENSE} =2.7 kΩ, it is guaranteed a linear current sense mode up to I_{OUT} = 1.78 mA * 12000 ≈ 21 A in whole temperature range and for battery up to 7 V.

5.1.3 Dimensioning the R_{sense} resistor

In this chapter will be explained the strategy for a proper R_{SENSE} dimensioning, allowing the controller a complete monitoring of the system. The target is to detect the three main functional states:

- Normal operation: where MSense operates in linear region.
- Stall/inrush current: where MSense could operates in linear region or V_{SENSE_SAT}, limited by I_{LIM}.
- Fault Detection: where MSense is clamped to V_{SENSE_H}.

In normal operating conditions, the current sense will work in linear region as per the following equation :

$$V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot \frac{I_{OUT_{NOM}}}{K}\left(V\right) \quad (29)$$

The sense resistor value can be calculated to optimize the ADC Voltage range with the load has nominal current.

Moreover, in order to allow correct fault detection, it is important that V_{SENSE} could be distinguished by a fault state V_{SENSEH_MIN}=5 V (as per datasheet) in any working condition (also during motor stall or Inrush phase).

This means that:

$$V_{SENSE\_MAX} < V_{SENSEH_{MIN}} = 5V \quad (30)$$

Depending on R_{SENSE} dimensioning, the max value of V_{SENSE} (V_{SENSE_MAX}) could be in linear region or in Saturation V_{SENSE_SAT}.

$$V_{SENSE\_MAX} = V_{SENSE_{SAT}} or V_{SENSE\_MAX} = R_{SENSE} \frac{K_{MIN}}{I_{OUT\_MAX}} \quad (31)$$

The Figure 34. V_{SENSE} saturation vs I_{LOAD} and R_{SENSE} is an important tool to properly dimension the R_{SENSE} based on Nominal Load, Stall current, taking into account also the maximum ADC dynamic V_{ADC_MAX} and the minimum value of V_{SENSEH}.

In the Figure 34. V_{SENSE} saturation vs I_{LOAD} and R_{SENSE} it is possible to distinguish the following regions:

- a linear region that is upper limited by V_{SENSE_SAT}, where MSense operates in normal operation, this is limited on the right side by I_{LIM}
- a fault region that is represented by the V_{SENSE_H}
- a maximum voltage range of the ADC, that is 100 mV below V_{SENSEH_MIN}, to distinguish between a current overload and a fault condition. This also allows the full scale voltage of the ADC to be exploited almost completely, under normal current load conditions.

As per Figure 34. V_{SENSE} saturation vs I_{LOAD} and R_{SENSE}, depending on R_{SENSE} value, V_{SENSE_SAT} condition could not occur, since reached for I_{OUT} values equal or higher than I_{LIMmin}. Another value to take into account is the maximum ADC dynamic (a proper value could be V_{ADC_MAX} =4.9 V). Another option could be settling V_{SENSE_MAX} as the minimum value of V_{SENSE_SAT}= 4.8 V (at V_{CC}=7 V and T_J = 150 °C). Fixing a V_{SENSE_MAX}=4.8 V in linear condition will guarantee a proper detection of a Fault in all operating conditions up to V_{CC}= 7 V. Hence

$$R_{SENSE} < V_{SENSE\_SAT\_MIN} \cdot \frac{K_{3\_MIN}}{I_{OUT\_MAX}} \quad (32)$$

where:

- V_{SENSE_MAX} chose as per worst condition $V_{SENSE\_SAT\_MIN}$ = 4.8 V.
- I_{OUT_MAX} is the maximum load current flowing in the selected high-side (for example, the motor stall current).

K_{3_MIN} factor represents the minimum K factor value at high current.

Finally, the current sense resistor must protect the MSense pin in case of reverse battery event. During this event, two antiparallel intrinsic diodes between MSense and V_{CC} pins are biased, one in forward (with $V_F \approx 0.7$ V) and one in breakdown reverse (with $V_{BR} \approx 4$ V), and the resulting current must be limited. This I_{SENSE} AMR value is 20 mA for VNH9030AQ, therefore the minimum R_{SENSE} to protect the MSense pin in case of reverse battery (supposing a static condition of V_{CC} = -16 V) is:

$$R_{SENSE} > \frac{-V_{CC} - (V_F + V_{BR})}{I_{MSENSE\_REV\_AMR}} = \frac{16V - (0.7V + 4V)}{20mA} = 565\ \Omega \quad (33)$$

In conclusion the R_{SENSE} must therefore fulfill the two conflicting conditions to ensure a proper fault detection and to protect the MSense pin in case of reverse battery event.

5.1.3.1 *R_{sense} calculation example*

In this example the R_{SENSE} is dimensioned for the VNH9030AQ device at the nominal battery voltage V_{CC} = 13 V.

The following VNH9030AQ parameters or assumptions are applied:

- V_{CC} = 13 V
- V_{SENSE_SAT} = 7.5 V
- V_{SENSEH_MIN} = 5 V
- K_{3_MIN} = 11160, K_{3_MAX} = 12840 and assuming that K_3 remains constant at higher current
- $I_{NOMINAL}$ = 5 A

Additionally, the following uC and load parameters are applied:

- V_{ADC_MAX} = 4.9 V (i.e. the maximum operating range of the ADC. A margin of 100 mV below V_{SENSEH_MIN} is selected to discern between a current overload and a fault condition).

Finally, the following DC motor load parameters are applied:

- I_{OUT_MAX} = 20 A (the motor stall current).

Looking at the Figure 34. V_{SENSE} saturation vs I_{LOAD} and R_{SENSE} settling a R_{SENSE} = 2.7 kΩ will allow to distinguish between normal current operation, overcurrent and fault condition, ensuring linearity in the whole load current range to be monitored and properly exploiting the full scale voltage of the ADC.

R_{SENSE} can be dimensioned also applying Eq. (32) to Eq. (33).

Since $V_{ADC\_MAX} < V_{SENSEH\_MIN}$ and $V_{ADC\_MAX} < V_{SENSE\_SAT\_MIN}$, the Eq. (32) can be applied:

$$R_{SENSE} < V_{ADC\_MAX} \cdot \frac{K_{MIN}}{I_{OUT_{MAX}}} = 4.9V \cdot \frac{11160}{20A} \cong 2734\ \Omega$$

$$R_{SENSE} > \frac{-V_{CC} - (V_{CC} + V_{BR})}{I_{MSENSE\_REV\_AMR}} = \frac{16V - (0.7 + 4)}{20mA} = 565\ \Omega$$

Hence the chosen sense resistor of 2.7 kΩ is appropriate.

5.1.4 Impact of output voltage on MultiSense output

Current sense operation for load currents nearing limit thresholds is not guaranteed or predictable. Indeed, the current limiter can cause the output voltage to drop significantly, down to almost 0 V in the event of a hard shortcircuit.

As the whole circuit is referenced to V_{OUT}, ambiguous and unreliable current values could derive from the MultiSense under such conditions.

To bring the MultiSense to a defined state, a dedicated circuit section shuts down the current sense circuitry when V_{OUT} drops below the V_{OUT_MSD} threshold (typically 5 V).

Therefore, in normal operation, current sense works properly inside the defined border conditions.

5.1.5 MultiSense fault flag indication

In case of faults detected in ON or OFF state, the MultiSense pin is pulled up to the V_{SENSEH} level, by properly selecting SEL0 and SEL1 indicating the Power MOSFET protected.

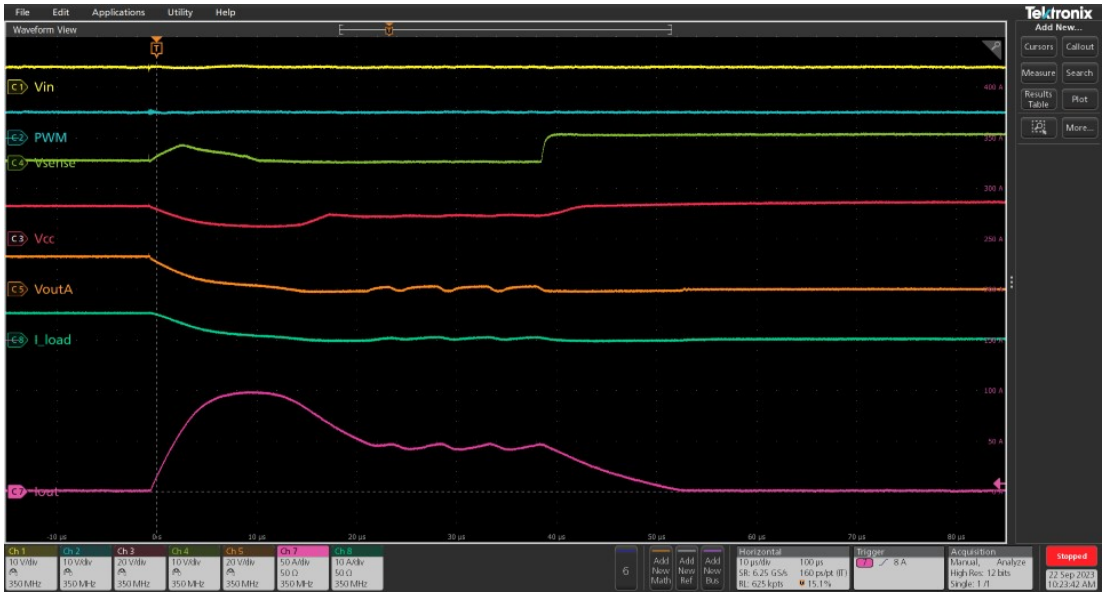
The conditions causing faults can be:

- Activated high-side: power limitation protection, junction temperature exceeding overtemperature threshold or short-circuit to GND.
- Activated low-side: cut-off current protection ($I_{OUT} > I_{SD\_LS}$) or junction temperature exceeding overtemperature shutdown threshold.
- In OFF state (INA = INB = PWM = L) voltage on OUT pin exceeds V_{OL} threshold.

Under this condition the current capability of MultiSense is regulated to I_{SENSEH} (given in the datasheet Typ 8 mA). Hence it is important to set properly the R_{sense} (see Section 5.1.3: Dimensioning the R_{sense} resistor) to allow a proper voltage setting of V_{SENSEH} to distinguish V_{SENSEH} vs. normal operation (with nominal, inrush or stall current).

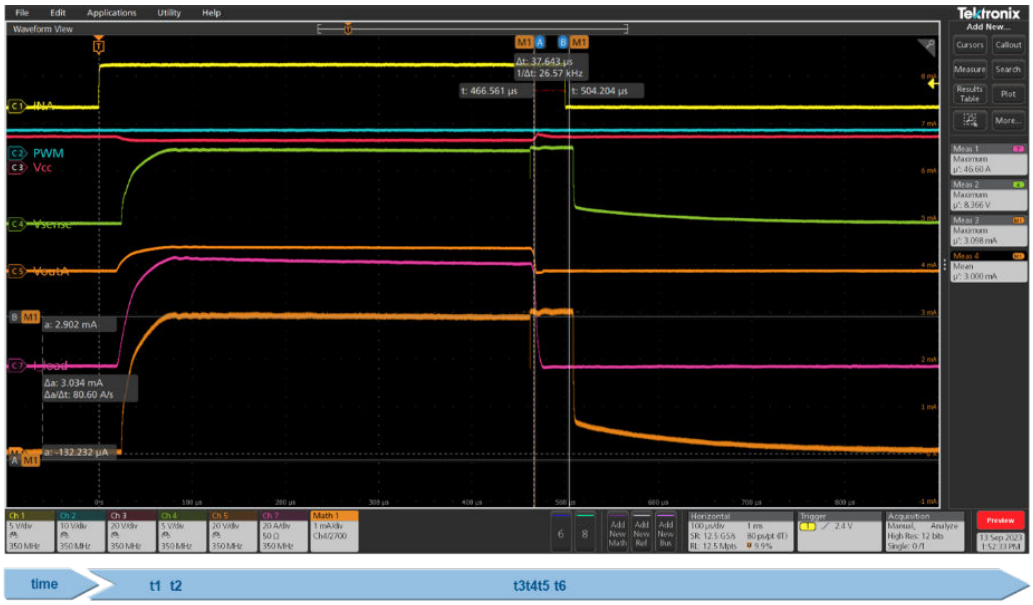
The Figure 35. Hard short-circuit on OUTA to GND shows the typical behavior of a VNH9030AQ in a hard short-circuit on OUTA to GND (INA = H, INB = L, PWM = H):

Figure 35. Hard short-circuit on OUTA to GND



The example of the figure below shows the VNH9030AQ in a condition with progressively increasing output current (single shot ramp) supplied by an electronic load. The MultiSense current monitors the increasing load until the device is latched off due to thermal protection. (R_{sense}= 2.7 kΩ).

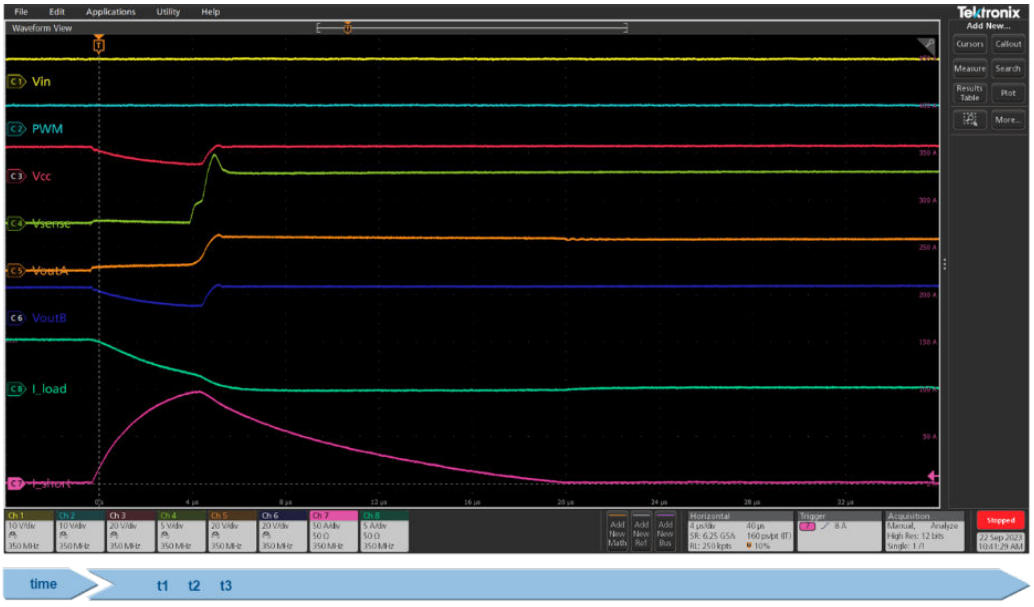
Figure 36. **Single shot ramp on OUTA**



1. *The saturation voltage V_{SENSE_SAT} is reached at about 40 A current.*
2. *The I_load rises until it reaches the threshold current limitation ILIM_H.*
3. *The thermal protection is triggered (power limitation, or the overtemperature shutdown).*
4. *When the output voltage drops below approximately 5 V (V_{OUT_MSD} in datasheet) the MultiSense pin goes in high impedance, until the first thermal protection is activated.*
5. *the MultiSense pin is then reactivated and the V_{SENSEH} voltage is issued and latched until INA remains active, high-side HSA is kept deactivated.*

The third example depicts output short-circuit to V_{CC} on activated low-side driver on OUTA (INA=L INB=H and PWM=H.

Figure 37. **Short-circuit to V_{CC} on OUT**



1. The current exceeds the shutdown threshold $I_{OUT} > I_{SD\_LS}$ or the junction temperature exceeds the overtemperature shutdown level.

2. The relevant driver is latched off.
3. V_{SENSEH} is signaled by the MultiSense output.

5.1.6 Latching and unlatching conditions

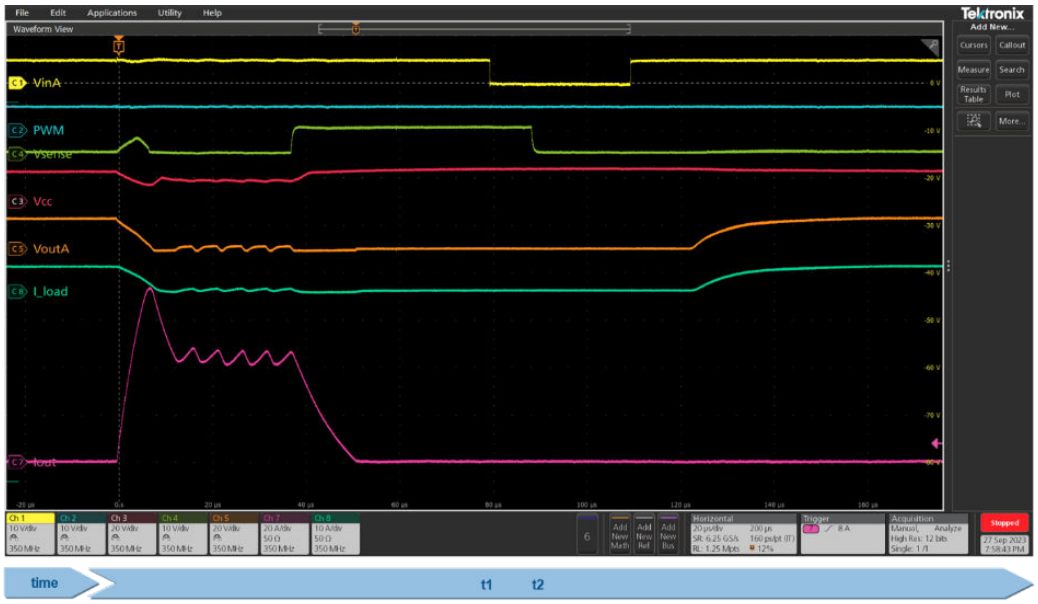
Latching conditions

In case of fault conditions, the corresponding leg is disabled (OUTA or OUTB are in high impedance). Properly selecting SEL0 and SEL1 pin and monitoring the MultiSense pin, it is possible to evaluate the latch off state for each high or low-side PowerMOSFET protected. The device will remain in fault status, MultiSense output equal to V_{SENSEH} and latch off condition, until unlatching procedure is performed to clear the fault of the latched side and restart it.

Unlatching conditions

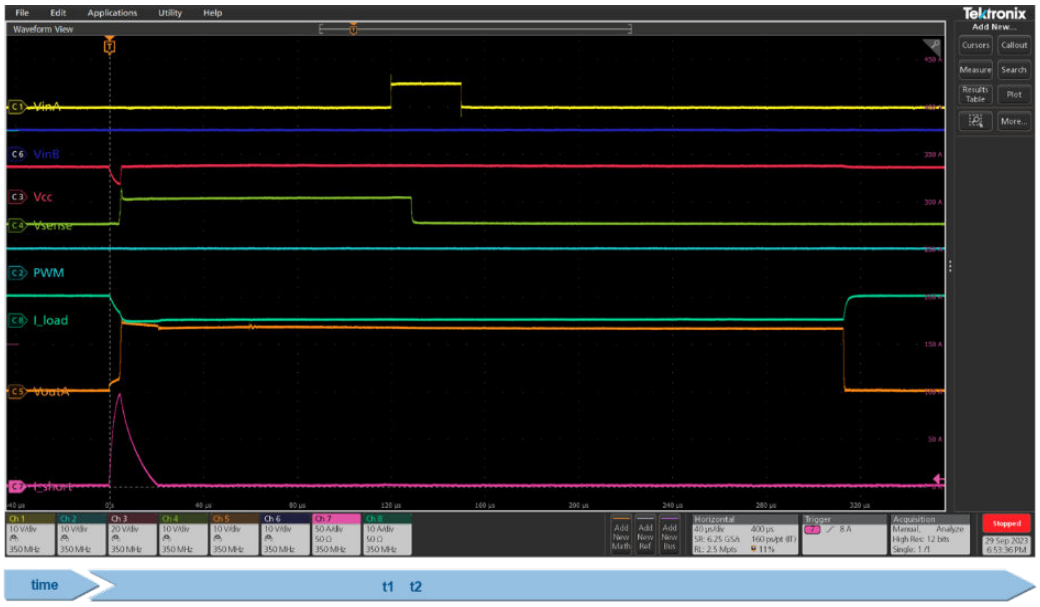
High-side driver: to unlatch the high-side driver after a latch off condition, the related input pin (INA or INB) must be settled low for a minimum time t_{LATCH_RST}. Then the device can be reactivated (by setting INA or INB high). In Figure 38. Unlatching sequence on HS is showed the unlatched high-side procedure

Figure 38. Unlatching sequence on HS



Low-side driver: to unlatch the low-side driver after a latch off condition, the related input pin (INA or INB) must be settled high for a minimum time t_{LATCH_RST}. After such period it is possible to set again INA or INB to low level re-activating the device.

Figure 39. **Unlatching sequence on LS**



5.1.7 Entering standby mode after an OVL event

To enter standby after a fault event, all input pins must be set to low level for a minimum time frame t_{D_SDBY} (from when the last input pin is set to low).

Suppose that a high-side driver (for example HSA) is latched in normal operation. To leave its latch off condition, INA is set low for t_{LATCH_RST}. This unlatches the high-side driver and satisfies the precondition of all INA or INB low. The device enters standby mode after t_{D_stby}.

Another scenario is when the low-side driver is latched (for example, LSB). To clear the latch off condition, the INB signal must be set from low to high. After all the input pins are set to low again, the device enters standby mode after t_{D_stby}.

Note: To exit standby, it is sufficient to set one of the input pins (INA, INB, PWM, MultiSense_EN, SEL0, SEL1) from low to high. It is recommended to set the PWM from low to high after any of the other input pins after a minimum 20 µs delay (to avoid overstressing the low-side if there is a short-circuit between output and V_{CC}).

6 OFF state diagnostic

In OFF state (INA=INB=PWM=0 and SEL0 or SEL1 selectively high) it is possible to detect the condition of open load, short to V_{CC} or short to GND.

By selecting SEL0 and SEL1 as per Table 5. Truth table: operative condition and diagnostic, each OUT can be monitored and compared with an internal voltage reference V_{OL}. A properly dimensioned pull-up / pull-down network is embedded inside the device and automatically connected when needed. The device will provide feedback on MultiSense pin: if $V_{OUTx} > V_{OL}$ the MultiSense will be settled to V_{SENSEH}. Thanks to OFF-state diagnostic it is possible to perform a complete diagnostic when the motor is OFF and to ensure a safe start up sequence.

The following plots show the delay times for the OL detection in OFF state vs settings of INA / INB and SELx. The relevant delay time t_{DSTKON} and t_{D_VOL} are given in the datasheets.

To proper perform OFF state diagnostic it must be assured that the device does not enter Stby before ended the task. T_{DSTKON} is defined as the minimum delay time after that the INA and INB pins (considering that PWM is already low) are set too low so that the device can give a valid indication of the OFF state diagnostic.

Figure 40. Principle of open load / short to V_{CC} detection in OFF state - delay after INA or INB is set from high to low

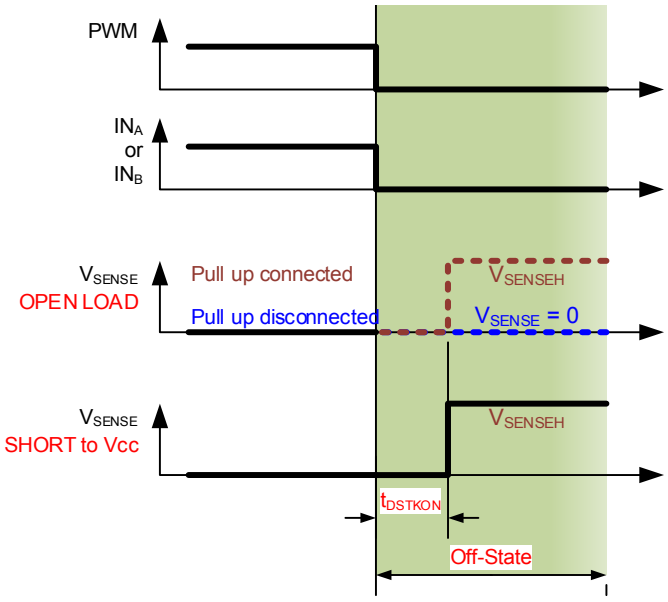


Figure 41. **Principle of open load / short to V_{CC} detection in OFF state - delay after INA or INB is set from high to low**

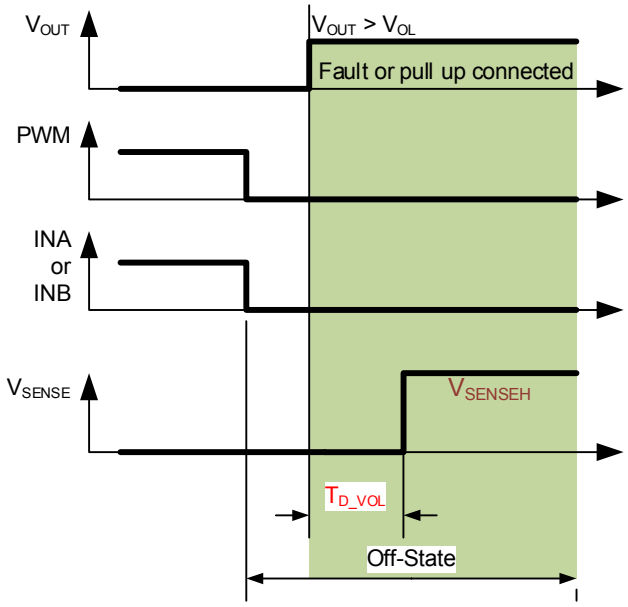


Figure 42. **Principle of open load / short to V_{CC} detection in OFF state - delay after all control signals are set low (enter stand-by mode)**

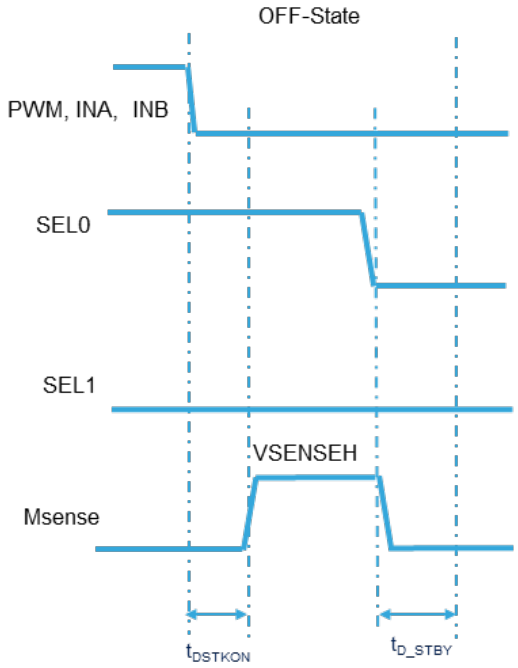


Table 6. **MultiSense pin levels in OFF-state (INA=INB=PWM=0)**

SEL0	SEL1	PULL_UP	MultiSense	OUT STATUS
1	0	Connected on OUT_B	LOW	$V_{OUTA}<V_{OL}$
			V_{SENSEH}	$V_{OUTA}>V_{OL}$
0	1	Connected on OUT_A	LOW	$V_{OUTB}<V_{OL}$
			V_{SENSEH}	$V_{OUTB}>V_{OL}$
1	1	--	LOW	$V_{OUTA}<V_{OL}$
			V_{SENSEH}	$V_{OUTA}>V_{OL}$

7 Phase OUT monitoring

The phase OUT monitoring feature is a new feature specifically designed to allow the VNH9xx devices to be ISO26262 ready and reaching the ASILB target at system level without any other external component (for more detail refer to the dedicated safety manual).

The device features the possibility to provide continuous feedback of OUTA and OUTB status through the dedicated digital signal pin PH_OUT. The PH_OUT pin is an open drain that needs an external pull-up resistor (suggested 1.5 kΩ) to complete the function. The PH_OUT pin reflects the selected-OUT state (high or low) by properly multiplexing through SEL0 and SEL1 (according to the Table 5. Truth table: operative condition and diagnostic).

The phase OUT monitoring operates in both ON and OFF states allowing the system to detect:

- A load fault: open load or short to V_{CC}/GND.
- A single Power MOSFET fault: if a Power MOSFET remains permanently ON or OFF independently from the input state.

The microcontroller checks that the output state is consistent with input logic, providing the proper reaction to a safe state in case of fault.

The VNH9xx series embed all the network needed to implement the phase OUT monitoring function, including pull-up, pull-down and switches. Depending on device status, the connection of the internal pull-up and pull-down network can properly be selected through SEL0 and SEL1 as per Table 5. Truth table: operative condition and diagnostic:

- During clockwise and counter clockwise motor activations, external pull-up resistors are not needed.
- During brake to VBAT, the microcontroller can alternatively switch off one of the two high-sides and thanks to the embedded pull-down resistor, the microcontroller can detect if the related high-side is failing short through the PH_OUT pin.
- During brake to GND, the microcontroller can alternatively switch off one of the two low-side and thanks to the embedded pull-up the microcontroller can detect if the related low-side is failing short through PH_OUT pin.

Note: During brake to GND condition (INA = INB = L, PWM = H) it is possible to turn on selectively one single LS Power MOSFET by settling the pin SEL1 and SEL0. This allows a higher monitoring level and a higher flexibility in half-bridge or multi-motor operation.

The following examples summarize all failure conditions, the MultiSense and PH_OUT signals behavior and recommendations for diagnostics sampling.

8 Full bridge configuration diagnostic summary

Below paragraph will explain in detail how to perform the complete application diagnostic in both ON and OFF state able to detect any condition on open load, short circuit or load properly connected.

A similar approach can be used also for safe detection to detect if any internal HS or LS PowerMOSFET is failing open or short. For a deeper explanation please refer to the dedicated safety manual.

8.1 Diagnostic in ON state

Figure 43. Example 1- load connected

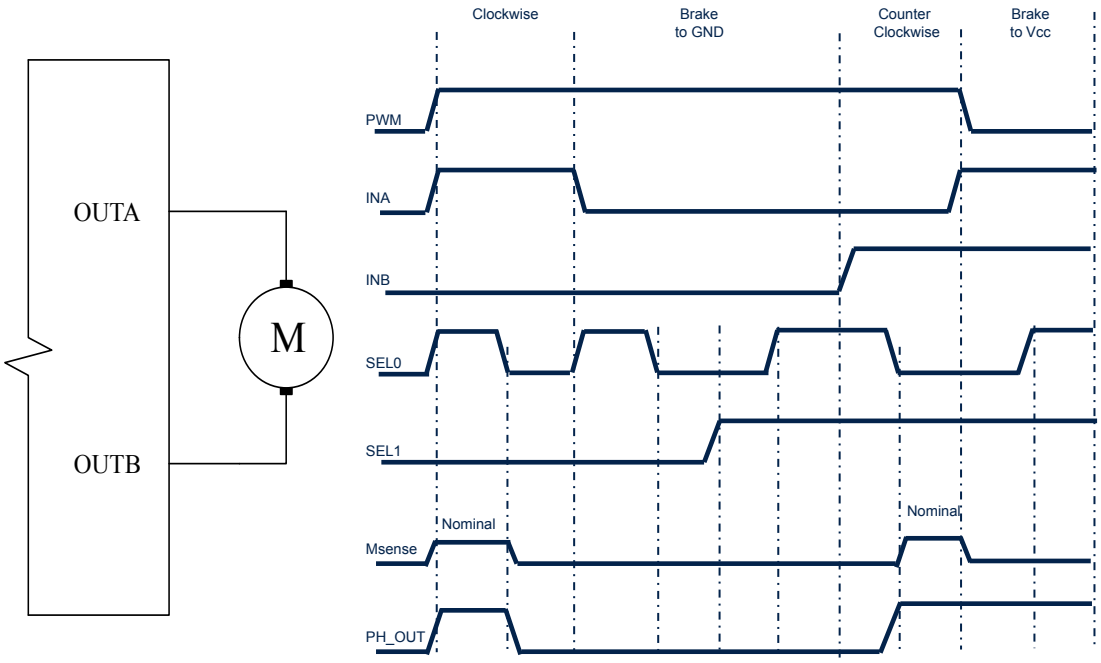


Table 7. Example 1

Condition	Signal	SEL0 = H, SEL1= L	SEL0 = L, SEL1= L
Clockwise (HSA, LSB active)	MSense	NOMINAL	0 V
	PH_OUT	High	LOW
	Notes	No error detected	
Brake to GND (LSA, LSB active)	MSense	0 V	O V
	PH_OUT	LOW	LOW
	Notes	No error detected	

Table 8. Example 1b

Condition	Signal	SEL0 = L, SEL1= H	SEL0 = H, SEL1= H
Brake to GND	MSense	LOW	LOW
	PH_OUT	LOW	LOW
	Notes	No error detected	

Condition	Signal	SEL0 = L, SEL1= H	SEL0 = H, SEL1= H
Counter clockwise (HSB, LSA active)	MSense	Nominal	0 V
	PH_OUT	HIGH	LOW
	Notes	No error detected	
Brake to V_{CC} (HSB, HSA active)	MSense	0 V	0 V
	PH_OUT	HIGH	HIGH
	Notes	No error detected	

Figure 44. Example 2- open load

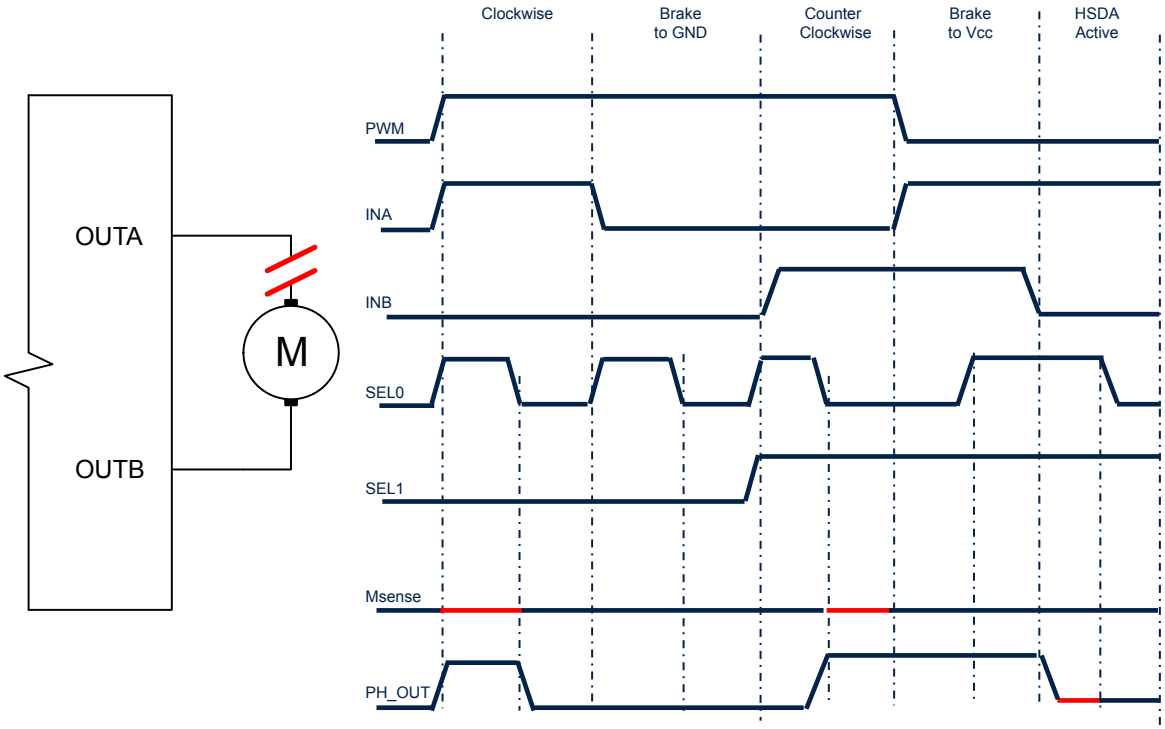


Table 9. Example 2

Condition	Signal	SEL0 = H, SEL1=L	SEL0 = L, SEL1=L
Clockwise (HSA, LSB active)	MSense	<Nominal	0 V
	PH_OUT	HIGH	LOW
	Notes	Error detected Msense output < Nominal	No error detected
Brake to GND (LSA, LSB active)	MSense	0 V	0 V
	PH_OUT	LOW	LOW
	Notes	No error detected	No error detected

Table 10. Example 2b

Condition	Signal	SEL0 = L, SEL1=H	SEL0 = H, SEL1=H
Counter clockwise (HSB, LSA active)	MSense	0 V	0 V
	PH_OUT	HIGH	LOW

Condition	Signal	SEL0 = L, SEL1=H	SEL0 = H, SEL1=H
Counter clockwise (HSB, LSA active)	Notes	Error detected Msense output < Nominal	No error detected
Brake to V_{cc} (HSB, HSA active)	MSense	0 V	0 V
	PH_OUT	HIGH	HIGH
	Notes	No error detected	No error detected
HSA active	MSense	0 V	0 V
	PH_OUT	HIGH	LOW
	Notes	No error detected	Error detected On PH_OUT

Figure 45. Example 3 - short-circuit to V_{CC} on OUTA

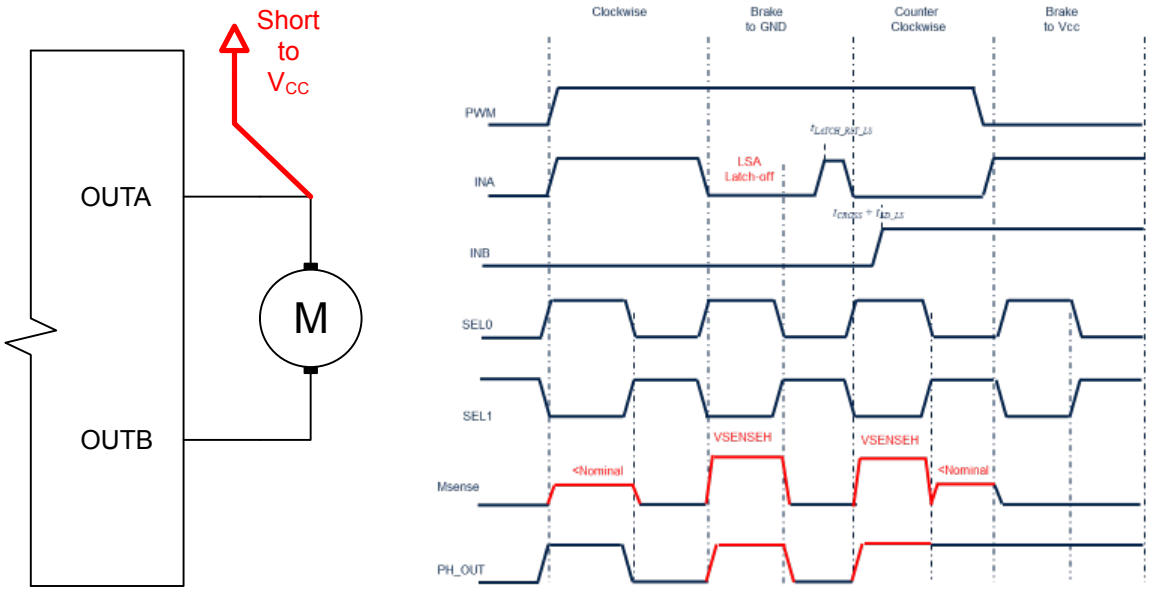


Table 11. Example 3

Condition	Signal	SEL0 = H, SEL1= L	SEL0 = L, SEL1= H
Clockwise (HSA, LSB active)	MSense	< Nominal	0 V
	PH_OUT	HIGH	LOW
	Notes	Error is detected monitoring OUTA by MultiSense, where VSENSE output < Nominal	
Counter clockwise (HSB, LSA active)	MSense	V_{SENSEH}	< Nominal
	PH_OUT	HIGH	HIGH
	Notes	The error is detected by MultiSense and PH_OUT. LSA is latched-off after the overcurrent condition. Delay time from falling edge of INA pin and time to shut down output in overcurrent condition must be considered (t_{CROSS} and t_{SD_LS}).	
Brake to Vcc (HSB, HSA active)	V_{SENSE}	0 V	0 V
	PH_OUT	HIGH	HIGH
	Notes	No error detected	
HSA active, HSB, LSB, LSA OFF	V_{SENSE}	0 V	0 V

Condition	Signal	SEL0 = H, SEL1= L	SEL0 = L, SEL1= H
HSA active, HSB, LSB, LSA OFF	PH_OUT	HIGH	HIGH
	Notes	No error detected	
Brake to GND (LSA, LSB active)	MSense	V_{SENSEH}	0 V
	PH_OUT	HIGH	LOW
	Notes	Error is detected by monitoring OUTA by MultiSense and PH_OUT. LSA is latched-off after the overcurrent condition. it can be unlatched by a high level pulse on the INA pin (t_{PULSE} > t_{LATCH_RST}). Delay time from falling edge of INA pin and time to shut down output in overcurrent condition must be considered (t_{CROSS} and t_{SD_LS}). A side effect of LSA latched-off during braking to GND causes motor activation through a short circuit on OUTA and active LSB.	

Table 12. Example 3b

Condition	Signal	SEL0 = H, SEL1= L	SEL0 = L, SEL1= L
Brake to GND (LSA, LSB active)	MSense	V_{SENSEH}	0 V
	PH_OUT	HIGH	LOW
	Notes	Error is detected by monitoring OUTA by MultiSense and PH_OUT. LSA is latched-off after the overcurrent condition. it can be unlatched by a high level pulse on the INA pin (t_{PULSE} > t_{LATCH_RST}). Delay time from falling edge of INA pin and time to shut down output in overcurrent condition must be considered (t_{CROSS} and t_{SD_LS}). A side effect of LSA latched-off during braking to GND causes motor activation through a short circuit on OUTA and active LSB.	

Note: Short circuit to Vcc on OUTB can be managed in a similar manner.

Figure 46. **Example 4 - short-circuit to GND on OUTA**

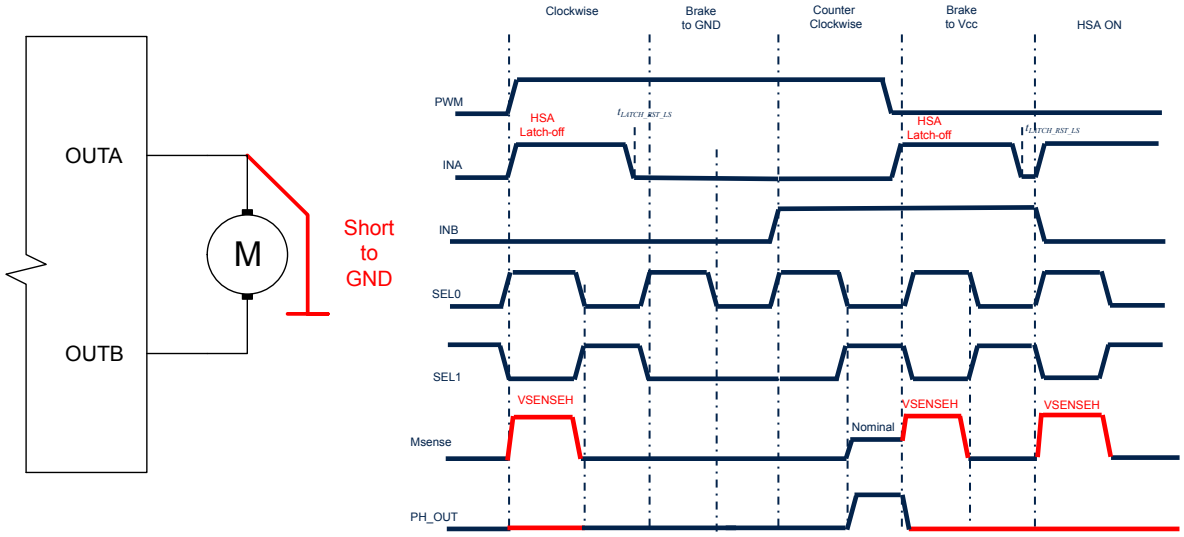


Table 13. **Example 4**

Condition	Signal	SEL0 = H, SEL1= L	SEL0 = L, SEL1= H
Clockwise (HSA, LSB active)	MSense	V_{SENSEH}	0 V
	PH_OUT	LOW	LOW
	Notes	The error is detected by MultiSense and PH_OUT. HAS is latched-off after the first intervention of power limitation or thermal shutdown. Output can be unlatched by a low level pulse on the INA pin (t_{PULSE} > t_{LATCH_RST}).	
Counter clockwise (HSB, LSA active)	MSense	0 V	Nominal
	PH_OUT	LOW	HIGH
	Notes	No error detected	
Brake to Vcc (HSB, HSA active)	MSense	V_{SENSEH}	0 V
	PH_OUT	LOW	LOW
	Notes	Power limitation/overtemperature shutdown. Output latched-off after the first intervention of power limitation or thermal shutdown. Output can be unlatched by a low level pulse on the INA pin (t_{PULSE} > t_{LATCH_RST}). A side effect of HSA latched-off during braking to Vcc causes motor activation through a short circuit on OUTA and active LSB. The condition is detected by V_{sense} > o when reading OUTB	
HSA active, HSB, LSB, LSA OFF	MSense	V_{SENSEH}	0 V
	PH_OUT	LOW	LOW
	Notes	The error is detected by MultiSense and PH_OUT. Output latched-off after the first intervention of thermal shutdown.	
Brake to GND (LSA, LSB active)	MSense	0 V	0 V
	PH_OUT	LOW	LOW
	Notes	No error detected	

Table 14. **Example 4b**

Condition	Signal	SEL0 = H, SEL1= L	SEL0 = L, SEL1= L
Brake to GND (LSA, LSB active)	MSense	0 V	0 V
	PH_OUT	LOW	LOW
	Notes	No error detected	

Note: Short-circuit to GND on OUTB can be managed in a similar manner.

8.2 Diagnostic during OFF state

Figure 47. **Example 5- load connected**

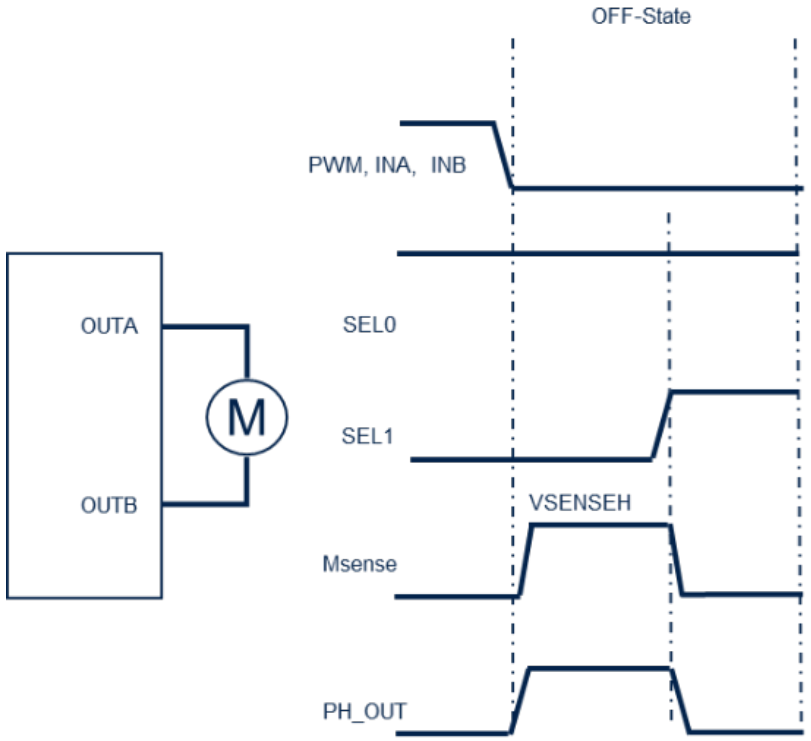


Table 15. **Example 5**

Condition	Signal	INA = INB = PWM= 0
SEL0 = H, SEL1 = L	MSense	V_{SENSEH}
	PH_OUT	HIGH
	Notes	PULL_UP on OUTB, Multisense monitoring OUTA, $V_{OUTA} > V_{OL}$. No error detected
SEL0 = H, SEL1 = H	MSense	0 V
	PH_OUT	LOW
	Notes	MultiSense monitoring OUTB, $V_{OUTB} < V_{OL}$ No error detected, confirming no short to Vcc

Figure 48. **Example 6- open load**

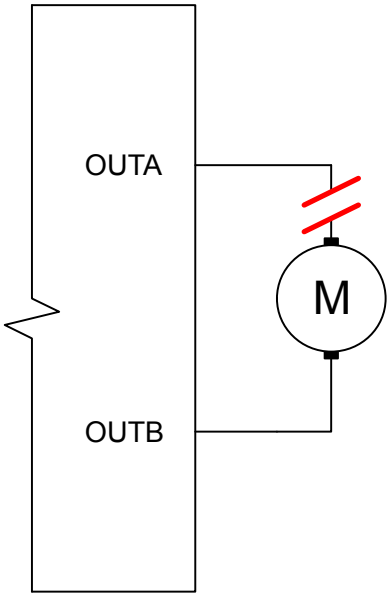


Table 16. **Example 6**

Condition	Signal	INA=INB=PWM=0
SEL0 = H, SEL1 = L	MSense	Low
	PH_OUT	Low
	Notes	PULL_UP on OUTB, MultiSense monitoring OUTA, $V_{OUTA} < V_{OL}$. Error detected on MSense and PH_OUT

Figure 49. **Example 7 - short circuit to V_{CC} on OUTA**

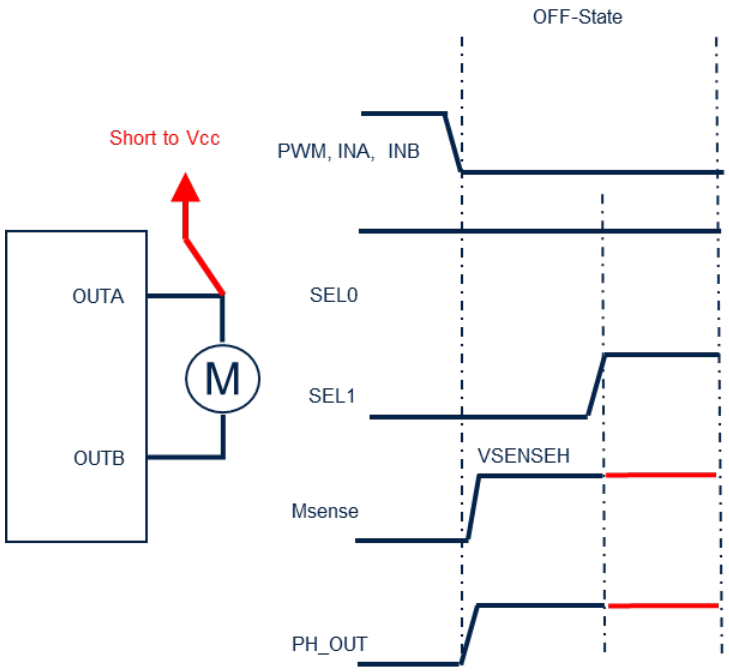


Table 17. Example 7

Condition	Signal	INA = INB = PWM = 0
SEL0 = H, SEL1 = L	MSense	V_{SENSEH}
	PH_OUT	HIGH
	Notes	PULL_UP on OUTB, MultiSense monitoring OUTA, $V_{OUTA} > V_{OL}$. No error detected
SEL0 = H, SEL1 = H	V_{SENSE}	V_{SENSEH}
	PH_OUT	HIGH
	Notes	MultiSense monitoring OUTB, $V_{OUTB} > V_{OL}$ Error detected, confirming short to Vcc

Figure 50. Example 8- short circuit to GND on OUTA

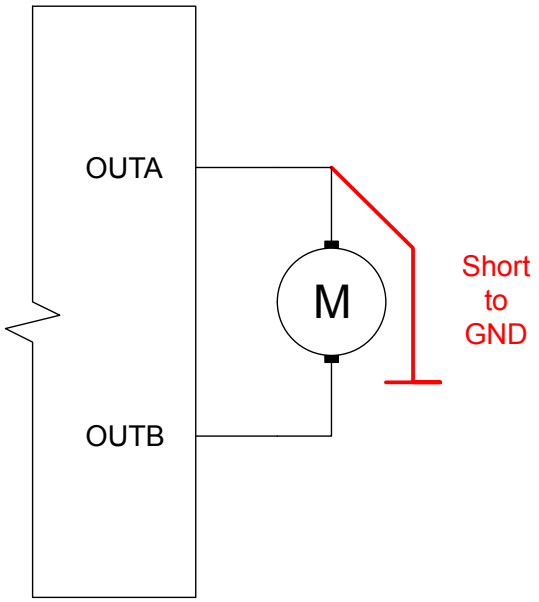


Table 18. Example 8

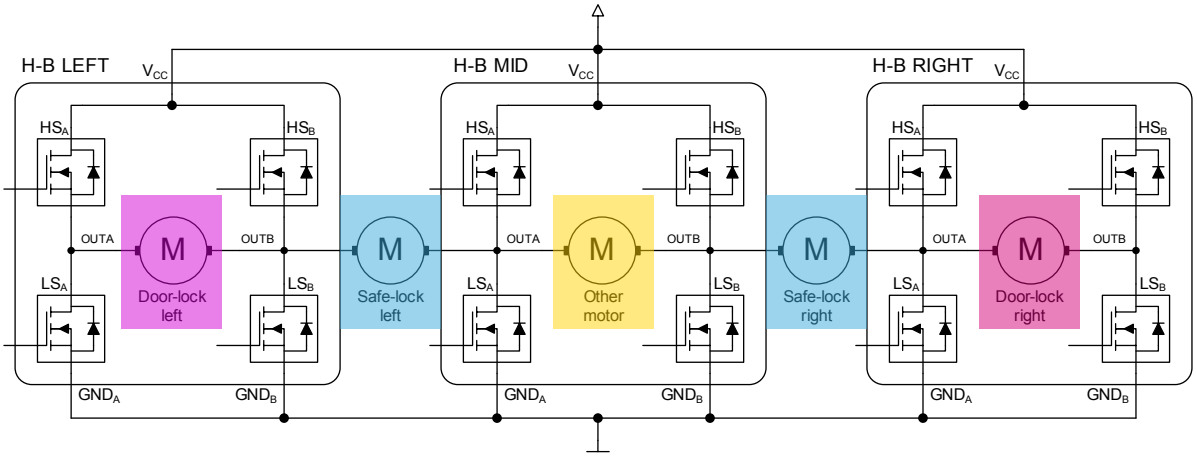
Condition	Signal	INA = INB = PWM = 0
SEL0 = H, SEL1 = L	V_{SENSE}	0 V
	PH_OUT	HIGH
	Notes	PULL_UP on OUTB, MultiSense monitoring OUTA, $V_{OUTA} < V_{OL}$. Short detected

Note: Sampling MultiSense for both outputs (SEL0 = L and SEL0 = H) to distinguish between open load and short circuit to GND condition.

9 Multi-motor configurations

To drive multiple loads (motors), it is possible to combine H-bridges in cascaded configuration, applying a smaller number of H-bridges than motors count. An example of lock system (see figure below) shows possibility to drive five motors in both directions with only three full H-bridges.

Figure 51. Multi-motor system example

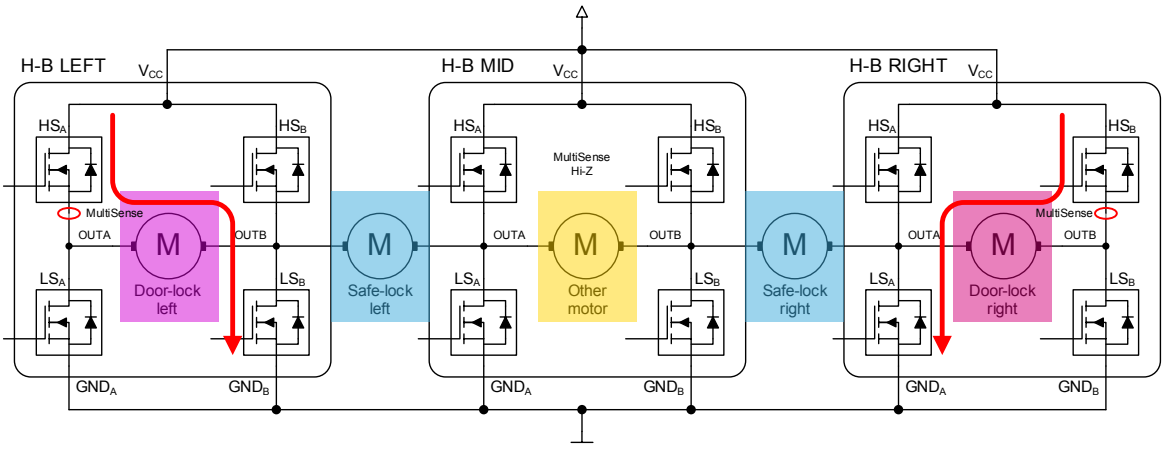


On the example depicted above, each motor can be controlled independently, applying specific combinations of INA, INB and PWM on dedicated H-bridges. In this example are considered VNH9030AQ devices.

In order to save time during motors transitions, multiple motors are activated at the same time.

Steps description:

Figure 52. Locking door-lock left, door-lock right

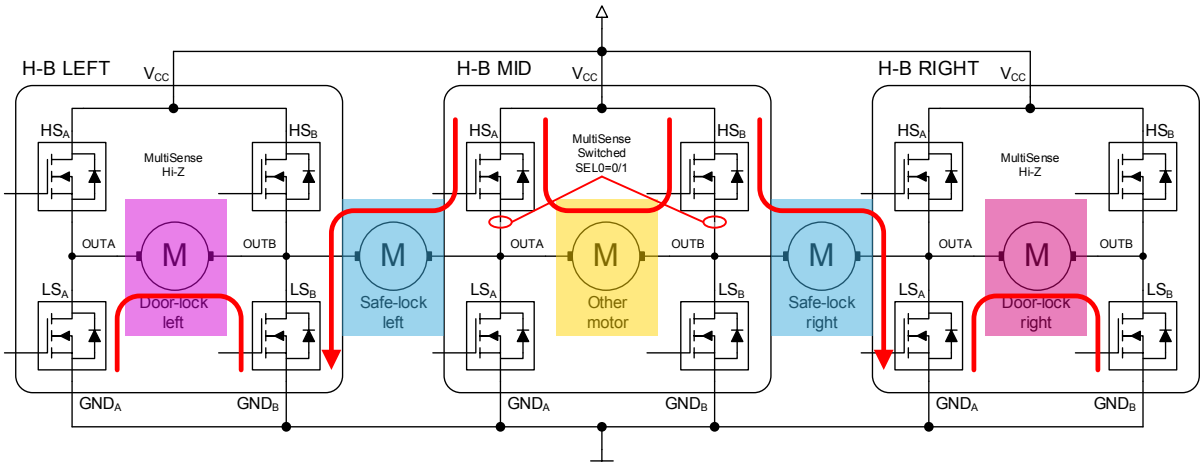


Applying signals INA = 1, INB = 0, PWM = 1, on motor1 is activated. Simultaneously applying signals INA = 0, INB = 1, PWM = 1 MOTOR5 is activated as well. Other motors are inactive as H-B MID is in high-Z mode (INA = INB = PWM = 0).

Analogue diagnostics applies current monitoring on HSA of motor1 by SEL0 = 1 SEL1 = 0 and current monitoring on HSB of motor5 by SEL1 = 1, SEL0 = 0.

9.1 Locking safe-lock left, safe-lock right

Figure 53. **Locking safe-lock left, safe-lock right**



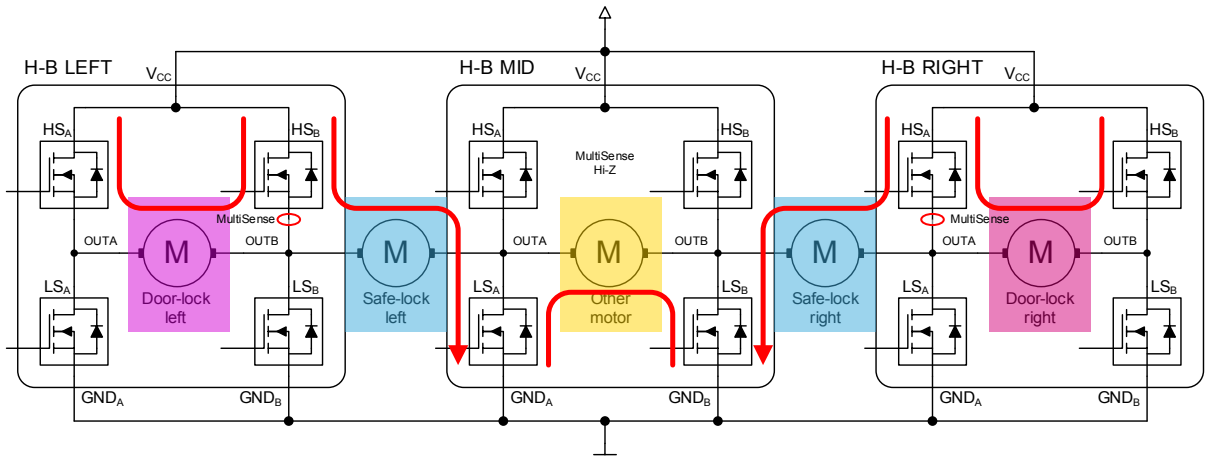
Applying signals INA = 0, INB = 0, PWM = 1 on H-B LEFT, door-lock left is braked to GND. Since H-B MID activates HSA by INA = 1 the safe-lock left is activated. Simultaneously, applying signals INB = 1 of H-B MID and INA = 0, INB = 0, PWM = 1 on H-B RIGHT the Safe-lock right is activated too. Door-lock right is braked to GND. Central motor is braked to V_{CC}.

Even during activation of both high-sides HSA and HSB on H-B MID, it is possible to monitor current over left and right side by alternating SEL0 & SEL1.

In order to monitor both high-sides HSA and HSB of H-B MID, SEL0 should be altered between 0 and 1 during active state of high-sides (INA = INB = 1).

9.2 Unlocking safe-lock left, safe-lock right

Figure 54. **Unlocking safe-lock left, safe-lock right**



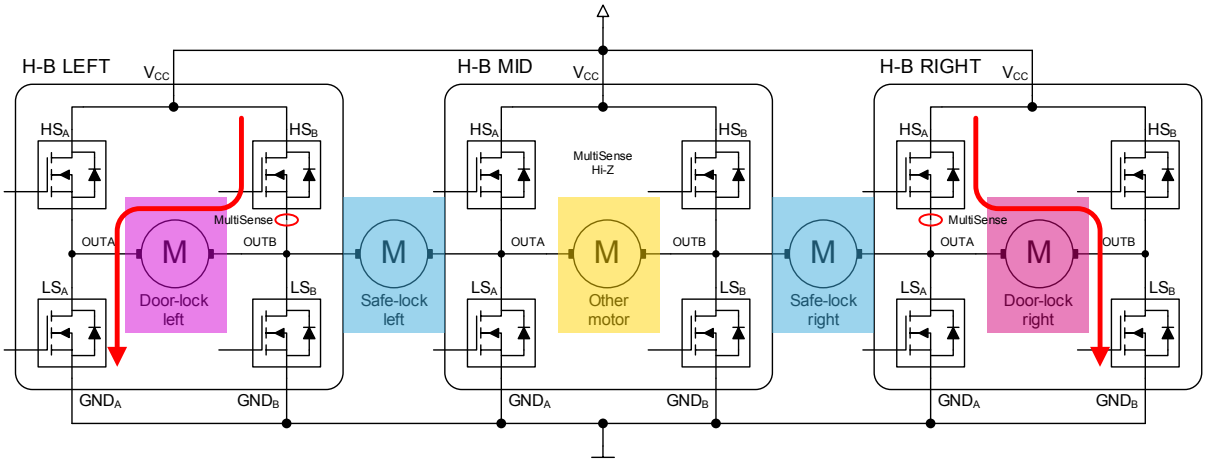
Applying signals INA = 1, INB = 1, PWM = 0 on H-B LEFT Door-lock left is braked to V_{CC}. Since H-B MID activates LSA by INA = 0, PWM = 1 the safe-lock left is unlocked. Simultaneously applying signals INB = 0 (keeping PWM = 1) of H-B MID and INA = 1, INB = 1, PWM = 0 on H-B RIGHT, the Safe-lock right is unlocked too. Central motor is braked to GND, door-lock right is braked to V_{CC}.

MultiSense on H-B LEFT monitor high-side HSB by SEL0 = 0 SEL1= 1, H-B RIGHT monitor high-side HSA by SEL0 = 1, SEL1 = 0.

In order to monitor both high-sides HSA and HSB of H-B MID, SEL0 & SEL1 should be altered between 0 and 1 during active state of high-sides.

9.3 Unlocking door-lock left, door-lock right

Figure 55. Unlocking door-lock left, door-lock right

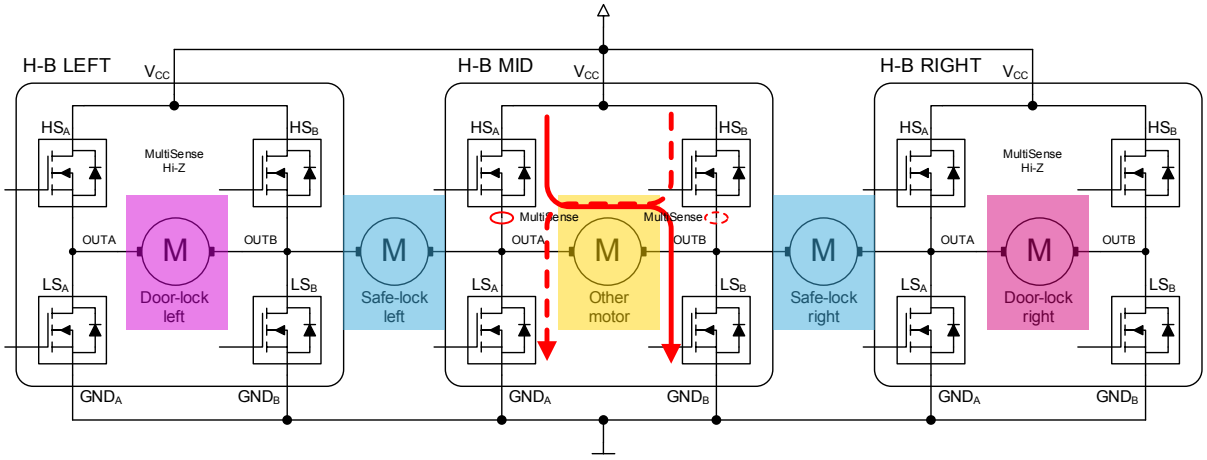


Applying signals INA = 0, INB = 1, PWM = 1, on H-B LEFT the Door-lock left is unlocked. Simultaneously applying signals INA = 1, INB = 0, PWM=1 on H-B RIGHT the Door-lock right is activated as well. Remaining motors are inactive as H-B MID is in high-Z mode (INA = INB = PWM = 0).

Analogue diagnostics apply to current monitoring on HSB of H-B LEFT by SEL0 = 0, SEL1 = 1 and current monitoring on HSA of H-B RIGHT by SEL0 = 1, SEL1 = 0.

9.4 Central motor separate control lock, unlock

Figure 56. Central motor control



In order to control central motor, only H-B MID is activated. H-B LEFT and H-B RIGHT is kept in high-Z mode by applying INA = INB = PWM = 0.

To control central motor in direction depicted by solid red line, INA = 1, INB = 0 and PWM = 1. MultiSense monitors high-side HSA by SEL0 = 1, SEL1 = 0.

To control central motor in opposite direction depicted by dotted red line, INA = 0 INB = 1 and PWM = 1 are applied. MultiSense monitors high-side HSB by SEL0 = 0, SEL1 = 1.

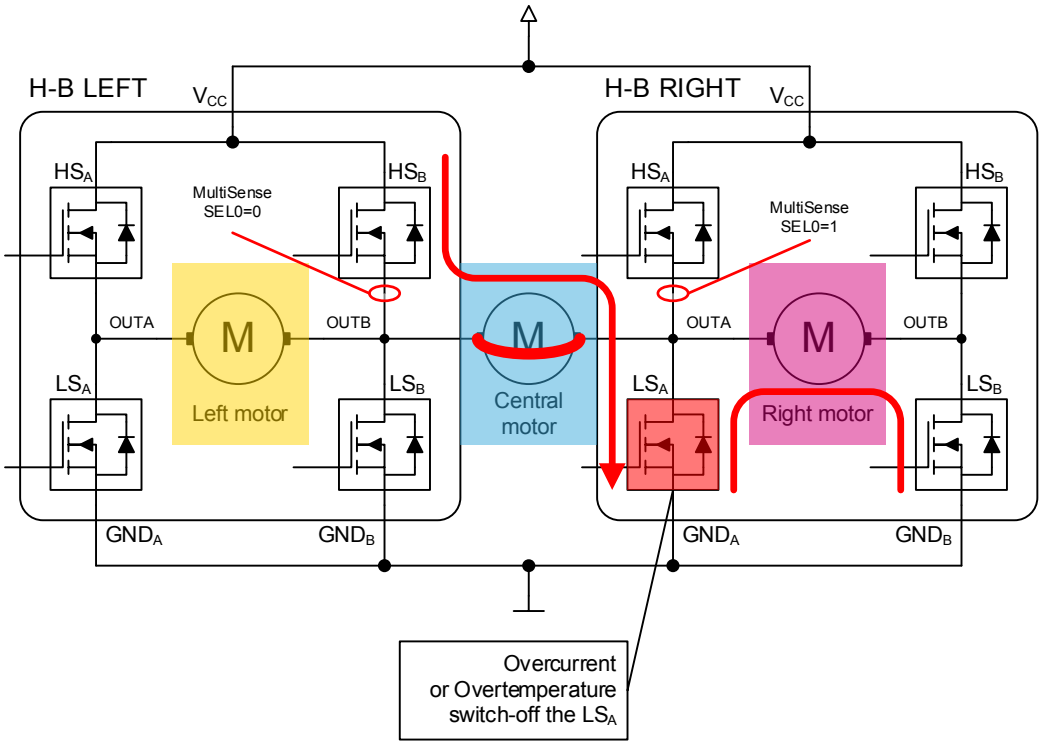
OFF-state diagnostics can be applied during High-Z state on H-bridges.

9.5 Preventing unwanted activation of the motor in brake state

In the multi-motor configuration an unwanted situation can appear, causing possible activation of the motor in brake state. Following sequence shows the effect on a simplified setup (see the figure below).

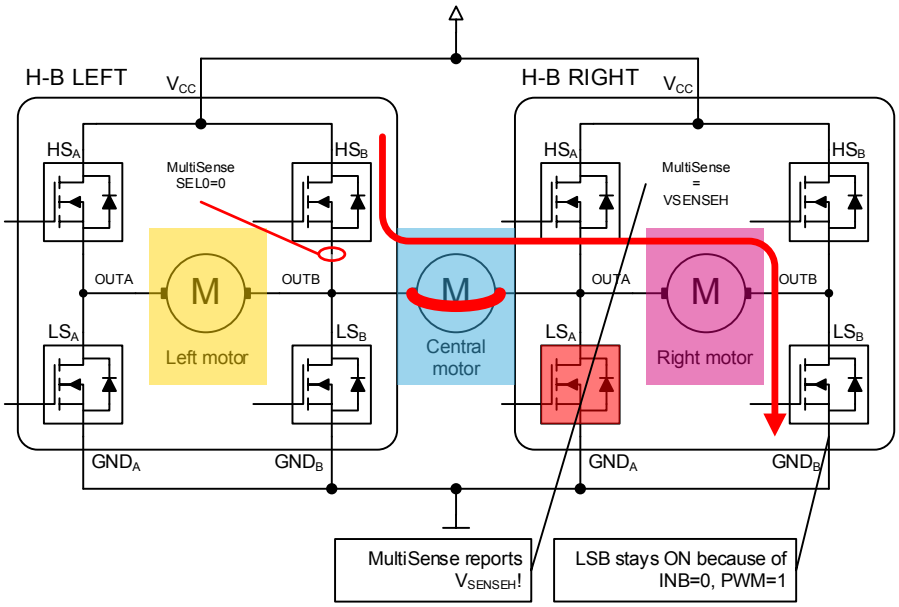
There is an activated central motor by the INB = 1 (high-side) on H-B LEFT, INA = INB = 0, PWM = 1 (low-side) on H-B RIGHT. The right motor is braked to GND.

Figure 57. Motor failure possible scenario



If one of the protections of the low-side on H-B RIGHT is activated (exceeding LS shut down current or overtemperature shutdown) due, for example, to a hard short circuit between the terminals of the central motor, since the PWM is high, the low-side on H-B RIGHT stays ON and therefore the right motor will be activated because it is in series with the central motor (see Figure 58. Unwanted motor activation through other failing motor).

Figure 58. **Unwanted motor activation through other failing motor**



VNH9xx allow a new feature to turn on only one of the two LSD by properly selecting SEL0 and SEL1.

On above example by selecting on H-B RIGHT INA = INB = 0, PWM=1 and SEL0 = SEL1 = 1 only LSA will be turned on. This avoids unwanted right motor activation in case of fault of LSA in the H-B right.

Revision history

Table 19. **Document revision history**

Date	Revision	Changes
17-Apr-2024	1	First release.

Contents

List of tables

List of figures

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2024 STMicroelectronics – All rights reserved