New LV Wide SOA Power MOSFET technology for Linear Mode operation

Gaetano Bazzano, Daniela Cavallaro, Marco Comola, Giuseppe Consentino, Stefania Fortuna, Giuseppe Longo, Gaetano Pignataro, Filippo Scrimizzi
STMicroelectronics, Stradale Primosole 50, Catania, Italy,

gaetano.bazzano@st.com, daniela.cavallaro@st.com, marco.comola@st.com, giuseppe.consentino@st.com, stefania.fortuna@st.com, giuseppe-mos.longo@st.com, gaetano.pignataro@st.com, filippo.scrimizzi@st.com,

Abstract

Many applications, especially in the Telecom (hot-swap + PoE) and Automotive field, require Power MOSFET robustness in linear mode. Modern devices have been designed for ever-decreasing on-resistance and very high current capability at the expense of reduced FBSOA (Forward-biased Safe Operating Area).

Linear Mode operation highlights a different scenario than a switched-mode application where the design is usually driven by dynamic and static power losses. If the device is operated in Linear Mode, the power dissipation is quite high because it works with high voltage drop and high current that could result in rapid increase of the junction temperature that may lead the Power MOSFET to thermal runaway or in other words to an unstable condition that occurs when the junction temperature increases without control until device failure occurs.

The objective of the following paper is to evaluate the key requirements of a Power MOSFET working in a hot-swap application and to compare the latest advanced LV technology, not suitable for it, with the new tailored technology designed by ST to satisfy the harsh requirement of the Linear Mode Operation.
**Introduction**

High-availability systems, such as servers, network switches, redundant-array-of-independent-disk (RAID) storage, and other forms of communications infrastructure, need to be designed for near-zero downtime throughout their useful life. If a component of such a system fails or needs updating, it must be replaced without interrupting the rest of the system so it means that the board or module will have to be removed and its replacement plugged in while the system remains up and running. This process is known as hot swapping.

When a line card is plugged into a live backplane, the card's discharged power supply filter capacitors present a low impedance and demand a large, sudden "inrush" current. This sudden high load can cause the backplane's power supply to collapse.

Hot-swap controllers, provide inrush current limiting when the card is first inserted, and short-circuit protection while the card is in operation.

![Diagram of a hot-swap controller](image)

**Figure 1: Hot-swap controller**

A hot-swap controller limits the inrush current by slowly decreasing the on-state resistance of an N-channel MOSFET. When the board is first plugged in, the controller slowly enhances the MOSFET, allowing the voltage at the MOSFET's drain to rise from zero volts (or fall from zero volts for PC boards powered by a negative supply).

Following figure shows the typical SOA curve included in most power MOSFET datasheets. The constant power curves, shown to the right of constant current line within the SOA boundary, are extracted from the thermal data with the assumption that the junction temperature is essentially
uniform across the power MOSFET die. The dissipated power does not cause a catastrophic failure to the device, but brings its junction temperature up to the maximum guaranteed temperature when the applied power pulse is evenly distributed on the die surface.

The parameter that measures such thermal instability is the thermal coefficient (TC). The thermal coefficient is defined as the derivative from the drain current versus temperature \( \left( \frac{\partial I_D}{\partial T} \right) \) and is generally normalized by the active area or device perimeter in order to compare the performances of different devices or structures.

When TC is zero, or negative, by increasing the temperature, the drain current decreases thus, the device works in thermal stability conditions. 

Whenever the TC is positive, the device may fail. That depends on the capability of the whole die thermal system to catch away the heat per unit area and time developed by the electrical power pulse. If the heat produced by unit time can be totally extracted from the device, then the power MOSFET works in safety conditions.

The above reported conditions are set by the external application conditions that together with the physical behaviour linked to the thermal stability of the mosfet elementary cells, define the thermal stability of the device working in linear mode.

**Figure 2: SOA limits**
The heat developed inside the junction is due to the electrical power dissipation in linear mode:

\[ P_D = V_{DS} \cdot I_D = \frac{\Delta T}{R_{thj-a}} \]

When the temperature rises the drain current changes depending on the thermal coefficient; the device can manage power till reaching of the failure point

\[ V_{DS} \cdot \frac{\partial I_D}{\partial T} < \frac{\partial \Delta T}{\partial T} \cdot \frac{1}{R_{thj-a}} \]

Sometimes even if the structural features of the device don’t match this requirement, it doesn’t fail because the \( R_{thj-a} \) is enough low to dissipate the generated heat due to the applied power, the failure happen when

\[ \left| \frac{\partial I_D}{\partial T} \right| = \frac{1}{V_{DS}} \cdot \frac{1}{R_{thj-a}} \]

Here below are reported the transcharacteristics at different temperatures with the crossing point at 0 TEMPCO and the thermal coefficient of the MOSFET. The lower is the 0 TEMPCO in term of Vgs and Id, the better is the MOSFET in self-limiting the current during the linear mode operation. The crossing among the limits conditions defined by the application (Vds voltage drop and thermal budget/Rth) and the thermal coefficient define the thermal instability current window. Therefore at a fixed Vds and Rth the MOSFET cannot withstand for long time any current inside this forbidden window.

![Figure 3: Thermal coefficient and Thermal instability current window](image-url)
\[
\frac{\partial P_{\text{generated}}}{\partial T} > \frac{\partial P_{\text{dissipated}}}{\partial T} \rightarrow V_{\text{DS}} \cdot \frac{\partial I_{DS}}{\partial T} > \frac{1}{Z_{\text{thJC}}(t_{\text{pulse}})}
\]

So practically:

\[
\text{Instability} = \frac{1}{V_{\text{DS}} \cdot Z_{\text{thJC}}(t)} < \frac{\Delta I_{\text{drain}}}{\Delta T}
\]

To avoid this unstable condition, ST has introduced a new technology able to meet a wider FBSOA capability in conjunction with an extremely low on-state resistance (trade-off between Linear Zone operation and Switching operation efficiency).

Here below are reported the comparison in terms of thermal coefficient, at high Vds and Tc, among a standard low Rds(on) trench technology and its equivalent die-size wide SOA one.

Comparing those two curves is evident the maximum value of the two parabolic curves and the current value starting from which the thermal coefficient becomes negative (thermal stability region for the MOSFET).

The wide SOA technology has lower maximum thermal coefficient and narrower positive coefficient area (TC<0 when Ids > 43A at Vds=20V).

The slope of the Trans-characteristic shows a controlled current gain. The lower is the slope the better is the linear mode capability.

Basing on a detailed characterization at high temperature we run a simulation trial to define the thermal stability behavior of our wide SOA technology and the best competition.

Thanks to a dedicated silicon structure elementary cells and package features, the current trend vs the working time in linear mode at high Vds shows an almost flat current curves.
This remarks the capability of the device to manage that working conditions (see below reported simulation curves).

**Figure 5: Trans-characteristics**

**Figure 6: Id vs Time**
The benchmark

To see the performances of our devices in a Hot Swap application we used the below simple board schematic:

![Board schematic](image)

**Figure 7: Board schematic**

Once the driver transistor is on, the pre-charged capacitance connected to the power supply will discharge through the DUT. The external gate-drain zener diodes will clamp the Vds voltage at the selected value and the gate-source resistor will provide the relevant Vgs to flow the fixed Ids current.

A STD trench technology device fixing the board at Vds=30V, Ids=25A (typical working condition in TELECOM application) fails at around 800us. Here below is reported the relevant scope waveform:

![Scope waveform](image)

**Figure 8: 25A/30V test results using STD Trench technology**
Applying the same testing condition to a new WIDE SOA technology device, we are able to survive at least 2 ms that represents the minimum time gap required from the main CTMs. Wide SOA device can withstand even $V_{ds}=40V$, $I_{ds}=25A$, $T_{pulse}=1ms$ in linear mode condition. Here below are reported the relevant scope waveforms:

**Figure 9:** 25A/30V test results for $T_p=2ms$ using Wide SOA Trench technology

**Figure 10:** 25A/40V test results for $T_p=1ms$ using Wide SOA Trench technology
Conclusions

The new wide SOA technology ST got for 100V MOSFETs shows good results both in terms of thermal coefficient and current gain control providing the thermal stability in the high voltage and current SOA area becoming less sensitive to the FBSOA drift (Spirito effect).
The already available samples are now able to withstand STD CTM's hot swap condition.
The process and design features of the new «WIDE SOA» technology allow to achieve a good linear mode ruggedness;

References