An evaluation of the failures in resonant topologies due to the body diode and the role of fast diode MOSFET

Domenico Nardo
STMicroelectronics
Catania, Italy
domenico.nardo@st.com

Alfio Scuto
STMicroelectronics
Catania, Italy
alfio.scuto@st.com

Simone Buonomo
STMicroelectronics
Catania, Italy
simone.buonomo@st.com

***Abstract*— The aim of this paper is to evaluate and understand the failure mechanism due to reverse recovery of the intrinsic body diode of the Super Junction MOSFET in terms of physical processes both inside the device and at the converter level. Nowadays, higher reliability and theoretically failure free systems are in high demand in order to maintain service continuity in typical telecom or server applications. The topologies under analysis in this paper are the half bridge resonant converter (HB LLC) and the full bridge resonant converter (FBLLC). Moreover, a solution for this problem based on the fast recovery diode SJ MOSFET based on MDmesh™ technology from STMicroelectronics was proposed.**

Keywords—MOSFET, Super Junction, resonant converter, fast diode, reverse recovery

I. Introduction

The need to manage an ever-increasing amount of data deriving from huge growth in telecommunications, IoT and cloud storage has led to an exponential growth in the adoption of DC/DC converters with higher efficiency. For this reason, soft switching applications have become crucial in the field of Telecom and Server. The main topologies adopted are the half and full bridge LLC and the phase shift full bridge. All of them work with the zero voltage switching (ZVS) condition at turn-on, which eliminates switch-on losses, allows higher efficiency, and reduces or in some cases eliminates the need for heatsinks.

The reliability and higher immunity to possible failures even in high stress conditions is mandatory to avoid service failure. All of this is dependent on primary side MOSFETs and on their most sensitive component, the intrinsic body diode. In standard working conditions, the body diode does not affect the normal operation of the converter, but it is fundamental in order to achieve the soft switching condition at turn-on. In this type of converter, the switching frequency is usually increased in order to reduce the volume and weight of the transformer as well as of the other passive components. However, high frequency operations increase the stress in the switching devices, thus a trade-off for optimal converter design must be found.

II. Reverse Recovery Mechanism

The intrinsic body diode of the super junction MOSFET that is created between the p+ body region and N- epitaxial layer, shown in Fig. 1, has an active role in some bridge topologies. In fact, it becomes a current path when both MOS of the half bridge are off. When the device is in the off state and the voltage across drain and source pin can forward bias the body diode, it can conduct current from source to drain.

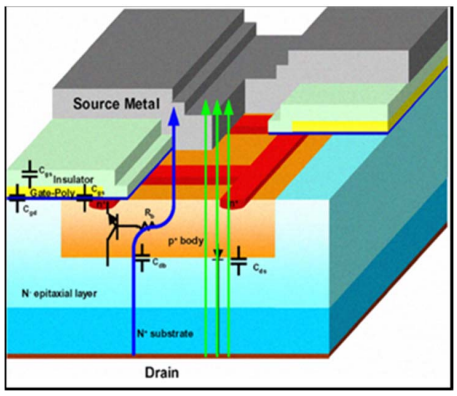

Figure 1 Vertical structure including the parasitic components

As soon as the drain to source voltage is insufficient to forward bias the diode, reverse recovery starts. Before the diode returns to its blocking state, it is necessary to restore the equilibrium position of the charges that were concentrated in the pn junction during the conduction [1].

In a bridge topology, when the diode passes from forward conduction to the blocking state, the reverse recovery is seen as a large current peak in the drain current of the MOSFET as it turns on, figure 4 shows this situation. Since the reverse recovery current depends on the average forward current, the higher the ISD [2], the higher the peak reverse recovery current (Irrm) is [3]. The time interval and di/dt of the fall of ISD to Irrm depends on the PCB layout, time and di/dt of the rise from Irrm to zero depends only on the intrinsic technology of the MOSFET. The device datasheet provides the test condition for the diode and its relative characteristics: Qrr, trr,

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Irrm. All of them are influenced by VDD, and a lower VDD results in higher values, which implies a worse condition, as shown in Fig. 3.

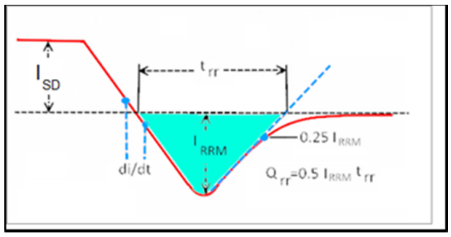

Figure 2 Details of Qrr, trr and Irrm

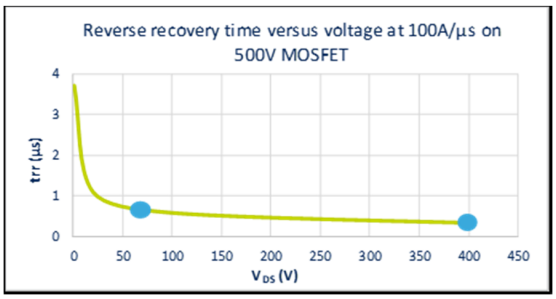

Figure 3 Dependences of body diode parameters on the VDD

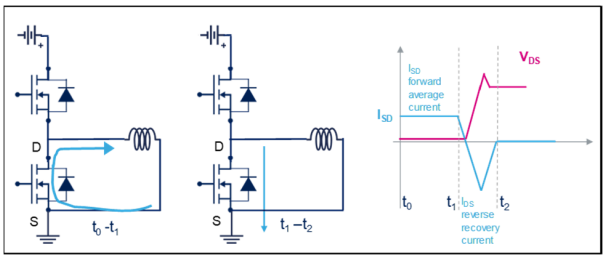

Figure 4 Body diode current during forward bias (t0 - t1) and during reverse recovery (t1 – t2).

III. Overview of Resonant Converters

The main topologies currently used in the DC/DC stage that achieve ZVS at turn-on are the following:

- Half bridge LLC (HB LLC)
- Full bridge LLC (FB LLC)
- Full bridge phase shift (FB PS)

The first topology is used for power levels ≤ 1500 W, while the other two are used for very high power up to 10 kW. For the first two converters, the mechanism for achieving ZVS is essentially the same: by using an LLC tank as shown in Fig. 5, consisting of two inductances in series and a capacitor. During the dead time, the current stored in the series inductor (Lr) is used to discharge the output capacitance (COSS) of the MOS that will be turned on; after the discharging of the COSS, the body diode can conduct and the MOS are turned on without the voltage-current cross. The behavior of the resonant tank is therefore inductive and the current of the tank falls to zero after the applied voltage reaches zero.

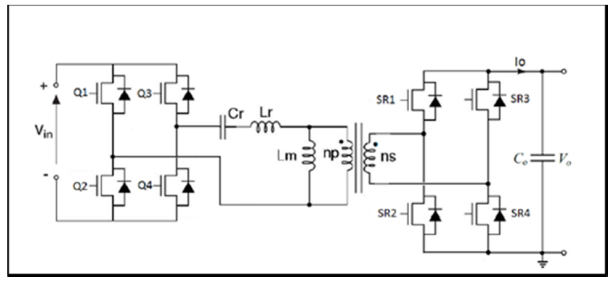

Figure 5 Typical schematic of a FB LLC

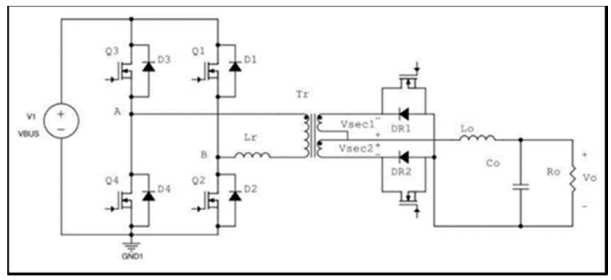

Figure 6 Typical schematic of a FB PS

For the FB PS, the ZVS condition is achieved in a different way: as shown in Fig. 6, only an Lr is used, without the Lm or the Cr. It is important to highlight that the two legs have a different level of available energy to achieve ZVS because one leg turns on after the powering phase and the other after the free-wheeling phase; for this reason, the two legs are referred to leading leg and lagging leg, respectively. Moreover, the devices of the diagonal do not turn on at the same time to achieve ZVS. In fact, when only one MOS is in ON state, the current stored in Lr is used to discharge the output capacitance of the turning on device; in this way, the diode conducts and the channel is turned on without the introduction of hard switching [4].

In summary, the behavior to achieve ZVS for the LLC is obtained during dead time, when both MOS are in OFF state, while in FB PS, ZVS is obtained when one MOS of the diagonal is ON.

It is important to note that both the HB and FB LLC can easily achieve soft switching even at light load, while it is more difficult for the FB PS, especially at light load and for the lagging leg, where there is less available energy.

IV. Overview of Fast Diode Super Junction MOSFET

The Super junction fast diode MOSFET designed to achieve low reverse recovery charge allows drastic reduction of the reverse recovery charge (Qrr), the reverse recovery time (Trr), and the reverse recovery peak current (Irrm) [5]. The reduced Trr and Irrm allows minimization of the reverse recovery effect when the ZVS condition is not achieved.

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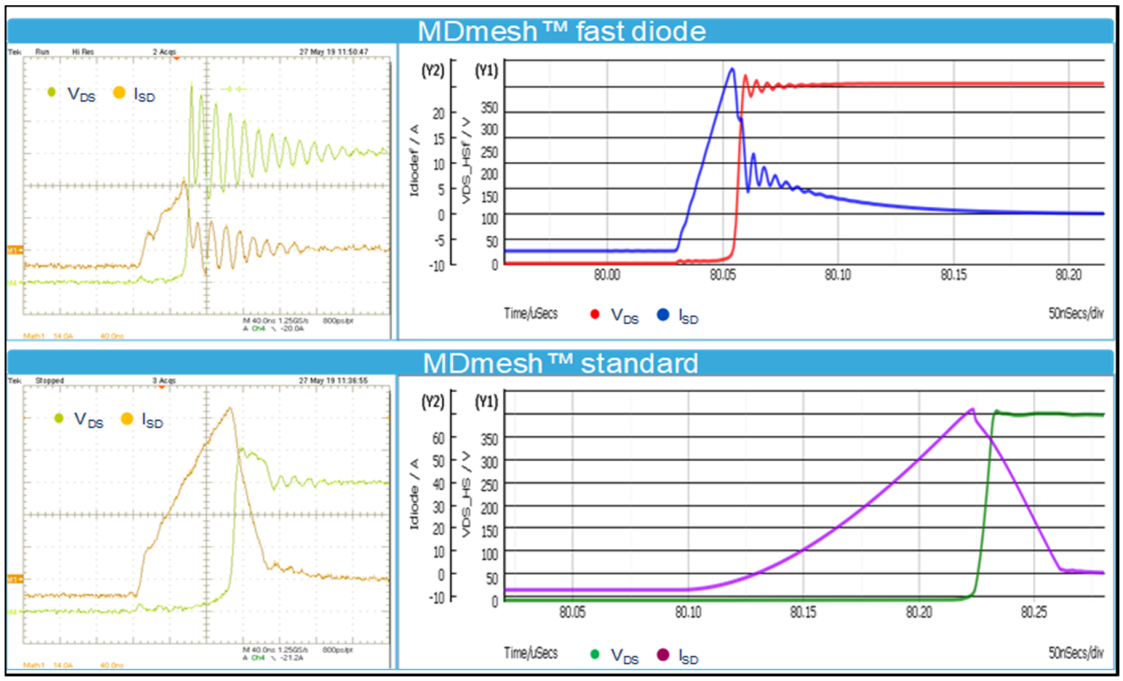

Figure 7 On the left the waveforms of double pulse test on the bench and on the right the simulated ones.

Another relevant benefit associated with the fast diode is the superior ability to handle both dynamic and static dv/dt, hence the reliability of the converter is greater because the device is less sensitive to these types of failures [6] [7].

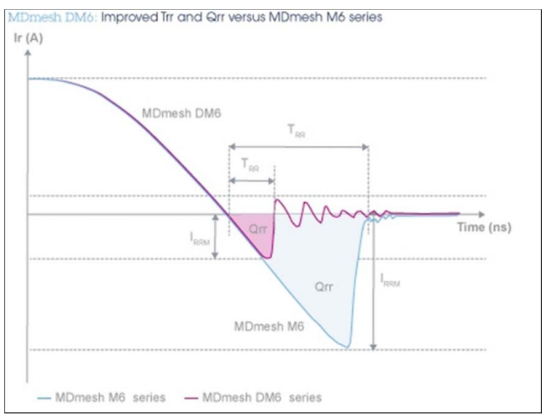

Figure 8 Typical Qrr for MDmesh™ DM6 (fast diode) vs MDmesh™ M6 (standard diode)

Table 1 shows the maximum allowed di/dt and dv/dt for fast and standard diodes.

Table 1 Maximum allowed values for di/dt and dv/dt declared on datasheet

	FAST	STANDARD
di/dt (A/µs)	900	400
dv/dt (V/ns)	50	15

V. Converter Failures due to Body Diode

The failures related to the body diode that can occur in a resonant converter [8] are associated with:

- Capacitive mode during startup
- Capacitive mode due to overload
- Capacitive mode due to short-circuit of the load

For the LLC, for the FB PS:

- Low and light load condition
- Full load condition
- Load short-circuit condition

During the normal operation of the converter, the body diode is only responsible for discharging the COSS of the MOSFET and obtaining the ZVS condition. On the other hand, when one of abovementioned situation occurs, the converter operates in capacitive mode or without soft switching, and the presence of hard switching at turn on causes the reverse recovery effect [9]. It is important to highlight that the dv/dt created by reverse recovery also depends on the di/dt, which depends directly on the board layout and on the forward average current.

For this reason, a failure condition in one system does not necessarily represent a failure in other converters. When hard switching and reverse recovery appears, the failures may be classified into three types: latch-up of the parasitic bipolar, exceeding the dv/dt rate of the body diode, and thermal runaway.

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VI. EVALUATION OF THE RISK AND MOSFET CHOICE

When designing a soft switching application, it is important to evaluate the risk of stressful and non-standard working conditions occurring. The method proposed in this paper is based on experimental measurements from a double pulse bench test and simulations in SIMetrix in order to align the simulated data with real data, figure 7. After this alignment, the obtained data allowed us to analyze the entire DC/DC converter in established failure conditions and determine, in the design stage, whether a normal MOSFET or a fast diode is needed to ensure a more highly reliable or theoretically failure free system.

Knowing the power level of the converter and the type of load being supplied greatly facilitates the prediction of system behavior. After having calibrated simulation data with the double pulse test results (parasitic inductance of pins, stray capacitance of inductor, etc.), we were able to accurately simulate the entire system and analyze currents during non-standard conditions more thoroughly in order to size the necessary protections appropriately. Figure 15 shows how the simulation results closely match corresponding real data for a specific startup condition and gate driving circuit, and also demonstrates how the fast diode version of the same MDmesh™ technology manages the reverse recovery effect better and operates within datasheet limits. In reality, the standard technology does not fail in this situation either, but its dv/dt and di/dt exceeds datasheet limits.

VII. PROPOSED METHOD

A. double pulse test

The first step in our method consists of a double pulse bench test and the generation of the same results in a simulator, where dv/dt, di/dt and Irrm conditions are reproduced. The double pulse test allows us to characterize the dynamic behavior of a MOSFET, which therefore becomes both driver and DUT. The gate and source pins of the DUT are shorted in order to prevent device turn on and use only its body diode, as shown in Fig. 9.

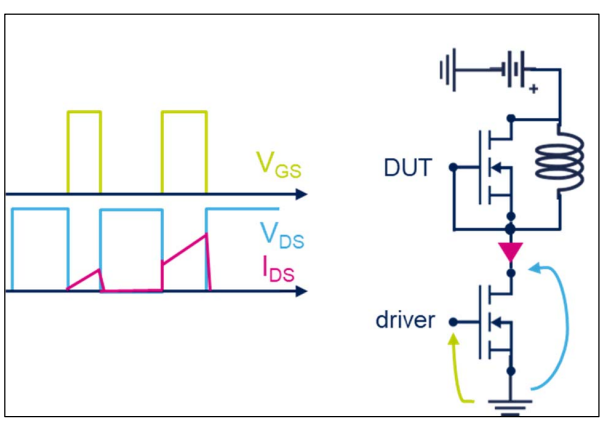

Figure 9 Schematic of a double pulse test and relative waveforms

During the second Vgs pulse (light green in Fig. 9), the VDS and ISD waveforms are captured and used as reference values in order to optimize the SPICE model and introduce real pin parasitic inductance values. This step is crucial because the parasitic inductances combined with the intrinsic di/dt of the device create an overshoot proportional to L*di/dt. In Fig. 7, the MDmesh™ with fast diode is faster than the standard one and this higher di/dt coupling speed with the L creates more ringing. The values of di/dt, dv/dt and Irrm are taken in accordance with Jedec regulations: di/dt 50% ISD ÷ 75%Irrm. The lower Irrm peak and faster transition help to reduce recovery losses, thus avoiding thermal runaway.

B. Correlation between bench and simulation

Table 2 shows the values of the bench test and the simulation.

Table 2 Results from bench and simulation

Bench			
device	Irrm (A)	di/dt (A/µS)	dv/dt (V/ns)
STP40N60M2	73.5	680	56
STP43N60DM2	29.5	400	105
Simulation			
device	Irrm (A)	di/dt (A/µS)	dv/dt (V/ns)
STP40N60M2	72	730	52
STP43N60DM2	29	457	98

The body diode parameters in the simulation agree with the bench counterparts after some adjustments of the Lgate, Ldrain and Lsource, and these values are strictly correlated with the packages and also depend on the distance and on the width of the trace between the bridge MOSFETs. In this case, considering a TO-220 as package, the obtained inductances are [10]:

- L_G 4.5 nH
- L_S 2.5nH
- L_D 1.5 nH

C. Setup the simulation: Include inductances in the topology

Figure 10 shows how to implement the new inductances inside a converter topology. It is important to highlight that all of these inductances must be considered as part of the MOSFET model, so all the probes placed in the simulation are external to them.

After this step, the converter topology was derived and the non-standard working conditions were evaluated [11]. In this way, it is possible to more accurately simulate these situations

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and determine in advance whether it is necessary to use standard or fast diode MOSFETs.

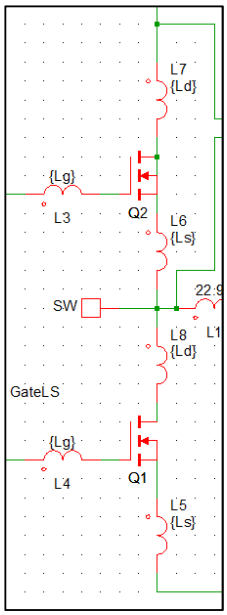

Figure 10 External inductances implementation in a HB configuration

VIII. METHOD IMPLEMENTATION

In this section, a startup and short-circuit phase are investigated in order to demonstrate the ability to operate inside the datasheet limits of both standard and fast diode versions associated with the power level of the converter. Moreover, the startup phase is split into two cases: one with the startup at no load and the other under full load conditions (1500W).

A. Startup

A typical operating condition of the converter is the startup phase, which is very stressful for the converter and for the MOSFETs as the switching behavior depends on the load (no load, full load, etc.). This means that the startup current is different and the responses of the resonant tank and primary bridge are therefore also different.

Figure 11 shows the voltage and drain current for both standard and fast diode technology in a startup condition with no load. In this condition, either MOSFETs can operate without hard switching and reverse recovery effects.

This changes entirely when the startup is performed under a full load condition. Table 3 shows the di/dt, dv/dt and Irrm values. It is important to note that the models used in the simulation reflect the same MDmesh™ technology, where only a platinum process is added in order to improve the body diode, and the fast diode version is obtained; in fact, the di/dt and dv/dt are highly similar because the gate driving and the converter are the same, only the Irrm peak changes considerably as it is linked to the Qrr, which is completely different, as shown in Figure 8.

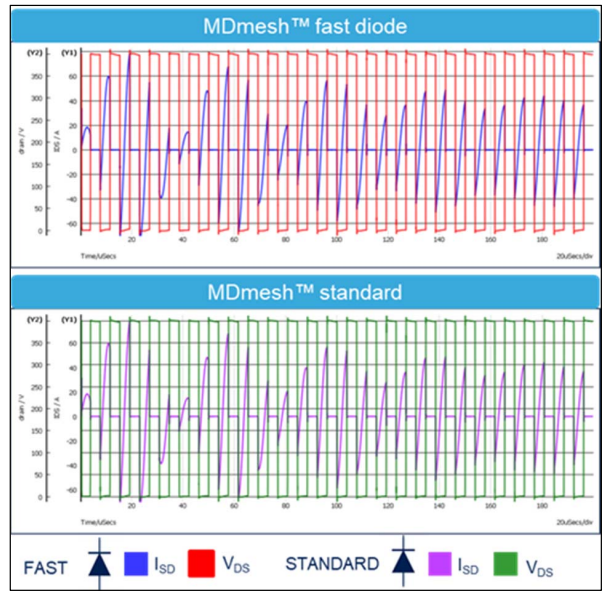

Figure 11 Startup waveforms with no load for the high side MOSFET. On the top fast diode, on the bottom standard diode MOSFET

In this case, only the fast diode version is able to operate within datasheet limits (Table 1) because the maximum allowed dv/dt for the standard diode is 15 V/ns.

Table 3 Data for startup at full load

	FAST	STANDARD
di/dt (A/µs)	112	104
dv/dt (V/ns)	45	40
Irrm (A)	71	80

Moreover, the faster di/dt and dv/dt allow a reduction in the reverse recovery transition, which together with the lower Irrm peak result in a smaller power loss.

In conclusion, a startup under no load or very light load conditions can be tolerated by both fast and standard diode solutions, while operation within datasheet specifications with loads approaching medium or full values is only supported by the fast diode.

B. Load short-circuit

The other condition evaluated is the load short-circuit. If a MOSFET can manage this working condition, it can certainly tolerate the fast transient of the load as the short-circuit condition is the worst type of load transition.

In this condition, the di/dt and dv/dt rates also help increase converter reliability and ruggedness because the drain current is very high during the load short-circuit.

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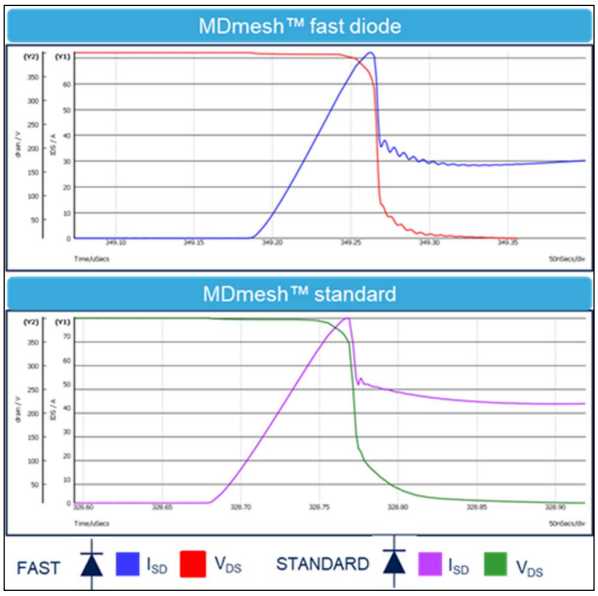

Figure 12 Startup waveforms with full load for the high side MOSFET. On the top fast diode, on the bottom standard diode MOSFET

A smaller Qrr implies a smaller Irrm current, which reduces the I_{DS} current peak and results in a smaller power loss for the same working condition.

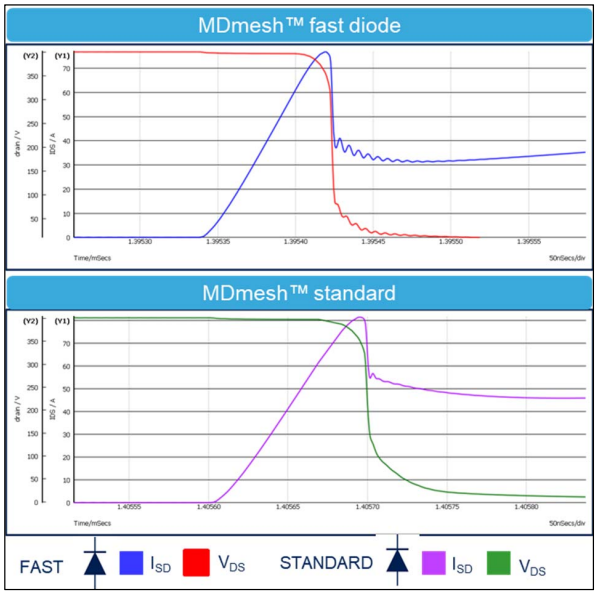

Figure 13 Short-circuit waveforms for the high side MOSFET. On the top fast diode, on the bottom standard diode MOSFET

Table 4 Summarizes the results for this condition.

Table 4 Data for load short-circuit

	FAST	STANDARD
di/dt (A/µs)	115	101
dv/dt (V/ns)	47	42
Irrm (A)	72	84

Figure 13 shows the waveforms for both devices, demonstrating that only the fast diode represents a safe solution able to operate inside datasheet limits. The switch-on power was also evaluated and shown in Figure 14, with smaller losses associated with the fast diode.

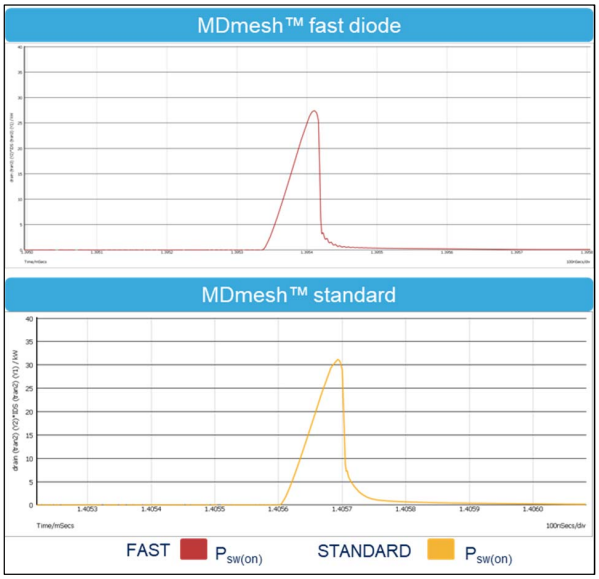

Figure 14 Switch-on energy for the high side MOSFET. On the top fast diode, on the bottom standard diode MOSFET the peak power is respectively 27kW and 31kW.

IX. Method Validation

Following the implementation, a comparison between simulated and real MOSFET waveforms during non-standard operation was performed. Due to the simplicity of the scenario, only the startup condition at full load was reproduced. Figure 15 shows how the simulated waveforms are similar to the real ones, proving that this modeling approach is useful for choosing MOSFETs in the design phase.

Given the accuracy of these results, further analyses could be performed, regarding for example the impact of the gate resistance on the di/dt and dv/dt or the power level, to therefore determine when a fast diode is the only viable solution.

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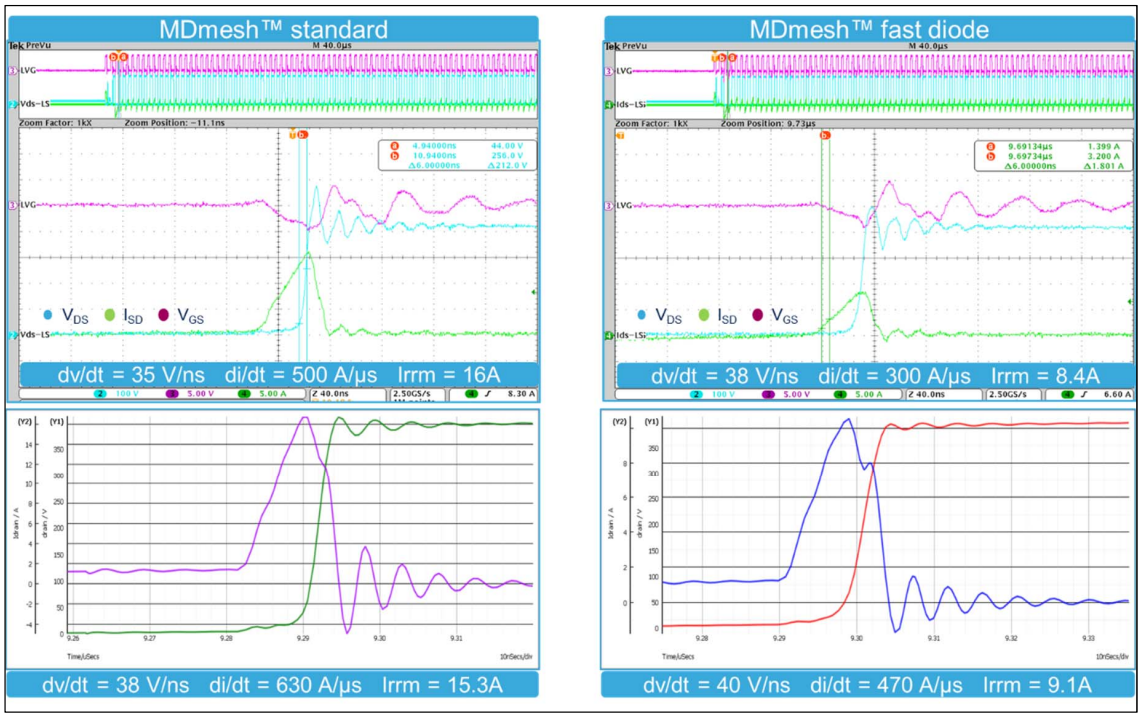

Figure 15 On the left waveforms for standard diode, on the right for fast diode for a startup condition at full load (1500W)

X. CONCLUSION

This paper has forwarded a method to evaluate the failures associated with body diode reverse recovery, based on simulations that were validated by experimental measurement. It is fundamental in the design phase to evaluate and consider the non-standard conditions that might occur in the resonant DC/DC stage of an SMPS. Both the capacitive mode at startup and during short-circuit were investigated and the key performance contributions of the MDmesh™ fast diode technology were demonstrated. The higher dynamic capabilities in terms of dv/dt and di/dt of fast diode MOSFETs allow better management of the reverse recovery effect when the converter operates in capacitive mode and hard switching is present, thus ensuring overall higher reliability of the converter. Furthermore, smaller Trr and Qrr help reduce both reverse recovery duration and Irrm peak current, so the thermal phenomena associated with hard switching at turn-on are also managed better. The optimization of the simulations through alignment with double pulse test outputs results in high correspondence to the real values, as demonstrated in the conclusive experimental measurements. This paper has analyzed the reasons behind the superiority ruggedness of fast diode SJ MOSFETs as they apply to the power rating of the converter and the type and behavior of the powered load.

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