Analysis of the impacts of the V_{GSth} in modern SMPS

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***Abstract*— Addressing modern SMPS applications, the impact of gate-source threshold voltage (V_{GSth}) in super junction MOSFET is investigated, using a DCM PFC and a half bridge LLC as test vehicles. Specifically, a higher V_{GSth}, while effecting the performance, introduces benefits and disadvantages as well.**

Keywords—MOSFET, threshold, SMPS

I. Introduction

The modern switch mode power supplies (SMPS) and power supplies in general targeting very high efficiency, in order to minimize the emission and waste of electrical energy. In last years, more improvements in terms of layout, passive components and optimizing of the control have been obtained then, a suitable solution to further increase the efficiency consists in the use of the Super Junction (SJ) MOSFETs. In facts, the device characteristics influence directly the converter working condition and thus the final efficiency. Moreover, another important issue is the electromagnetic noise of the power converter, in fact, the silicon trend is to reduce its size as well as the rise of its switching speed, so the di/dt and dv/dt increase.

STMicroelectronics with its last SJ technology MDmesh™ M6 [1] has done a MOSFET with a higher V_{GSth} respect to the traditional one (3V), in order to obtain some benefits in the PFC stage and other ones in the DC / DC stage to improve both power efficiency and noise [2], [3], [14-16].

II. V_{GSTH} Impacts at the Turn-On

Figure 1 Turn-on behavior with two different Vth

The V_{GSth} threshold impacts the switch-on behavior then [4], the drain current starts to flow when the V_{GS} value reaches the threshold and at the same time the drain voltage starts to fall to zero, moreover also the period of the miller plateau changes, as showed in Fig. 1. Both these two factors involve in change of the di/dt and dv/dt of the switch, the lower threshold has a faster switching transition, on the contrary Vth 1 (higher than Vth2) is slower [5] [17-19].

Figure 2 Transfer characteristics for two devices with different threshold. In blue line the device with VGSth = 3V and in light blue dot line with VGSth = 4V

Obviously, the transfer characteristics is different, for the same values of V_{GS}, the device with lower Vth conducts more current and reach the maximum value of Id faster than device with higher threshold as showed in Fig. 2. Consequently, the power losses are different, and the higher losses are linked with the higher Vth. If the body diode reverse recovery effect is considered, more concerns are useful to fully explain the switch performance.

$$I_{Dpeak} = I_{SWon} + I_{RR} \qquad \text{Eq. 1}$$

In facts, the current at the turn-on is the sum of the switch current (I_{SWon}) plus the current of the reverse recovery (I_{RR}) Eq.1. For the same diode and in the equal application conditions, the reverse recovery current value is the same, but if the I_{SWon} is smaller, due to its transfer characteristics the peak of the switch-on power is smaller and thus help to reduce the power losses with respect to the case with smaller Vth.

III. V_{GSTH} Impacts at the Turn-Off

On the contrary for the switch-off [6], [20], [21], the higher VGSth values during the turn-off of a SJ MOSFET helps to reduce the switch-off energy. As shown in Figure 3, the threshold voltage defines toff, and the drain current must

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fall to zero when VGS reaches the threshold, the red curve shows the VGS during the switch-off for two different thresholds, Vth1 and Vth2 (Vth1 > Vth2) [7].

Figure 3 Turn-off behavior with two different Vth

Thus, a higher VGSth reduces the toff, due to higher di/dt and dv/dt, and the different current slopes produce different switching off time and a different VDS cross point. Consequently, the associated off energy (Eoff) will be lower for Vth1 and higher for Vth2

IV. Double Pulse Test

The double pulse test allows to analyze the device behavior during turn-on and turn-off, thus the impact of VGSth is analyzed in both conditions. The test was done for a devices couple of the same technology but with different threshold voltage.

A. *Turn-on*

The simulation with a double pulse test confirms that the current's peak (light green curve) at turning on is lower for higher Vth as showed in Fig. 4. Moreover, the $P_{SW(ON)}$ (green curve) power's peak is smaller respect to the device with lower Vth but the duration time (ton) is bigger Fig. 5. The gate resistances used for the test are Rgon = Rgoff = 10 Ω.

Figure 4 Waveforms for turn-on. On the top the case for Vth = 3V and on the bottom the case for Vth = 4V

In table 1 are reported the dv/dt, di/dt and ton, in table 2

Table 1 Switch-on data

Switch-on data			
	dv/dt (V/ns)	di/dt (A/µs)	ton (ns)
Vth 3V	49	844	17.70
Vth 4V	47	675	19.07

Figure 5 Turn-on power. In red for Vth = 3V and in green for Vth = 4V

are reported the switch-on energy, power and current peaks.

Table 2 Switch-on energy

Switch-on energy			
	Eon (µJ)	IDS_{peak} (A)	$P_{SW(ON)peak}$ (kW)
Vth 3V	35.66	13.33	4
Vth 4V	37.56	12.73	3.8

The obtained results confirm that in terms of switch-on the higher threshold decrease the di/dt and dv/dt, increase the transition time (ton), reduce the current peak and consequently the power peak of the switch-on.

B. *Turn-off*

The simulation with single pulse test confirms that the toff for the device with higher Vth is shorter than the MOSFET with lower Vth. Similarly, the power's peak (green curve Fig. 7) and associated Eoff are respectively smaller for the higher Vth (Vth 4V). The gate resistances used for the test are Rgon = Rgoff = 10 Ω.

Figure 6 Waveforms for turn-off. On the top the case for Vth = 3V and on the bottom the case for Vth = 4V

Tale 3 and table 4 report the data respectively the first one in terms of di/dt and dv/dt and other one in terms of switch-off energy and power.

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Table 3 Switch-off data

Switch-off data			
	dv/dt (V/ns)	di/dt (A/µs)	toff (ns)
Vth 3V	43.60	655	10.11
Vth 4V	46	765	9.11

Figure 7 Turn-off power. In red for Vth = 3V and in green for Vth = 4V

The $P_{SW(OFF)}$'peak is lower for the device with higher Vth due to the faster speed of the drain current.

Table 4 Switch-off energy

Switch-off energy		
	Eoff (µJ)	$P_{SW(OFF)peak}$ (kW)
Vth 3V	11.12	2.2
Vth 4V	9.01	1.9

V. Switch Mode Power Supply

In this section a short overview on the typical stage of the modern switch mode power supply (SMPS) is done, in Fig. 8 are showed a typical composition of a SMPS [8] and are highlighted the PFC stage and the DC/DC stage.

Figure 8 Composition of a SMPS, with a special focus on the PFC and DC/DC stage

In red is highlighted the PFC stage with the capacitors of the DC link, in green the DC/DC stage, both share the capacitor of the DC link at the output of the PFC and it is the input of DC/DC stage.

The common topologies adopted in the PFC stage are essentially:

- Continuous current mode (CCM)
- Discontinues current mode (DCM)
- Interleaved
- Totem pole

Fig, 9 shown these topologies. Briefly, the role of the PFC is to boost up the voltage at the output of the rectifier bridge and to align the phase between current and voltage, the typical output voltage of a PFC is 400V. After the PFC stage a DC/DC converter is present, the role of this converter is to

Figure 9 Top: CCM PFC. Middle: Interleaved PFC. Bottom: Totem pole PFC

obtain the desired DC voltage at the output, at load level.

Figure 10 Top: Full Bridge LLC. Middle: Half Bridge LLC. Bottom: Phase Shift Full Bridge

The typical output voltage for server and telecom for example are in the range: 48 -12 V_{DC}. Nowadays in order to achieve even a higher power efficiency, the topologies adopted in this

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stage are resonant, Zero voltage switching (ZVS) or Zero current switching (ZCS), the main adopted is the ZVS topologies and in the specific, linked to the power level, the half bridge LLC, the full bridge LLC and the full bridge phase shift.

VI. V_{GSTH} IMPACTS ON PFC

In this section the impacts of the VGSth on the PFC converter [9] is discussed. As has been said before the higher threshold impacts the switching performance, in terms of energy, as disadvantages during turn-on, because increase this value and as advantages during turn-off, but other benefits come as showed in Fig. 11.

Figure 11 Turn-on waveforms in the PFC stage for the same device but with VGSth different, in DCM PFC

The higher threshold reduces the current peak, and moreover due to slower di/dt and dv/dt also the ringing on the VGS is smaller, both of these conditions help to improve the EMI [10] issue during the turn-on [11]. If the PCF is controlled in transition mode or in DCM, where the switch-on losses are smaller (as shown in Fig.11.) the reducing of current peak reduce the total switch-on losses.

Figure 12 Turn-off waveforms in the PFC stage for the same device but with VGSth different, in a DCM PFC

The switch-off energy is reduced by the 3%, this less energy involve in a reduction of the case temperature due to the smaller dissipation in terms of 1.5°C (f_{sw} = 97 kHz, $R_{thj-case}$ = 62.5 °C/W).

This gain in terms of less temperature is very useful in chargers and adaptors, with a power rating up to 300W.

VII. V_{GSTH} IMPACTS ON LLC

The advantages of a higher threshold in a DC/DC stage, especially in a LLC [12] (both half bridge or full bridge) are linked with the reduction of the switch-off energy. In the resonant converter due to the ZVS at the turn-on and the consequently no impacts of the reverse recovery effect of the MOSFET body diode, in order to reduce the PCB dimension and increase power density, the switching frequency is higher than PFC stage, in the range 140 – 300 kHz, at this frequency a small reduction of the switching energy involve a higher reduction of the case temperature.

In fact, a reduction of the 6.5% of the switching energy for a f_{sw} = 140 kHz with a $R_{thj-case}$ = 62.5 °C/W involve in a temperature reduction of 4 °C.

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Figure 13 Turn-off waveforms in the DC/DC stage for the same device but with VGSth different, in a HB LLC

Considering the entire power supply, PFC plus DC/DC, with the change of the Vth from 3V to 4V, a reduction of 5.5 °C is obtained.

VIII. Common Benefits and Drawback

Below is a summary of the benefits and drawbacks associated with a higher VGSth:

Benefits:

- Smaller turn-off time
- Lower switching losses at switch-off
- Higher immunity to false turn-on due to noise
- Lower gate oscillation

Drawbacks:

- Impact on gate driver
- Higher di/dt at switch-off

The threshold voltage sets the condition when the current starts to flow in the MOSFET; if there are disturbances in the converter or if the ground plane is weak, some current can flow on the gate resistance (through the parasitic gate to drain capacitance C_{GD}) and may create a voltage between gate and source terminals that could turn on the MOSFET and thus compromise the reliable operation of the entire system. Higher thresholds give higher immunity because the voltage required across Gate and Source (i.e., the product of RGon and noise current) to turn on the MOSFET is higher.

The higher threshold also mitigates the gate oscillation that occurs during turn-on and turn-off, which can improve the reliability of the device due to lower gate oxide stress.

A major drawback is the impact on the gate driver. In some lighting applications or chargers, the driving voltage is less than 10V; around 6 to 8 V. Figure 2, which shows the transfer characteristics of two devices with respective VGSth = 3V and 4V values, demonstrates that a higher threshold limits the current capability when the driver is unable to operate with 10V.

IX. Conclusion

In this paper, the impact of the V_{GS} threshold voltage of SJ MOSFETs has been analyzed evaluating the deriving benefits and drawbacks in modern SMPS converter when a MOSFET with higher threshold is used.

Depending by the topology adopted in the PFC stage, the converter could have significant switch-on losses (CCM, Totem Pole, …) or smaller, even negligible, losses at the turn-on (interleaved, DCM) thus, the higher V_{GSth} can helps in different aspects. On the other hand, if the designer aims to reduce the EMI issues, device with higher threshold should be used, otherwise, if the goal is to boost the power efficiency smaller VGSth must be chosen in the PFC stage.

On the contrary, for the DC/DC stage made by resonant converter LLC or ZVS the higher threshold helps to reduce the switch-off losses and the reducing of the case temperature, with the consequential possibility to adopt SMD packages.

Considering all the advantages and disadvantages of higher VGSth in resonant applications, it seems that this approach is the right option as it improves electrical and thermal performance, especially at light loads, and increases noise immunity as well as mitigating gate oscillation, this last consideration is valid also the PFC section obviously.

X. References

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