VNI4140K-32
Quad high-side smart power solid-state relay

Datasheet - production data

Features

<table>
<thead>
<tr>
<th>Type</th>
<th>$V_{demag}^{(1)}$</th>
<th>$R_{DS(on)}^{(1)}$</th>
<th>$I_{out}^{(1)}$</th>
<th>$V_{CC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>VNI4140K-32</td>
<td>$V_{CC}-41$ V</td>
<td>0.08 $\Omega$</td>
<td>1 A</td>
<td>41 V</td>
</tr>
</tbody>
</table>

1. Per channel

- Output current: 1 A per channel
- Shorted load protections
- Junction overtemperature protection
- Case overtemperature protection for thermal independence of the channels
- Thermal case shutdown restart not simultaneous for the various channels
- Protection against loss of ground
- Current limitation
- Undervoltage shutdown
- Open drain diagnostic outputs
- 3.3 V CMOS/TTL compatible inputs

Description

The VNI4140K-32 is a monolithic device made using STMicroelectronics VIPower technology, intended to drive four independent resistive, capacitive or inductive loads with one side connected to ground. Active current limitation avoids the system power supply dropping in case of shorted load. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. In overload conditions, the channel turns OFF and back ON automatically so to maintain junction temperature between $T_{TSD}$ and $T_R$. If this condition causes case temperature to reach $T_{CSD}$, the overloaded channel is turned OFF and restarts only when case temperature has decreased down to $T_{CR}$. In case of more than one channel in overload, restart of the overloaded channels is not simultaneous, in order to avoid high peak current from the supply. Non-overloaded channels continue operating normally. The open drain diagnostic outputs indicate overtemperature conditions.

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<td>22</td>
</tr>
<tr>
<td>17</td>
<td>PowerSSO-24 reel shipment (suffix “TR”)</td>
<td>23</td>
</tr>
<tr>
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1 Pin connection

Figure 2. Pin connection (top view)

Table 1. Pin description

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>Tab</td>
<td>TAB</td>
<td>Exposed tab internally connected to $V_{CC}$</td>
</tr>
<tr>
<td>1</td>
<td>$V_{CC}$</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>2</td>
<td>IN1</td>
<td>Channel 1 input 3.3 V CMOS/TTL compatible</td>
</tr>
<tr>
<td>3</td>
<td>STAT1</td>
<td>Channel 1 status in open drain configuration</td>
</tr>
<tr>
<td>4</td>
<td>IN2</td>
<td>Channel 2 input 3.3 V CMOS/TTL compatible</td>
</tr>
<tr>
<td>5</td>
<td>STA2</td>
<td>Channel 2 status in open drain configuration</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>Device ground connection</td>
</tr>
<tr>
<td>7</td>
<td>STAT3</td>
<td>Channel 3 status in open drain configuration</td>
</tr>
<tr>
<td>8</td>
<td>IN3</td>
<td>Channel 3 input 3.3 V CMOS/TTL compatible</td>
</tr>
<tr>
<td>9</td>
<td>STAT4</td>
<td>Channel 4 status in open drain configuration</td>
</tr>
<tr>
<td>10</td>
<td>IN4</td>
<td>Channel 4 input 3.3 V CMOS/TTL compatible</td>
</tr>
<tr>
<td>11</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>OUT4</td>
<td>Channel 4 power stage output, internally protected</td>
</tr>
<tr>
<td>14</td>
<td>OUT4</td>
<td>Channel 4 power stage output, internally protected</td>
</tr>
<tr>
<td>15</td>
<td>OUT4</td>
<td>Channel 4 power stage output, internally protected</td>
</tr>
<tr>
<td>16</td>
<td>OUT3</td>
<td>Channel 3 power stage output, internally protected</td>
</tr>
<tr>
<td>17</td>
<td>OUT3</td>
<td>Channel 3 power stage output, internally protected</td>
</tr>
<tr>
<td>Pin</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>------</td>
<td>-------------------------------------------------------</td>
</tr>
<tr>
<td>18</td>
<td>OUT3</td>
<td>Channel 3 power stage output, internally protected</td>
</tr>
<tr>
<td>19</td>
<td>OUT2</td>
<td>Channel 2 power stage output, internally protected</td>
</tr>
<tr>
<td>20</td>
<td>OUT2</td>
<td>Channel 2 power stage output, internally protected</td>
</tr>
<tr>
<td>21</td>
<td>OUT2</td>
<td>Channel 2 power stage output, internally protected</td>
</tr>
<tr>
<td>22</td>
<td>OUT1</td>
<td>Channel 1 power stage output, internally protected</td>
</tr>
<tr>
<td>23</td>
<td>OUT1</td>
<td>Channel 1 power stage output, internally protected</td>
</tr>
<tr>
<td>24</td>
<td>OUT1</td>
<td>Channel 1 power stage output, internally protected</td>
</tr>
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</table>
2 Maximum ratings

Table 2. Absolute maximum ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Power supply voltage</td>
<td>41 V</td>
<td></td>
</tr>
<tr>
<td>-VCC</td>
<td>Reverse supply voltage</td>
<td>-0.3 V</td>
<td></td>
</tr>
<tr>
<td>I_GND</td>
<td>DC ground reverse current</td>
<td>-250 mA</td>
<td></td>
</tr>
<tr>
<td>I_OUT</td>
<td>Output current (continuous)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_R</td>
<td>Reverse output current (per channel)</td>
<td>-5 A</td>
<td></td>
</tr>
<tr>
<td>I_IN</td>
<td>Input current (per channel)</td>
<td>± 10 mA</td>
<td></td>
</tr>
<tr>
<td>V_IN</td>
<td>Input voltage</td>
<td>+VCC V</td>
<td></td>
</tr>
<tr>
<td>V_STAT</td>
<td>Status pin voltage</td>
<td>+VCC V</td>
<td></td>
</tr>
<tr>
<td>I_STAT</td>
<td>Status pin current</td>
<td>± 10 mA</td>
<td></td>
</tr>
<tr>
<td>V_ESD</td>
<td>Electrostatic discharge (R = 1.5 kΩ; C = 100 pF)</td>
<td>2000 V</td>
<td></td>
</tr>
<tr>
<td>E_AS</td>
<td>EAS = 500 mA TAMB = 125 °C</td>
<td>5 J</td>
<td></td>
</tr>
<tr>
<td>P_TOT</td>
<td>Power dissipation at Tc = 25 °C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_J</td>
<td>Junction operating temperature</td>
<td>Internally limited</td>
<td>°C</td>
</tr>
<tr>
<td>T_STG</td>
<td>Storage temperature</td>
<td>-55 to 150 °C</td>
<td></td>
</tr>
</tbody>
</table>

2.1 Thermal data

Table 3. Thermal data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rth(JC)</td>
<td>Thermal resistance junction-case(^{(1)})</td>
<td>Max. 2</td>
<td>°C/W</td>
</tr>
<tr>
<td>Rth(JA)</td>
<td>Thermal resistance junction-ambient</td>
<td>Max.</td>
<td>see Figure 11</td>
</tr>
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</table>

1. Per channel.

3 Recommended

Table 4. Input switching limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_Vin</td>
<td>Maximum input switching frequency</td>
<td>10 kHz</td>
<td></td>
</tr>
</tbody>
</table>
4 Electrical characteristics

$10.5 \text{ V} < V_{CC} < 36 \text{ V}; -40 ^\circ\text{C} < T_J < 125 ^\circ\text{C}$; unless otherwise specified.

Table 5. Power section

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply voltage</td>
<td></td>
<td>10.5</td>
<td>36</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>ON state resistance</td>
<td>$I_{OUT} = 0.7 \text{ A}$ at $T_J = 25 ^\circ\text{C}$</td>
<td>0.080</td>
<td></td>
<td></td>
<td>$\Omega$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{OUT} = 0.7 \text{ A}$</td>
<td>0.140</td>
<td></td>
<td></td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$V_{clamp}$</td>
<td></td>
<td>$I_S = 20 \text{ mA}$</td>
<td>41</td>
<td>45</td>
<td>52</td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply current</td>
<td>All channels in OFF state, ON state with $V_{IN} = 5 \text{ V}$</td>
<td>250</td>
<td>2.4</td>
<td>4</td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$\text{mA}$</td>
</tr>
<tr>
<td>$V_{OUT(OFF)}$</td>
<td>OFF state output voltage</td>
<td>$V_{IN} = 0 \text{ V}$ and $I_{OUT} = 0 \text{ A}$</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>$I_{OUT(OFF)}$</td>
<td>OFF state output current</td>
<td>$V_{IN} = V_{OUT} = 0 \text{ V}$</td>
<td>0</td>
<td></td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>$I_{LGND}$</td>
<td>Output current in ground disconnection</td>
<td>$V_{CC} = V_{IN} = \text{GND} = 24 \text{ V}; T_J = 125 ^\circ\text{C}$</td>
<td></td>
<td></td>
<td></td>
<td>500</td>
</tr>
<tr>
<td>$F_{CP}$</td>
<td>Charge pump frequency</td>
<td>Channel in ON state(1)</td>
<td></td>
<td></td>
<td></td>
<td>1450</td>
</tr>
</tbody>
</table>

1. To cover EN55022 class A and class B normative.

$V_{CC} = 24 \text{ V}; -40 ^\circ\text{C} < T_J < 125 ^\circ\text{C}$; $R_L = 48 \Omega$, input rise time $< 0.1 \mu\text{s}$

Table 6. Switching

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_d(ON)$</td>
<td>Turn ON delay</td>
<td>-</td>
<td>6</td>
<td>-</td>
<td>$\mu\text{s}$</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise time</td>
<td>-</td>
<td>5</td>
<td>-</td>
<td>$\mu\text{s}$</td>
</tr>
<tr>
<td>$t_d(OFF)$</td>
<td>Turn OFF</td>
<td>-</td>
<td>12</td>
<td>-</td>
<td>$\mu\text{s}$</td>
</tr>
<tr>
<td>$t_f$</td>
<td>Fall time</td>
<td>-</td>
<td>5</td>
<td>-</td>
<td>$\mu\text{s}$</td>
</tr>
<tr>
<td>$dV/dt(ON)$</td>
<td>Turn ON voltage slope</td>
<td>-</td>
<td>4</td>
<td>-</td>
<td>$\text{V}/\mu\text{s}$</td>
</tr>
<tr>
<td>$dV/dt(OFF)$</td>
<td>Turn OFF voltage slope</td>
<td>-</td>
<td>4</td>
<td>-</td>
<td>$\text{V}/\mu\text{s}$</td>
</tr>
</tbody>
</table>
Figure 3. Switching parameter conventions

- $dV/dT$ - $t_{\text{rise}}$ - $t_{\text{fall}}$
- $t_{\text{dON}}$ - $t_{\text{dOFF}}$

- $V_{\text{out}}$ at 10%, 80%, 90%
- $V_{\text{in}}$ at 50%
- $V_{\text{out}}$ at 10%, 90%
### Table 7. Logical input

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Input low level voltage</td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input high level voltage</td>
<td></td>
<td>2.20</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{I(HYST)}$</td>
<td>Input hysteresis</td>
<td></td>
<td>0.15</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input current</td>
<td>$V_{IN} = 15 \text{ V}$</td>
<td>10</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 36 \text{ V}$</td>
<td>210</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 8. Protection and diagnostic

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{STAT}$</td>
<td>Status voltage output low</td>
<td>$I_{STAT} = 1.6 \text{ mA}$</td>
<td>0.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{USD}$</td>
<td>Undervoltage protection</td>
<td></td>
<td>7</td>
<td>10.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{USDHY}$</td>
<td>Undervoltage hysteresis</td>
<td></td>
<td>0.4</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{LIM}$</td>
<td>DC short-circuit current</td>
<td>$V_{CC} = 24 \text{ V}; R_{LOAD} &lt; 10 \text{ mΩ}$</td>
<td>1.1</td>
<td>2.6</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$I_{PEAK}$</td>
<td>Maximum DC output current</td>
<td>Dynamic load</td>
<td>1.6</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$I_{LSTAT}$</td>
<td>Status leakage current</td>
<td>$V_{CC} = V_{STAT} = 36 \text{ V}$</td>
<td>30</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$T_{TSD}$</td>
<td>Junction shutdown temperature</td>
<td></td>
<td>150</td>
<td>170</td>
<td>190</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{R}$</td>
<td>Junction reset temperature</td>
<td></td>
<td>135</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$T_{HIST}$</td>
<td>Junction thermal hysteresis</td>
<td></td>
<td>7</td>
<td>15</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$T_{CSD}$</td>
<td>Case shutdown temperature</td>
<td></td>
<td>125</td>
<td>130</td>
<td>135</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{CR}$</td>
<td>Case reset temperature</td>
<td></td>
<td>110</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$T_{CHYST}$</td>
<td>Case thermal hysteresis</td>
<td></td>
<td>7</td>
<td>15</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$V_{demag}$</td>
<td>Output voltage at turn-OFF</td>
<td>$I_{OUT} = 0.5 \text{ A}; L_{LOAD} &gt;= 1 \text{ mH}$</td>
<td>$V_{CC} - 41$</td>
<td>$V_{CC} - 45$</td>
<td>$V_{CC} - 52$</td>
<td>V</td>
</tr>
</tbody>
</table>
Figure 4. Current and voltage conventions

[Diagram showing current and voltage conventions with labels: \( I_{INi} \), \( I_{STAT} \), \( I_{OUTi} \), \( V_{INi} \), \( V_{STAT} \), \( GND \), \( V_{OUTi} \), \( V_{CC} \), \( I_{CC} \), \( I_{GND} \).]
## 5 Truth table

### Table 9. Truth table

<table>
<thead>
<tr>
<th>Conditions</th>
<th>INPUTn</th>
<th>OUTPUTn</th>
<th>STATUSn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal operation</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Overtemperature</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Undervoltage</td>
<td>L</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>Shorted load (current limitation before thermal shutdown)</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>X</td>
<td>H</td>
</tr>
</tbody>
</table>
6 Thermal management

The power dissipation in the IC is the main factor that sets the safe operating condition of the device in the application. Therefore, it must be considered very carefully. Furthermore, the available space on the PCB should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness. Two different protections have been implemented to guarantee safety of the device if it overheats due to an overloaded condition or high environment temperature. The following flowchart explains in detail this protection functionality.

**Figure 5. Thermal behavior**
7 Switching waveforms

Figure 6. Switching waveforms
8 Pin functions

Figure 7. Input circuit

Figure 8. Status circuit
Figure 9. Charge pump switching frequency (typical) vs. temperature
9 Package and PCB thermal data

9.1 VNI4140K-32 thermal data

**Figure 10. VNI4140K-32 PCB**

Note: Layout condition of $R_{th}$ and $Z_{th}$ measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70 mm (front and back side), copper areas: from minimum pad layout to 8 cm²).

**Figure 11. $R_{th}(JA)$ vs. PCB copper area in open box free air condition (one channel ON)**
Figure 12. VNI4140K-32 thermal impedance junction-ambient single pulse (one channel ON)
10 Reverse polarity protection

Reverse polarity protection can be implemented on board using two different solutions:
1. Placing a resistor (R_GND) between IC GND pin and load GND
2. Placing a diode between IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to the following equation:

**Equation 1**

\[ R_{GND} \geq \frac{V_{CC}}{I_{GND}} \]

where \( I_{GND} \) is the DC reverse ground pin current and can be found in *Section 2: Maximum ratings* of this datasheet.

Power dissipated by \( R_{GND} \) (when \( V_{CC} < 0 \): during reverse polarity situations) is:

**Equation 2**

\[ P_D = \frac{V_{CC}^2}{R_{GND}} \]

If option 2 is selected, the diode has to be chosen by taking into account \( V_{RRM} > |V_{CC}| \) and its power dissipation capability:

**Equation 3**

\[ P_D \geq I_S \cdot V_F \]

*Note:* In normal conditions (no reverse polarity), due to the diode, there is a voltage drop between GND of the device and GND of the system.

**Figure 13. Reverse polarity protection**

This schematic can be used with any type of load.
11 Demagnetization energy

Figure 14. Maximum demagnetization energy vs. load current, typical values

- Single channel demagnetization
- Four channels demagnetization

- $E_{off}$ (J)
- $I_{out}$ (A)

Tamb = 125 °C
12 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 10. PowerSSO-24 mechanical data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>mm</th>
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</thead>
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<tr>
<td></td>
<td>Min.</td>
</tr>
<tr>
<td>A</td>
<td>2.15</td>
</tr>
<tr>
<td>A2</td>
<td>2.15</td>
</tr>
<tr>
<td>a1</td>
<td>0</td>
</tr>
<tr>
<td>b</td>
<td>0.33</td>
</tr>
<tr>
<td>c</td>
<td>0.23</td>
</tr>
<tr>
<td>D</td>
<td>10.10</td>
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<tr>
<td>E</td>
<td>7.4</td>
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<tr>
<td>e</td>
<td></td>
</tr>
<tr>
<td>e3</td>
<td></td>
</tr>
<tr>
<td>G</td>
<td></td>
</tr>
<tr>
<td>G1</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>10.1</td>
</tr>
<tr>
<td>h</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.55</td>
</tr>
<tr>
<td>N</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>4.1</td>
</tr>
<tr>
<td>Y</td>
<td>6.5</td>
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</table>
Figure 15. PowerSSO-24 package dimensions

Figure 16. PowerSSO-24 tube shipment (no suffix)

Table 11. PowerSSO-24 tube shipment

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Base quantity</td>
<td>49</td>
</tr>
<tr>
<td>Bulk quantity</td>
<td>1225</td>
</tr>
<tr>
<td>Tube length (± 0.5)</td>
<td>532</td>
</tr>
<tr>
<td>A</td>
<td>3.5</td>
</tr>
<tr>
<td>B</td>
<td>13.8</td>
</tr>
<tr>
<td>C (± 0.1)</td>
<td>0.6</td>
</tr>
</tbody>
</table>

Note: All dimensions are in mm.
Figure 17. PowerSSO-24 reel shipment (suffix “TR”)

Table 12. PowerSSO-24 reel dimensions

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
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<tr>
<td>Base quantity</td>
<td>1000</td>
</tr>
<tr>
<td>Bulk quantity</td>
<td>1000</td>
</tr>
<tr>
<td>A (max.)</td>
<td>330</td>
</tr>
<tr>
<td>B (min.)</td>
<td>1.5</td>
</tr>
<tr>
<td>C (± 0.2)</td>
<td>13</td>
</tr>
<tr>
<td>F</td>
<td>20.2</td>
</tr>
<tr>
<td>G (2 ± 0)</td>
<td>24.4</td>
</tr>
<tr>
<td>N (min.)</td>
<td>100</td>
</tr>
<tr>
<td>T (max.)</td>
<td>30.4</td>
</tr>
</tbody>
</table>
Table 13. PowerSSO-24 tape dimensions

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Tape width</td>
<td>W</td>
<td>24</td>
</tr>
<tr>
<td>Tape hole spacing</td>
<td>P0 (± 0.1)</td>
<td>4</td>
</tr>
<tr>
<td>Component spacing</td>
<td>P</td>
<td>12</td>
</tr>
<tr>
<td>Hole diameter</td>
<td>D (± 0.05)</td>
<td>1.55</td>
</tr>
<tr>
<td>Hole diameter</td>
<td>D1 (min.)</td>
<td>1.5</td>
</tr>
<tr>
<td>Hole position</td>
<td>F (± 0.1)</td>
<td>11.5</td>
</tr>
<tr>
<td>Compartment depth</td>
<td>K (max.)</td>
<td>2.85</td>
</tr>
<tr>
<td>Hole spacing</td>
<td>P1 (± 0.1)</td>
<td>2</td>
</tr>
</tbody>
</table>

Figure 19. VNI4140K-32 suggested footprint

Note: STMicroelectronics is not responsible for any PCB related issues. The footprint shown in the above figure is a suggestion which might not be in line to the customer PCB supplier design rules.

All dimensions are in mm.
13 Ordering information

<table>
<thead>
<tr>
<th>Order codes</th>
<th>Package</th>
<th>Packaging</th>
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</thead>
<tbody>
<tr>
<td>VNI4140K-32</td>
<td>PowerSSO-24</td>
<td>Tube</td>
</tr>
<tr>
<td>VNI4140KTR-32</td>
<td>PowerSSO-24</td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>
## Revision history

Table 15. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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</thead>
<tbody>
<tr>
<td>12-Dec-2011</td>
<td>1</td>
<td>Initial release.</td>
</tr>
<tr>
<td>06-Feb-2012</td>
<td>2</td>
<td>Updated $I_{IM}$ minimum value in Table 8: Protection and diagnostic.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Inserted new feature: ESD according to IEC 61000-4-2 up to +/-25 KV, in cover page.</td>
</tr>
<tr>
<td>07-Mar-2012</td>
<td>3</td>
<td>Suggested footprint inserted. In Table 5, parameter $I_{огND}$ has been added.</td>
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<tr>
<td>25-Mar-2013</td>
<td>4</td>
<td>Updated $I_{LIM}$ minimum value in Table 8. Minor text changes.</td>
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<tr>
<td>06-Nov-2013</td>
<td>5</td>
<td>Updated $E_{AS}$ value in Table 2: Absolute maximum ratings. Added Figure 14.</td>
</tr>
<tr>
<td>11-Dec-2013</td>
<td>6</td>
<td>Updated Section 10.</td>
</tr>
</tbody>
</table>
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