SATAULC6-2M6

Ultra low capacitance ESD protection

Datasheet - production data

µQFN (pin view)
SATAULC6-2M6

Features

- 2-line ESD protection (at 15 kV air and contact discharge, exceeds IEC 61000-4-2)
- Protects V_{BUS} when applicable
- Ultra low capacitance: 0.9 pF @ 825 MHz
- Fast response time
- µQFN package
- RoHS compliant

Benefits

- ESD protection of V_{BUS} when applicable
- Optimized rise and fall times for maximum data integrity
- Large bandwidth to minimize impact on data signal quality
- Consistent differential signal balance:
  - Ultra low impact on intra- and inter-pair skew
  - Matching high bit rate SATA, DVI, HDMI and IEEE 1394 requirements
- Low PCB space occupation - 1.45 mm^2 for µQFN
- Low leakage current for longer operation of battery powered devices
- Higher reliability offered by monolithic integration
- Designed for go-through layout

Complies with these standards

- IEC 61000-4-2 level 4
  - 15 kV air discharge
  - 8 kV contact discharge
- MIL STD883G-Method 3015-7

Applications

- SATA port up to 3 Gb/s
- DVI and HDMI ports up to 1.65 Gb/s
- IEEE 1394a and b (Firewire) ports up to 1.6 Gb/s
- USB 2.0 ports up to 480 Mb/s (Hi-Speed), backwards compatible with USB 1.1 low and full speed
- Ethernet port: 10/100/1000 Mb/s
- SIM card protection
- Video line protection
- Portable electronics

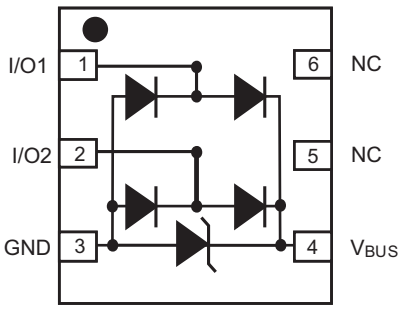
Description

The SATAULC6-2M6 is a monolithic, application specific discrete device dedicated to ESD protection of high speed interfaces.

Its very low line capacitance secures a high level of signal integrity. The device topology provides this integrity without compromising the complete protection of ICs against the most stringent ESD strikes.

1 Characteristics

Figure 1. Functional diagram



µQFN 6 leads

Table 1. Absolute ratings

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 air discharge IEC 61000-4-2 contact discharge MIL STD883G-Method 3015-7	±15 ±15 ±25	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Maximum junction temperature		125	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max	
I_{RM}	Leakage current	V_{RM} = 5 V			0.5	µA
V_{BR}	Breakdown voltage between V_{BUS} and GND	I_R = 1 mA	6			V
V_{CL}	Clamping voltage	I_{PP} = 1 A, t_p = 8/20 µs Any I/O pin to GND			12	V
		I_{PP} = 5 A, t_p = 8/20 µs Any I/O pin to GND			19	V
$C_{i/o-i/o}$	Capacitance between I/O	V_R = 0 V, F = 825 MHz GND not connected			0.45	pF
$C_{i/o-GND}$	Capacitance between I/O and GND	V_R = 0 V, F = 825 MHz Any I/0 pin to GND			0.9	pF
$\Delta C_{i/o-GND}$	Capacitance variation between I/O and GND	V_R = 0 V, F = 1 MHz		0.08		pF

Figure 2. Line capacitance versus frequency (typical values)

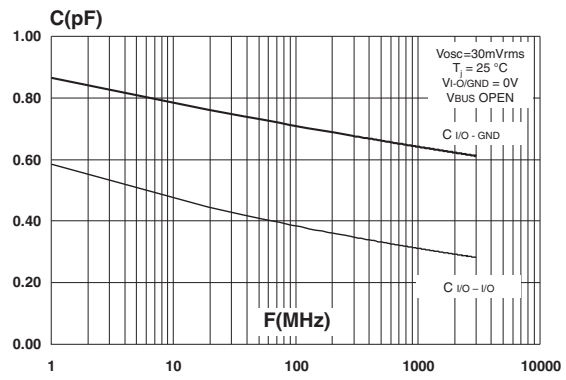


Figure 3. Attenuation (typical values)

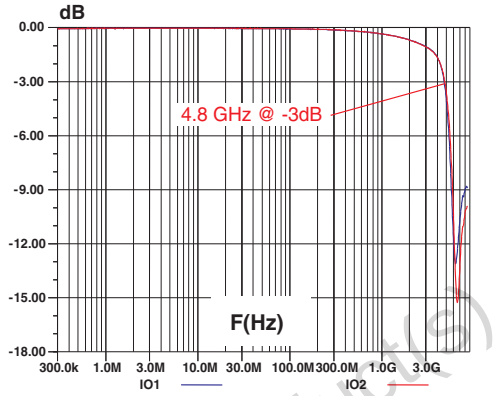


Figure 4. Eye diagram at 1.5 Gbps PCB + device

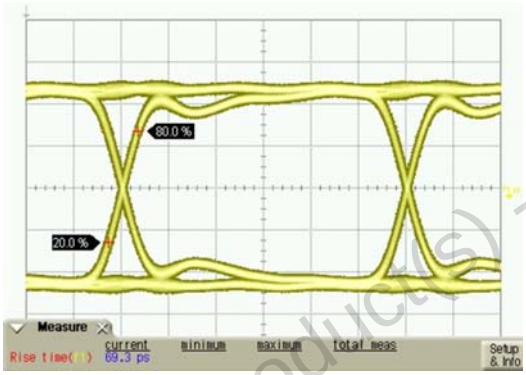


Figure 5. Eye diagram at 1.5 Gbps PCB only

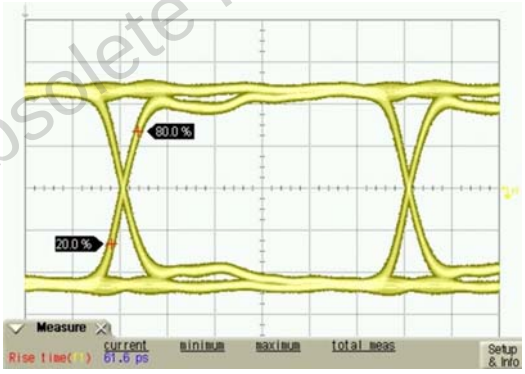


Figure 6. Eye diagram at 3.0 Gbps PCB only

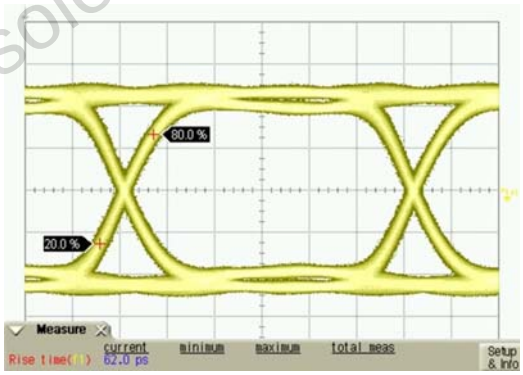
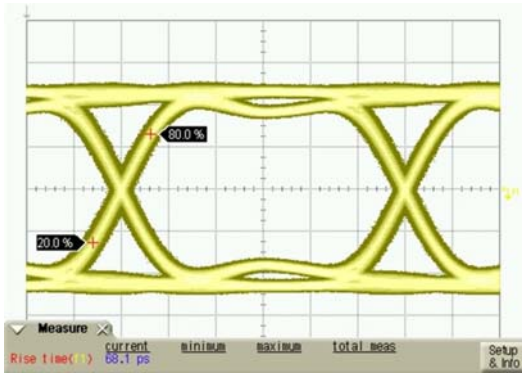
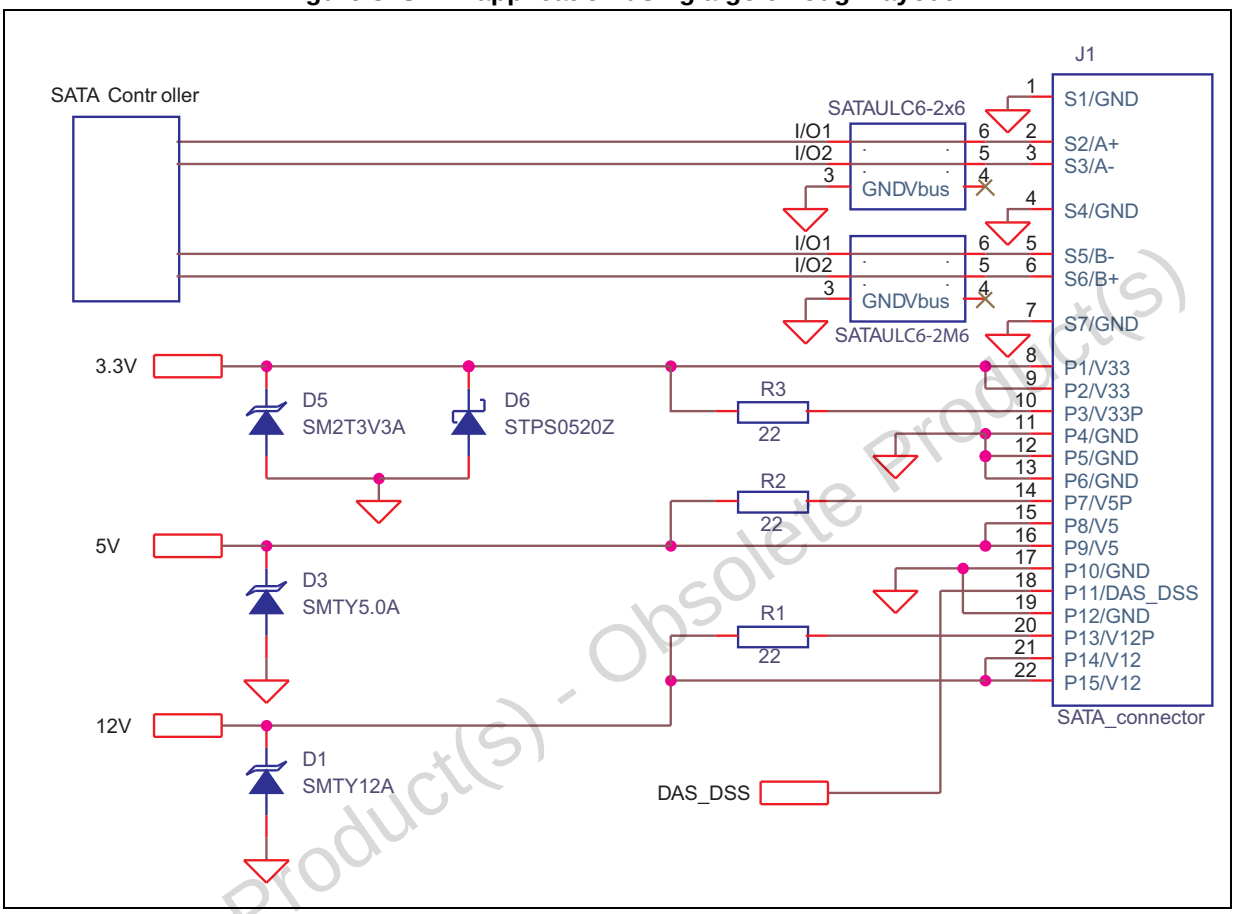


Figure 7. Eye diagram at 3.0 Gbps PCB + device



2 Application example

Figure 8. SATA application using a go-through layout

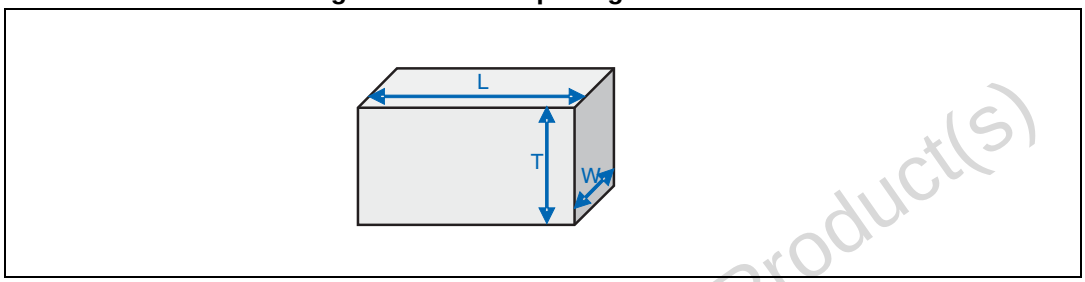


3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness)

Figure 9. Stencil opening dimensions



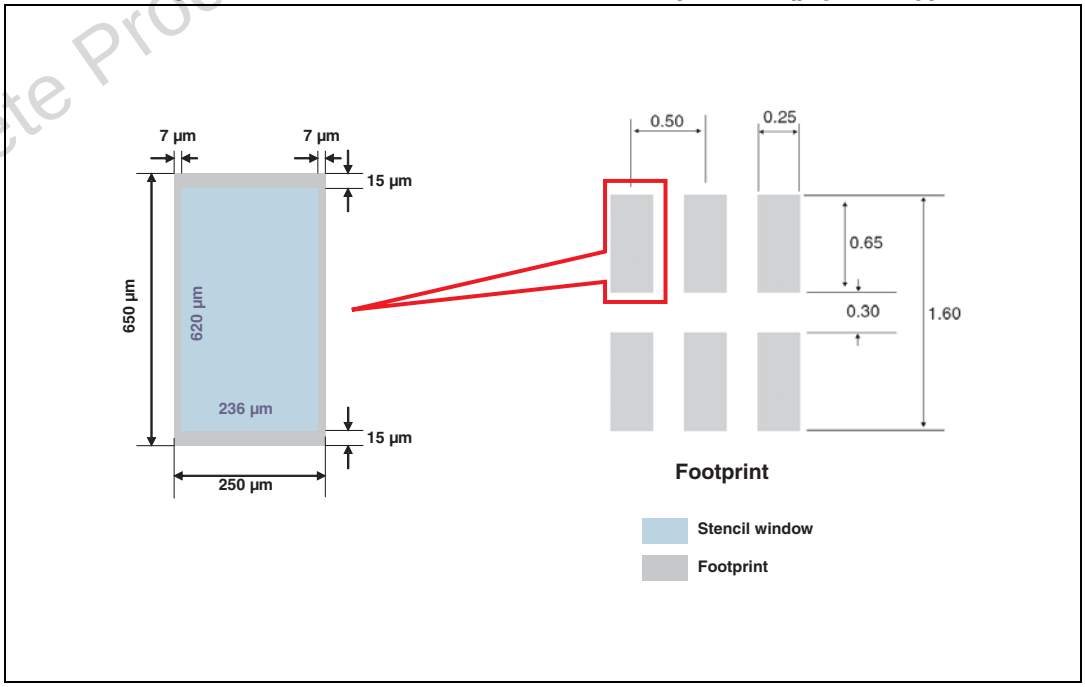
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 10. Recommended stencil window position (µQFN only)



3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

3.3 Placement

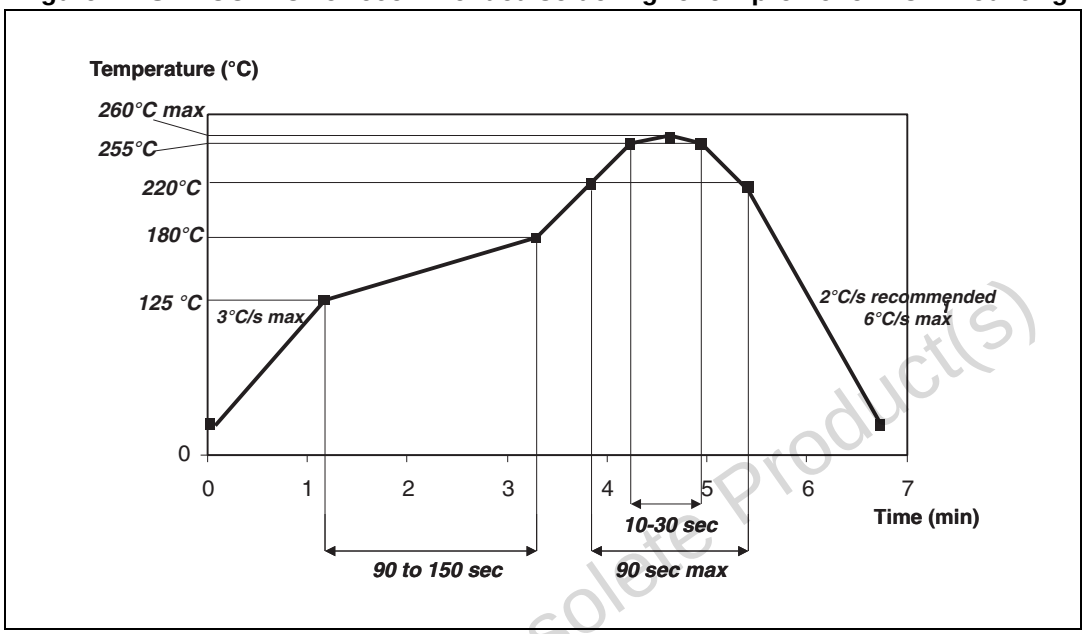
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

3.5 Reflow profile

Figure 11. ST ECOPACK® recommended soldering reflow profile for PCB mounting



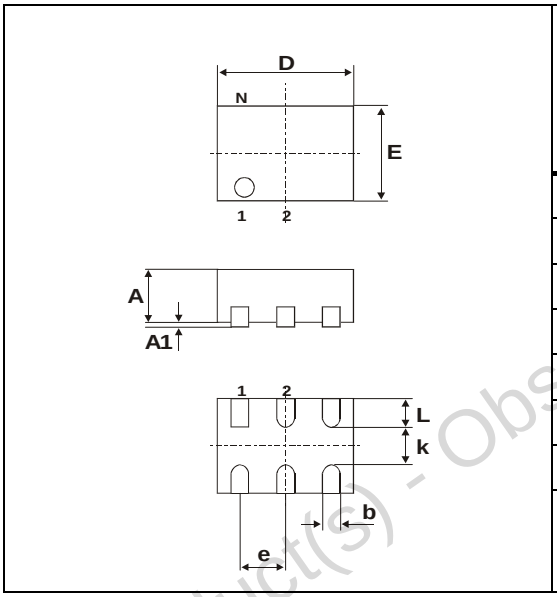
Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Package information

- Epoxy meets UL94, V0

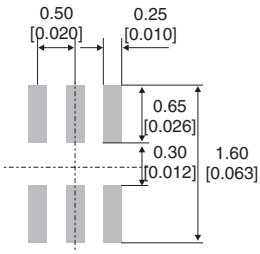
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. Micro QFN 1.45x1.00 6L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D		1.45			0.057	
E		1.00			0.039	
e		0.50			0.020	
K	0.20			0.008		
L	0.30	0.35	0.40	0.012	0.014	0.016

Figure 12. µQFN 6 leads footprint dimensions in mm [inches]



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
SATAULC6-2M6	S(1)	µQFN 6 leads	2.17 mg	3000	Tape and reel

1. The marking can be rotated by 90° to differentiate assembly location.

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
08-Dec-2008	1	First issue
07-Oct-2015	2	Removed device in SOT-666. Updated document accordingly.

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