ESDALC6V1-1BM2

Single line low capacitance Transil™ for ESD protection

Features

- single line low capacitance Transil diode
- bidirectional ESD protection
- ESD protection > 30 kV (IEC 61000-4-2 contact discharge)
- breakdown voltage \( V_{BR} = 6.1 \text{ V min.} \)
- low diode capacitance (22 pF typ. at 0 V)
- low leakage current < 100 nA at 3 V
- very small PCB area 0.6 mm\(^2\)
- lead-free package

Benefits

- high ESD protection level
- high integration
- suitable for high density boards

Complies with the following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G - Method 3015-7, class 3B:
  - Human body model

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- computers
- printers
- communication systems
- cellular phone handsets and accessories
- video equipment

Description

The ESDALC6V1-1BM2 is a bidirectional single line TVS diode designed to protect the data lines or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

TM: Transil is a trademark of STMicroelectronics
1 Characteristics

Table 1. Absolute maximum ratings (T<sub>amb</sub> = 25 °C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;PP&lt;/sub&gt;&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>Peak pulse voltage (IEC 61000-4-2 contact discharge)</td>
<td>± 30</td>
<td>kV</td>
</tr>
<tr>
<td>P&lt;sub&gt;PP&lt;/sub&gt;&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>Peak pulse power dissipation (8/20 µs)</td>
<td>140</td>
<td>W</td>
</tr>
<tr>
<td>I&lt;sub&gt;PP&lt;/sub&gt;</td>
<td>Repetitive peak pulse current (8/20 µs)</td>
<td>9</td>
<td>A</td>
</tr>
<tr>
<td>T&lt;sub&gt;J&lt;/sub&gt;</td>
<td>Junction temperature</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>T&lt;sub&gt;stg&lt;/sub&gt;</td>
<td>Storage temperature range</td>
<td>- 55 to + 150</td>
<td>°C</td>
</tr>
<tr>
<td>T&lt;sub&gt;L&lt;/sub&gt;</td>
<td>Maximum lead temperature for soldering during 10 s</td>
<td>260</td>
<td>°C</td>
</tr>
<tr>
<td>T&lt;sub&gt;OP&lt;/sub&gt;</td>
<td>Operating temperature range</td>
<td>- 40 to + 125</td>
<td>°C</td>
</tr>
</tbody>
</table>

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

Table 2. Electrical characteristics

<table>
<thead>
<tr>
<th>Order code</th>
<th>V&lt;sub&gt;BR&lt;/sub&gt; @ I&lt;sub&gt;R&lt;/sub&gt;</th>
<th>I&lt;sub&gt;RM&lt;/sub&gt; @ V&lt;sub&gt;RM&lt;/sub&gt;</th>
<th>R&lt;sub&gt;d&lt;/sub&gt;</th>
<th>αT</th>
<th>C@0 V Bias</th>
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<tbody>
<tr>
<td></td>
<td>min.</td>
<td>max.</td>
<td>max.</td>
<td>typ.</td>
<td>max.</td>
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<tr>
<td>V</td>
<td>V</td>
<td>mA</td>
<td>nA</td>
<td>V</td>
<td>Ω</td>
</tr>
<tr>
<td>ESDALC6V1-1BM2</td>
<td>6.1</td>
<td>8.0</td>
<td>1</td>
<td>100</td>
<td>3</td>
</tr>
</tbody>
</table>

Symbol Parameter

V<sub>BR</sub> = Breakdown voltage
V<sub>RM</sub> = Stand-off voltage
V<sub>CL</sub> = Clamping voltage
I<sub>RM</sub> = Leakage current @ V<sub>RM</sub>
I<sub>PP</sub> = Peak pulse current
V<sub>F</sub> = Forward voltage drop
Figure 3. Relative variation of peak pulse power versus initial junction temperature

Figure 4. Peak pulse power versus exponential pulse duration

Figure 5. Clamping voltage versus peak pulse current (typical values)

Figure 6. Junction capacitance versus reverse voltage applied (typical values)

Figure 7. Relative variation of leakage current versus junction temperature (typical values)

Figure 8. ESD response to IEC 61000-4-2 (+15 kV air discharge) on each channel
2 Ordering information scheme

Figure 9. ESD response to IEC 61000-4-2 (-15 kV air discharge) on each channel

Figure 10. S21 attenuation measurement result

ESDA   LC   6V1 - 1   B   M2

ESD array
Low capacitance
Breakdown voltage
6V1 = 6.1 volts min.
Number of lines
Directional
B = bidirectional
Package
M2 = SOD882
3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. SOD882 dimensions

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Dimensions</th>
<th>Millimeters</th>
<th>Inches</th>
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<tbody>
<tr>
<td></td>
<td>A</td>
<td>0.40</td>
<td>0.016</td>
</tr>
<tr>
<td></td>
<td>A1</td>
<td>0.00</td>
<td></td>
</tr>
<tr>
<td></td>
<td>b1</td>
<td>0.20</td>
<td>0.008</td>
</tr>
<tr>
<td></td>
<td>b2</td>
<td>0.20</td>
<td>0.008</td>
</tr>
<tr>
<td></td>
<td>D</td>
<td>1.00</td>
<td>0.039</td>
</tr>
<tr>
<td></td>
<td>E</td>
<td>0.60</td>
<td>0.024</td>
</tr>
<tr>
<td></td>
<td>e</td>
<td>0.65</td>
<td></td>
</tr>
<tr>
<td></td>
<td>L1</td>
<td>0.45</td>
<td>0.018</td>
</tr>
<tr>
<td></td>
<td>L2</td>
<td>0.45</td>
<td>0.018</td>
</tr>
</tbody>
</table>

Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 12. Footprint (dimensions in mm) Figure 13. Marking
Figure 14. Tape and reel specifications

All dimensions in mm

User direction of unreeling
4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

   Figure 15. Stencil opening dimensions

   b) General design rule
      Stencil thickness (T) = 75 ~ 125 µm
      Aspect Ratio = \( \frac{W}{T} \geq 1.5 \)
      Aspect Area = \( \frac{L \times W}{2T(L + W)} \geq 0.66 \)

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio - between 60% and 65%.

   Figure 16. Recommended stencil windows position

4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.
4.3 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

**Figure 17. ST ECOPACK recommended soldering reflow profile for PCB mounting**

![Reflow profile diagram](image)

**Note:** Minimize air convection currents in the reflow oven to avoid component movement.
5 Ordering information

Table 4. Ordering information

<table>
<thead>
<tr>
<th>Order code</th>
<th>Marking</th>
<th>Package</th>
<th>Weight</th>
<th>Base qty</th>
<th>Delivery mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESDALC6V1-1BM2</td>
<td>P(1)</td>
<td>SOD882</td>
<td>0.89 mg</td>
<td>12000</td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>

1. The marking can be rotated by 90° to differentiate assembly location

6 Revision history

Table 5. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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<td>11-Jan-2007</td>
<td>1</td>
<td>Initial release.</td>
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<tr>
<td>1-Apr-2007</td>
<td>2</td>
<td>Reformatted to current standards. Added Figure 13.: Marking. Updated Figure 14.: Tape and reel specifications. Added Section 4: Recommendation on PCB assembly.</td>
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<tr>
<td>02-Dec-2010</td>
<td>3</td>
<td>Updated base quantity Table 4.</td>
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