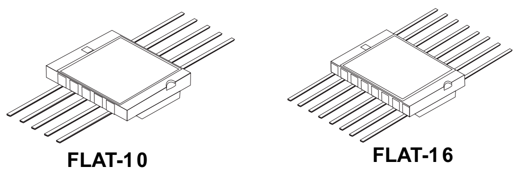
RHFPM4424

Rad-hard 4.5 A dual low-side MOSFET driver

Datasheet - production data



Features

- Wide operating voltage range: 4.5 V to 18 V
- Parallel driving capability up to 9 A
- Non-inverting configuration
- Input 5 V logic level compatibility
- 110 ns typical propagation delay
- Matched propagation delays between the two channels (5 ns max.)
- 20 mV maximum low level output voltage
- 30 ns rise and fall times
- +/-5 V common mode bouncing between signal and power grounds
- TID:
  - 300 krad HDR
  - 100 krad LDR
- QML-V qualification planned
- Hermetic package

Applications

- Switch mode power supply
- DC-DC converters
- Motor controllers
- Line drivers

Description

The RHFPM4424 is a flexible, high-frequency dual low-side driver specifically designed to work with high capacitive MOSFETs and IGBTs in a high radiation environment such as the aerospace.

The RHFPM4424 outputs can sink and source 4.5 A of peak current independently. By putting in parallel the two PWM outputs, a higher driving current (up to 9 A peak) can be obtained.

The RHFPM4424 works with CMOS/TTL compatible PWM signal so it can be driven by an external PWM controller, for instance the ST1843 or the ST1845. The hermetic FLAT-16 version has an industry standard pinout and it can dissipate up to 1.5 W (750 mW per channel), while FLAT-10 version optimizes the PCB real estate. Both of packages are hermetic, making the device well-suited for any kind of harsh environment.

Table 1. Device summary(1)

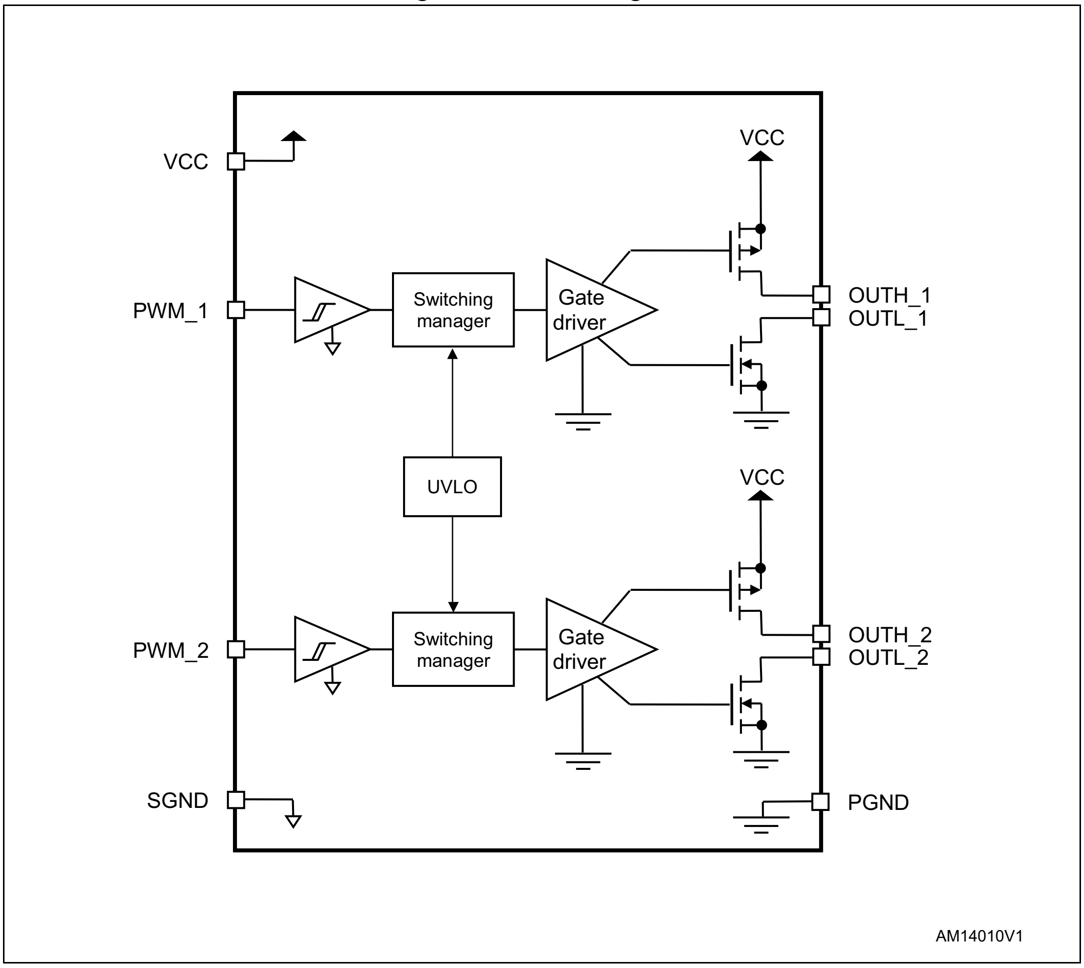
Order codes	SMD pin	Quality level	EPPL	Package	Max. power dissipation [mW]	Mass [g]	Temperature range
RHFPM4424LK1(2)	-	Engineering model	-	FLAT-10	200	0.7	-55 to 125 °C
RHFPM4424K1	-	Engineering model	-	FLAT-16	550	0.7	-55 to 125 °C

1. Contact ST sales office for information about the die specific conditions and for other quality levels.
2. Under development.

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin configuration (top view)

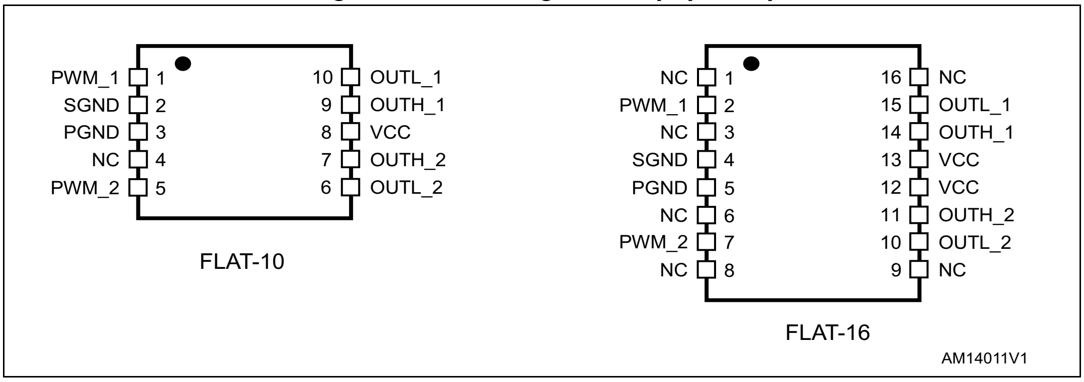


Table 2. Pin description

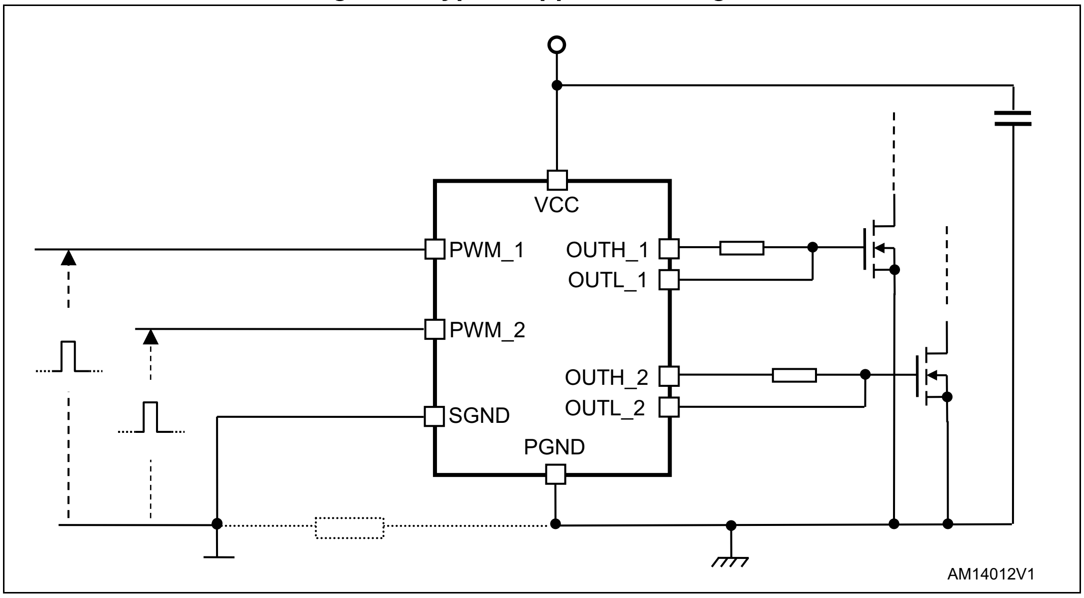
Pin		Name	Type	Description
FLAT-10	FLAT-16			
8	12 13	VCC	Supply	Supply voltage. Bypass with low ESR (for example MLCC type) capacitor to the PCB ground plane.
3	5	PGND	Ground	Ground reference for output drivers. Connect this pin to the PCB ground plane.
2	4	SGND	Ground	Ground reference for PWM input pins. Input pin (PWM_1, PWM_2 and SGND) common mode can range +/-5 V versus PGND.
1	2	PWM_1	I	PWM input signal (non-inverting) for driver 1 featuring TTL/CMOS compatible threshold and hysteresis. Don't leave the pin floating.
5	7	PWM_2	I	PWM input signal (non-inverting) for driver 2 featuring TTL/CMOS compatible threshold and hysteresis. Don't leave the pin floating.
9	14	OUTH_1	O	High-side open drain pin of driver 1. Connect this pin to OUTL_1 either directly or by an external resistor if an asymmetric ON/OFF switching time is desired.
10	15	OUTL_1	O	Low-side open drain pin of driver 1. Connect this pin to OUTH_1 either directly or by an external resistor if an asymmetric ON/OFF switching time is desired.
7	11	OUTH_2	O	High-side open drain pin of driver 2. Connect this pin to OUTL_2 either directly or by an external resistor if an asymmetric ON/OFF switching time is desired.

Table 2. Pin description (continued)

Pin		Name	Type	Description
FLAT-10	FLAT-16			
6	10	OUTL_2	O	Low-side open drain pin of driver 2. Connect this pin to OUTH_2 either directly or by an external resistor if an asymmetric ON/OFF switching time is desired.
4	1 3 6 9 16	NC		Not connected pin. Leave it floating or connect it to any potential.

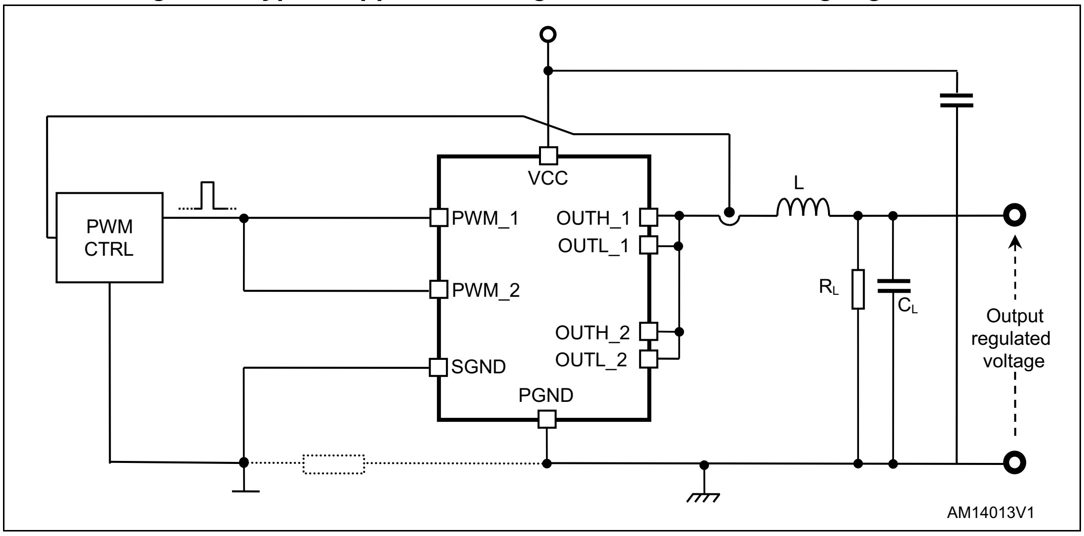
3 Typical application diagram

Figure 3. Typical application diagram



Note: SGND and PGND can be shorted or decoupled up to +/-5 V.

Figure 4. Typical application diagram as buck switching regulator



Note: SGND and PGND can be shorted or decoupled up to +/-5 V.

In Figure 4, the output stage of the RHFPM4424 device directly drives an inductor; in this configuration, the RHFPM4424 output stages are in parallel to exploit the maximum current capability of the device. The MOSFET driver works as a synchronous buck converter.

4 Absolute maximum ratings

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		FLAT-10	FLAT-16	
R_{thjc}	Max. thermal resistance, junction-to-case	25	8	°C/W
P_{TOT}	Maximum power dissipation @ T_{amb} = 70 °C	1.0	1.5	W

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage	PGND-0.3 to PGND+20	V
PGND	Power ground	-	V
SGND	Signal ground	PGND-5 to PGND+5	V
PWM_1 PWM_2	PWM input	SGND-0.3 to VCC+0.3	V
OUT_1 OUT_2	Driver output	PGND-0.3 to VCC+0.3	V
I_{OUT}	DC output current (for each driver)	750	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_J	Maximum operating junction temperature	150	°C
T_{LEAD}	Lead temperature (soldering, 10 seconds)(1)	300	°C
V_{HBM}	ESD capability, human body model	2000	V
V_{MM}	ESD capability, machine model	200	V

1. The distance is 1.5 mm far from the device body and the same lead is resoldered after 3 minutes.

5 Electrical characteristics

V_{CC} = 4.5 V to 18 V and T_J = -55 to 125 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	V_{CC} quiescent current	VCC = 18 V Inputs not switching OUTH_1 ≡ OUTL_1 OUTH_2 ≡ OUTL_2 T_j = 25 °C		1.2	1.8	mA
V_{UVLO}	Undervoltage lockout threshold for turn-on	VCC rising		4.3	4.5	V
	Undervoltage lockout hysteresis			300		mV
Input stage						
PWM_x	Input at high level – V_{IH}	Rising threshold	2.0			V
	Input at low level – V_{IL}	Falling threshold			0.8	V
I_{PWM}	PWM_x input pin current	PWMx = SGND	-1		+1	µA
		PWM_x = 3.3 V VCC = 10 V and 18 V	0		+2	µA
		PWM_x = VCC-0.5 V VCC = 18 V	0		+5	µA
dV_{PWM}/dt	PWM_x input pin transient(1)		100			mV/s
Output stage						
R_{hi}	Source resistance	VCC = 10 V Inputs at high level I_{OUT} = 100 mA T_j = 25 °C		0.7	1.0	Ω
		VCC = 10 V Inputs at high level I_{OUT} = 100 mA			1.4	Ω
R_{lo}	Sink resistance	VCC = 10 V Inputs at low level I_{OUT} = 100 mA T_j = 25 °C		1.0	1.4	Ω
		VCC = 10 V Inputs at low level I_{OUT} =100 mA			2.0	Ω
I_{SOURCE}	Source peak current(1)	VCC = 10 V Inputs at high level C_{OUT} to GND = 10 nF		5.5		A

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SINK}	Sink peak current[(1)]	VCC = 10 V Inputs at low level C_{OUT} to GND = 10 nF		4.5		A
V_{OH}	High level output voltage, VCC-V_{OUT}	Inputs at high level OUTH_1 ≡ OUTL_1 OUTH_2 ≡ OUTL_2 I_{OUT} = 1 mA			20	mV
V_{OL}	Low level output voltage, V_{OUT}	Inputs at low level OUTH_1 ≡ OUTL_1 OUTH_2 ≡ OUTL_2 I_{OUT} = 1 mA			20	mV
t_R	Output rise time	VCC = 10 V OUTH_1 ≡ OUTL_1 OUTH_2 ≡ OUTL_2 C_{OUT} to GND = 10 nF		30	60	ns
t_F	Output fall time	VCC = 10 V OUTH_1 ≡ OUTL_1 OUTH_2 ≡ OUTL_2 C_{OUT} to GND = 10 nF		30	60	ns
Propagation delay						
t_D	Input- to-output delay time	VCC = 10 V OUTH_1 ≡ OUTL_1 OUTH_2 ≡ OUTL_2 C_{OUT} to GND = 10 nF		110		ns
	Matching between propagation delays[(1)]		-5		5	ns

1. Parameter guaranteed at design level, not tested in production.

6 Radiations

6.1 Total ionizing dose (MIL-STD-883 test method 1019)

The products guaranteed in radiation within RHA QML-V system fully comply with the MIL-STD-883 test method 1019 specification. The RHFPM4424 is being RHA QML-V qualified, tested and characterized in full compliance with the MIL-STD-883 specification, both below 10 mrad/s and between 50 and 300 rad/s.

- Testing is performed in accordance with MIL-PRF-38535 and the test method 1019 of the MIL-STD-883 for total ionizing dose (TID).
- ELDRS characterization is performed in qualification only on both biased and unbiased parts, on a sample of ten units from two different wafer lots.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

6.2 TID and HI results

The behavior of the product when submitted to heavy ions is not tested in production. Heavy ion trials are performed on qualification lots only.

Table 6. Radiations

Type	Characteristics		Value	Unit
TID	2 krad/s high dose rate up to		300	krad
	85 mrad/s medium dose rate up to		100	
	ELDRS free up to		On going	
	10 mrad/s low dose rate up to		On going	
Heavy ions	SEL immunity	$V_{CC} = 18$ V	60	MeV.cm^2/mg
		$V_{CC} = 16$ V	70	
	SET (at 25 °C)	Characterized		

7 Device description and operation

7.1 Overview

The RHFPM4424 is a dual low-side driver suitable to charge and discharge big capacitive loads like MOSFETs or IGBTs used in power supplies and DC-DC modules. The RHFPM4424 can sink and source 4.5 A on each low-side driver branch but a higher driving current can be obtained by paralleling its outputs.

Even though this device has been designed to cope with loads requiring high peak current and fast switching time, the ultimate driving capability depends on the power dissipation in the device which must be kept below the power dissipation capability of the package. This aspect is met in *Section 8.2*.

The RHFPM4424 uses VCC pin to supply and two ground pins (SGND signal ground and PGND power ground) for return. SGND is used as reference ground for the input stage and it can be connected to ground of the remote controller. PGND is the reference ground for the output stage; SGND can bounce +/-5 V versus PGND so that PWM input pin common mode can range +/-5 V versus PGND.

The dual low-side driver has been designed to work with supply voltage in the range from 4.5V to 18 V.

Before VCC overcomes UVLO threshold (VUVLO), the RHFPM4424 keeps off both low-side MOSFETs (OUTL_x outputs are grounded) then, after UVLO threshold has crossed, PWM input keeps the control of the driver operations. Input pins (PWM_1 and PWM_2) are CMOS/TTL compatible with capability to work with voltages up to VCC.

7.2 Input stage

PWM inputs of the RHFPM4424 dual low-side driver are compatible to CMOS/TTL levels with capability to be pulled up to VCC.

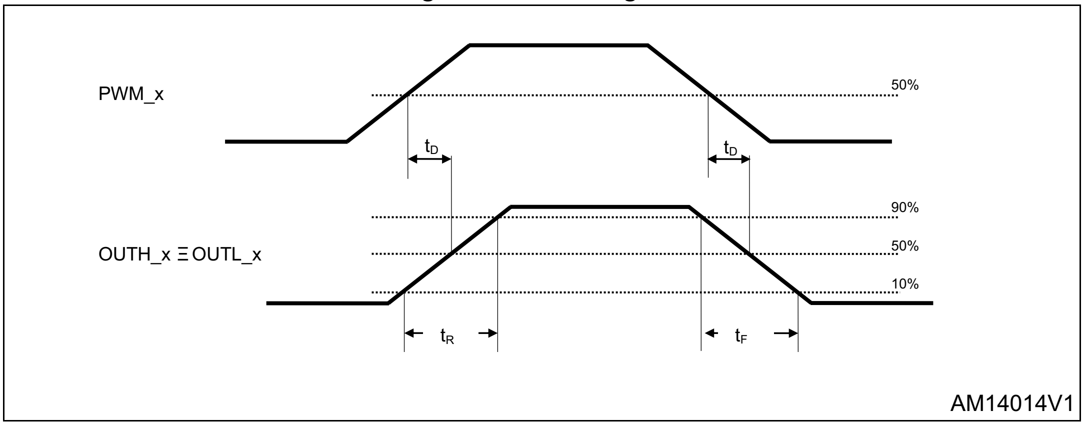
The relation between PWM_1 and PWM_2 input pins and the corresponding PWM output is depicted in *Figure 5*. In the worst case, input levels above 2.0 V are recognized as high logic values and values below 0.8 V are recognized as low logic values.

Input-to-output propagation delays (t_D) and also rise (t_R) and fall (t_F) times have been designed to assure the operation in fast switching environment.

The matching between delays in the two branches of the RHFPM4424 assures symmetry in the operations and allows the parallel output functionality.

SGND input stage ground reference can bounce versus PGND of +/-5 V.

Figure 5. Time diagram



7.3 Output stage

The RHFPM4424 output stage uses ST's proprietary lateral DMOS. Both NDMOS and PDMOS have been sized to exhibit high driving peak current as well as low on-resistance. When OUTL_x and OUTH_x are connected together, the typical peak current is 4.5 A.

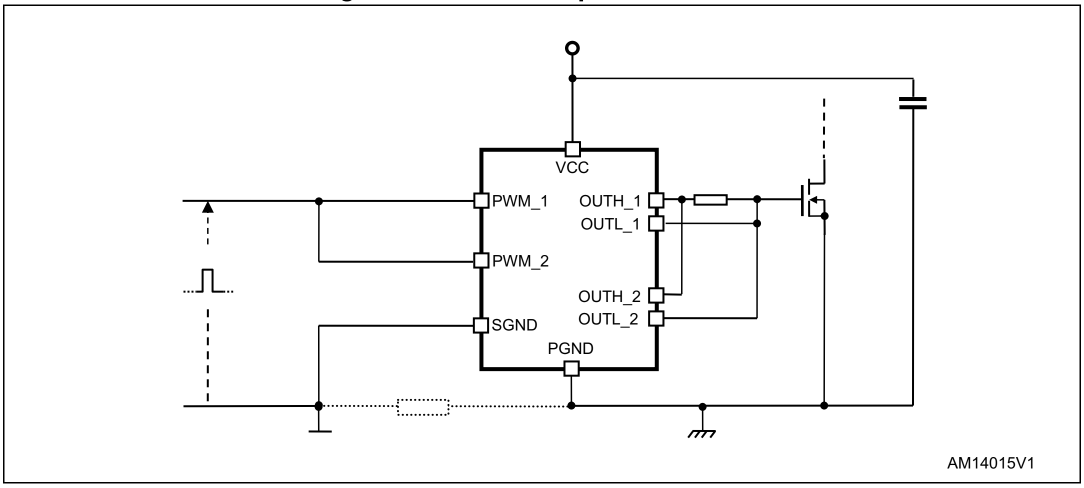
The device features the adaptive anti-cross-conduction protection. The RHFPM4424 continuously monitors the status of the internal NDMOS and PDMOS: in case of a PWM transition, before the desired DMOS switches on, the device awaits until the other DMOS completely turns off. No static current flows from VCC to ground.

7.4 Parallel output operation

For applications demanding high driving current capability (over 4.5 A provided by the single branch), the RHFPM4424 allows the two drivers to be in parallel to reach the highest current, up to 9 A.

This configuration is depicted in *Figure 6* where PWM_1 and PWM_2 and OUTH_x and OUTL_x are tied together. The matching of internal propagation delays guarantees that the two drivers switch on and off simultaneously.

Figure 6. Parallel output connection



7.5 Gate driver voltage flexibility

The RHFPM4424 allows the user to select the gate drive voltage so to optimize the efficiency of the application.

The low-side MOSFET driving voltage depends on the voltage applied to VCC and can range from 4.5 V to 18 V.

8 Design guidelines

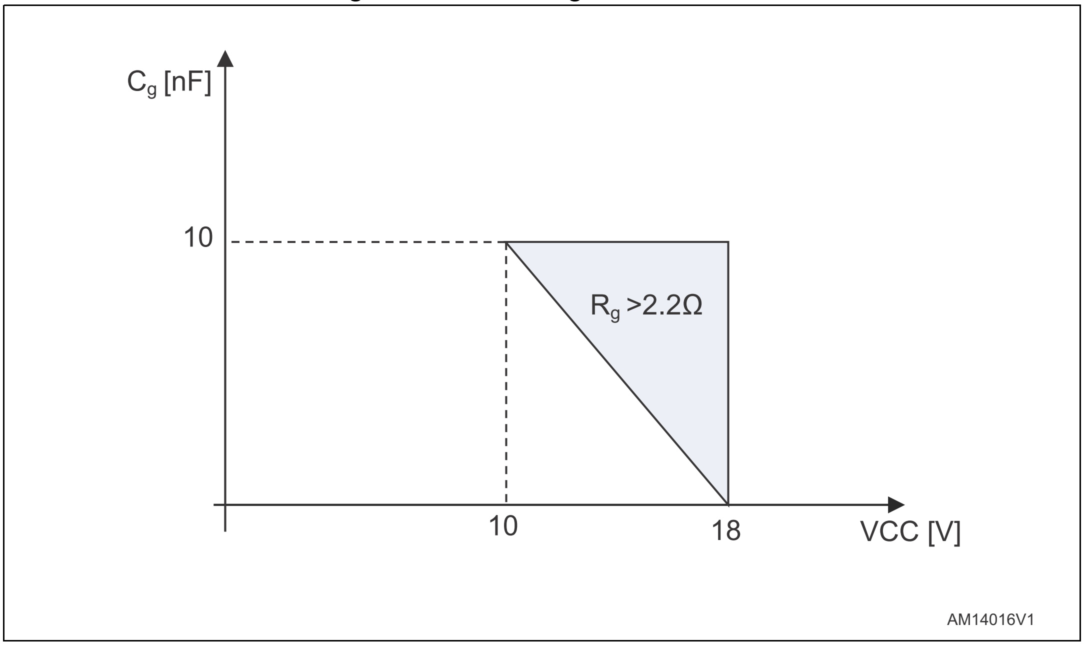
8.1 Output series resistance

The output resistance allows the high frequency operation without exceeding the maximum power dissipation of the driver package.

See *Section 8.2* to understand how the output resistance value is obtained. For applications with VCC supply voltage greater than 10 V and high capacitive loads (Cg > 10 nF), the dissipated power in the output stage of the device has to be limited, therefore at least 2.2 Ω Rg gate resistor has to be added.

Figure 7 is a synthetic view of the boundaries for the safe operation of the RHFPM4424.

Figure 7. Minimum gate resistance



8.2 Power dissipation

The RHFPM4424 embeds two high current low-side drivers which drive high capacitive MOSFETs. This section estimates the power dissipated inside the device in normal applications. Two main terms contribute to the device power dissipation: bias power and driver power.

- PDC bias power depends on the static consumption of the device through the supply pins and it is given by below equation:

Equation 1

$$P_{DC} = V_{CC} * I_{CC}$$

- The driver power is the necessary power to continuously switch on and off the external MOSFETs; it is a function both of the switching frequency and total gate charge of the selected MOSFETs. P_{SW} total dissipated power is given by three main factors:
  - external gate resistance (when present)
  - intrinsic MOSFET resistance
  - intrinsic driver resistance

It is indicated in the below equation:

Equation 2

$P_{SW} = F_{SW} * (Q_G * V_{CC})$

When an application is designed using the RHFPM4424, the effect of external gate resistors on the power dissipated by the driver has to be taken into account.

External gate resistors help the device to dissipate the switching power since the same power, P_{SW}, is shared between the internal driver impedance and the external resistor.

In *Figure 7*, the MOSFET driver can be represented by a push-pull output stage with two different MOSFETs:

- PDMOS to drive the external gate to high level
- NDMOS to drive the external gate to low level (with $R_{DS(on)}$: R_{hi}, R_{lo}).

The external MOSFET can be represented as C_{gate} capacitance, which stores QG gate charge required by the external MOSFET to reach VCC driving voltage. This capacitance is charged and discharged at F_{SW} frequency.

P_{SW} total power is dissipated among the resistive components distributed along the driving path. According to the external gate resistance and the intrinsic MOSFET gate resistance, the driver only dissipates a P_{SW} portion as follows (per driver):

Equation 3

$$P_{SW} = \frac{1}{2} \cdot C_{gate} \cdot (V_{CC})^2 \cdot F_{SW} \cdot \left(\frac{R_{hi}}{R_{hi} + R_g + R_{load}} + \frac{R_{lo}}{R_{lo} + R_g + R_{load}}\right)$$

The total dissipated power from the driver is given by $P_{TOT} = P_{DC} + 2*P_{SW}$.

Figure 8. Driver and load equivalent circuits

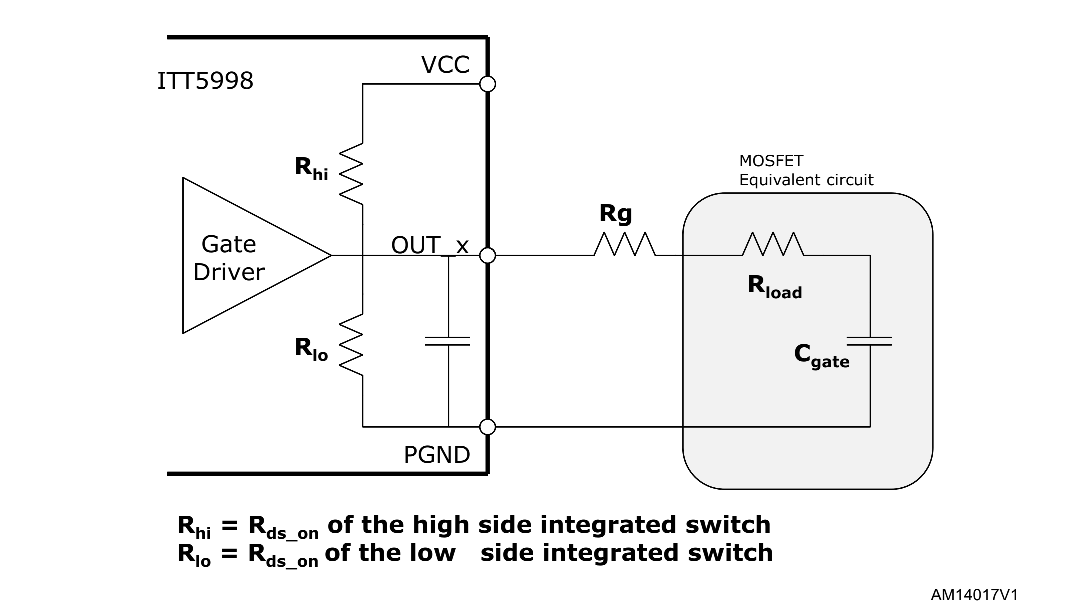


Figure 9. Power dissipation with Rg = 2.2 Ω

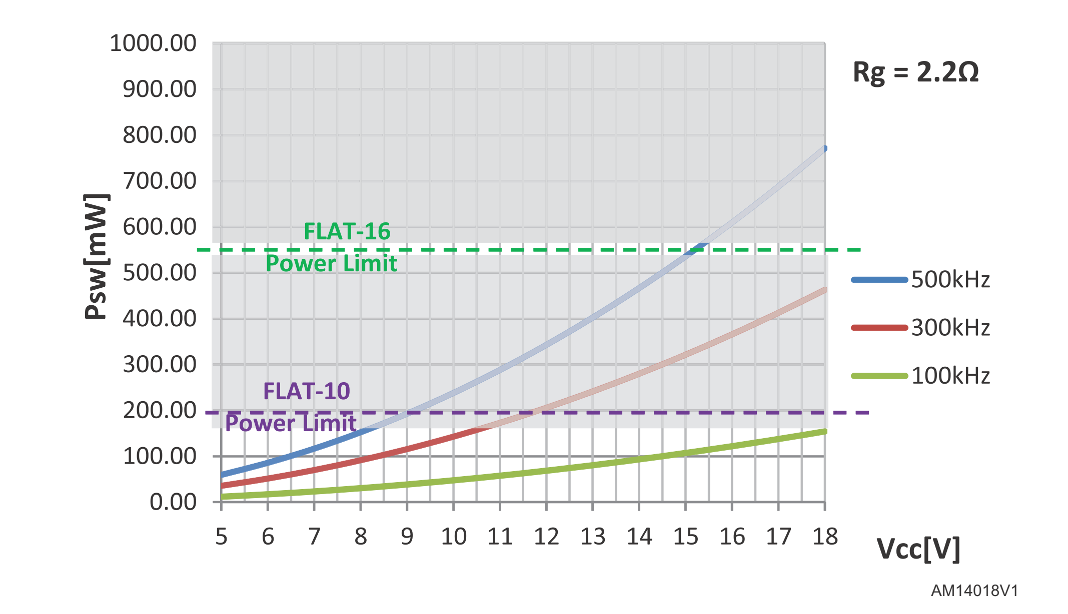
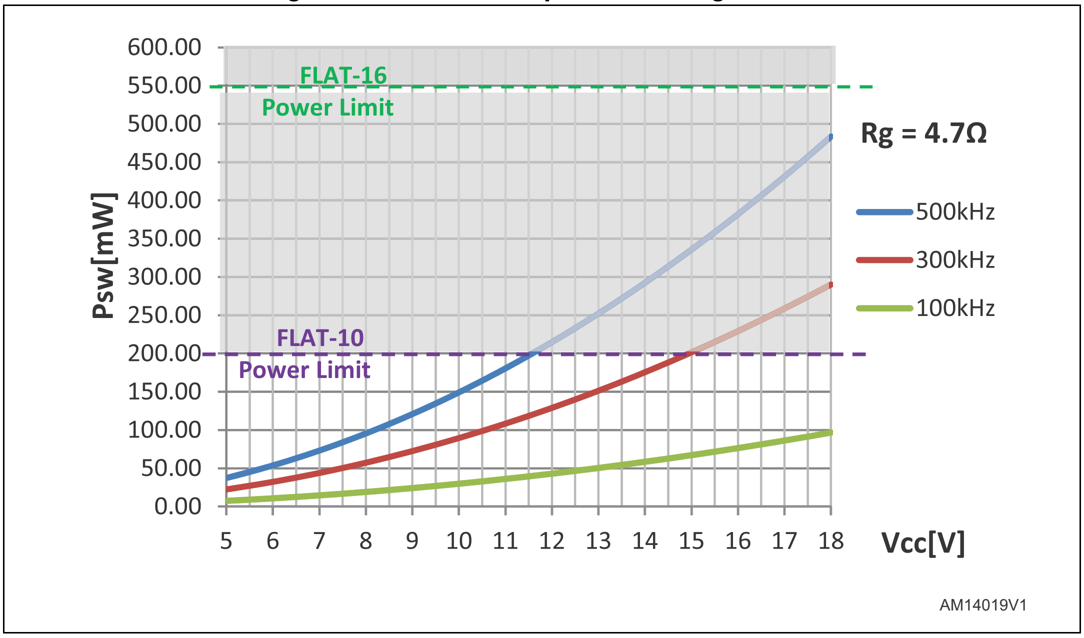
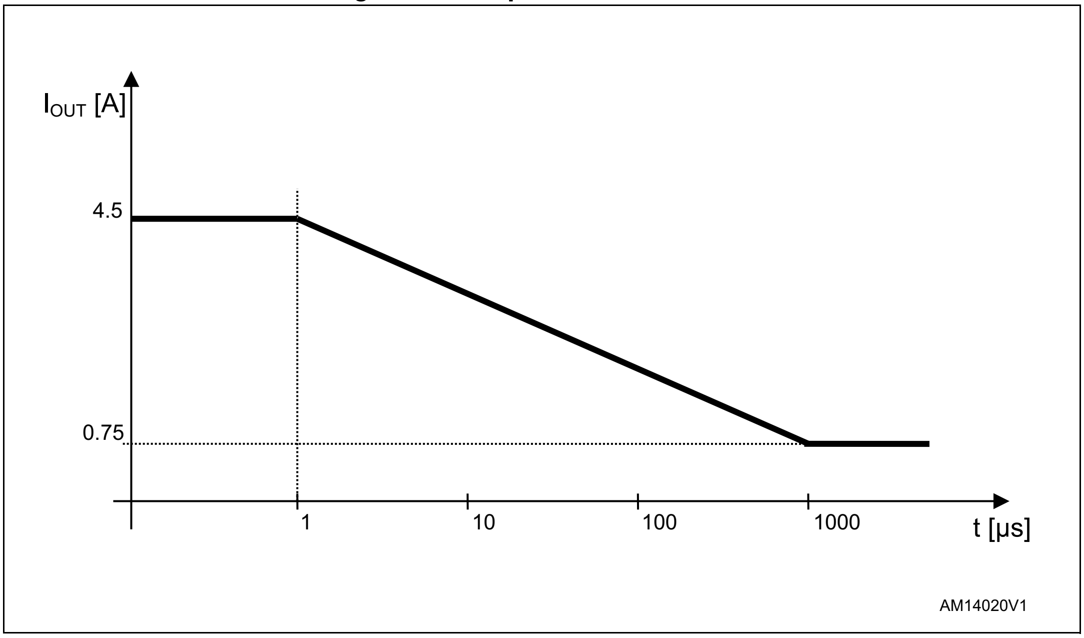


Figure 10. Power dissipation with Rg = 4.7 Ω



With regard to the power dissipation and current capability purpose, a profile, for the curve output current versus time, is recommended. See the one depicted in *Figure 11*:

Figure 11. Output current vs. time



9 Layout and application guidelines

The first priority, when components are placed for these applications, is the power section, minimizing the length of each connection and loop. To minimize noise and voltage spikes (EMI and losses as well) power connections have to be a part of a power plane with wide and thick conductor traces: loop has to be minimized. The capacitor on VCC, as well as the output inductor should be placed as closer as possible to IC. Traces between the driver and the external MOSFETs should be short to reduce the inductance of the trace and the ringing in the driving signals. Moreover, the number of vias has to be minimized to reduce the related parasitic effect.

Small signal components and connections to critical nodes of the application as well as bypass capacitors for the device supply are also important. The bypass capacitor (VCC capacitors) has to be placed close to the device with the shortest loop to minimize the parasitic inductance.

To improve heat dissipation, the copper area has to be placed under the IC. This copper area may be connected to other layers (if available) through vias so to improve the thermal conductivity: the combination of copper pad, copper plane and vias under the driver allows the device to reach its best thermal performance. It is important for the power device to have a thermal path compatible with the dissipated power: both the driver and the external MOSFET have to be mounted on a dedicated heat sink (for example, the driver should be soldered on the copper area of the PCB, which is in strict thermal contact to an aluminum frame) sticking each part to the frame (without using any screw for the MOSFET). The glue could be the resin ME7158 (space approved resin). Moreover, two small FR4 spacers could be added to guarantee the electrical isolation of the package from the frame.

A recommended PCB layout is shown in *Figure 12*.

Figure 12. Evaluation board layout: top view

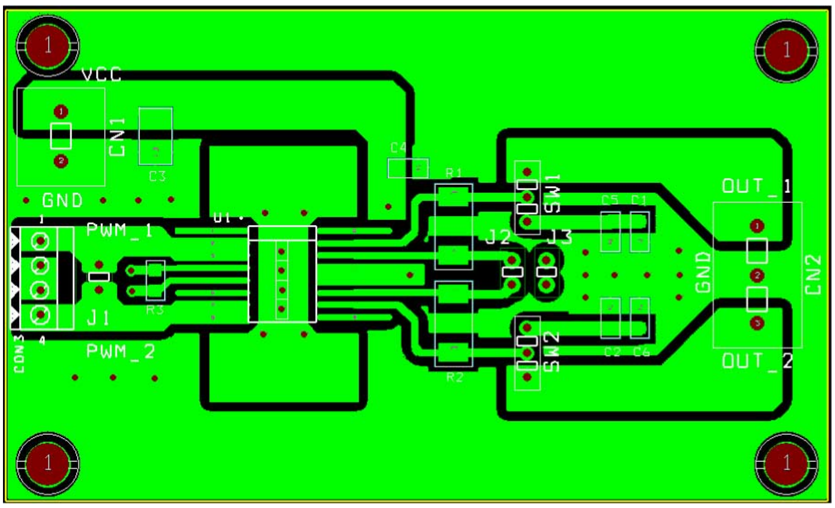


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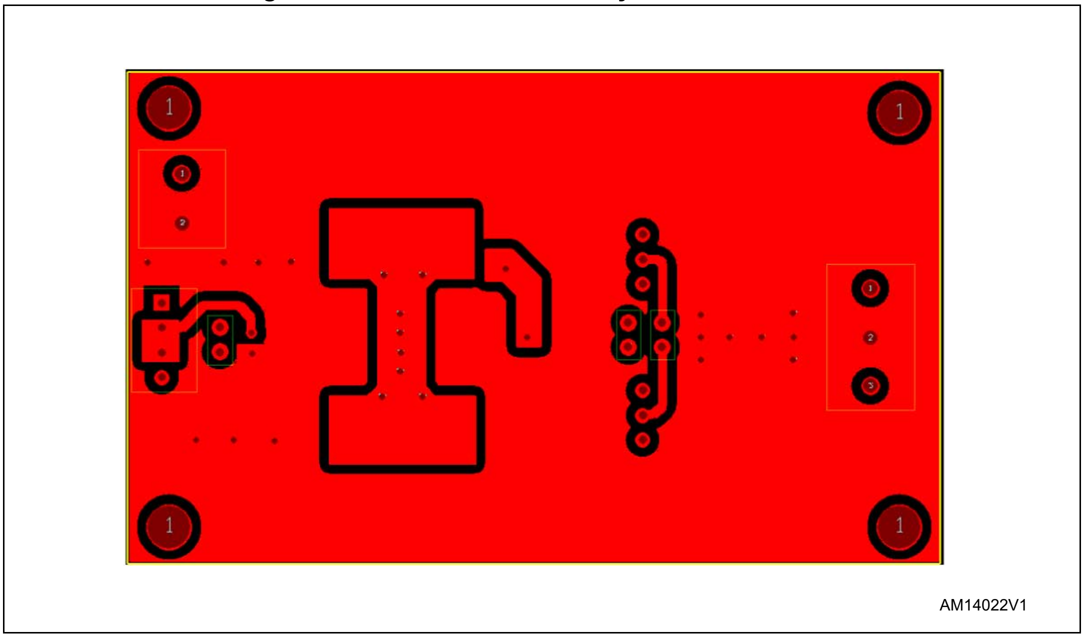
Figure 13. Evaluation board layout: bottom view



10 Typical characteristics

Figure 14. PWM_x rise time vs. supply voltage

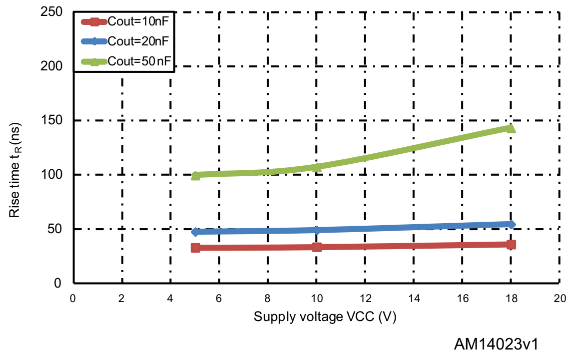


Figure 15. PWM_x rise time vs. temperature

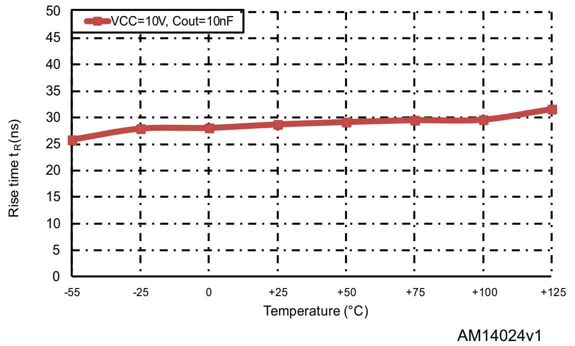


Figure 16. PWM_x fall time vs. supply voltage

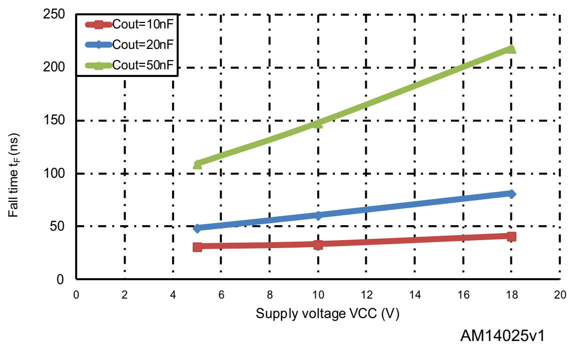


Figure 17. PWM_x fall time vs. temperature

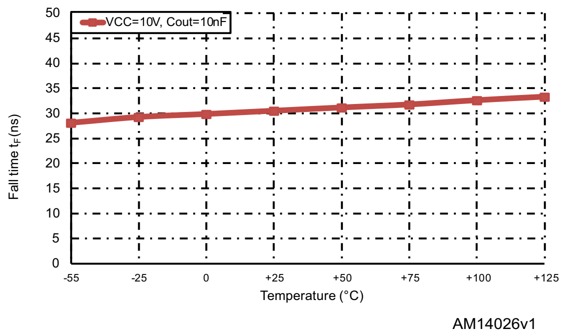


Figure 18. Input-to-output delay time vs. supply voltage

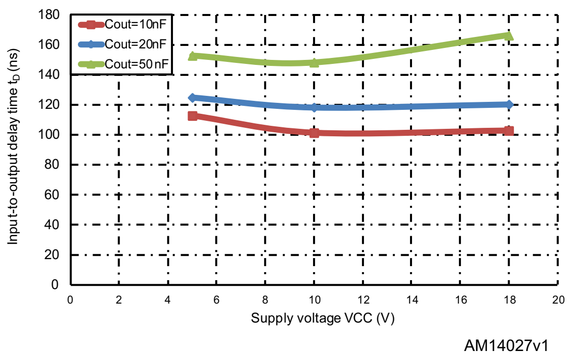


Figure 19. Input-to-output delay time vs. temperature

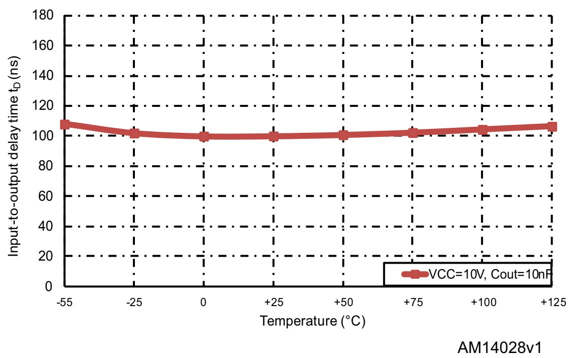


Figure 20. Source resistance vs. temperature

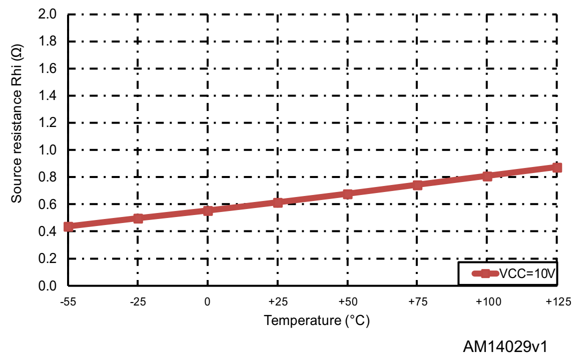


Figure 21. Sink resistance vs. temperature

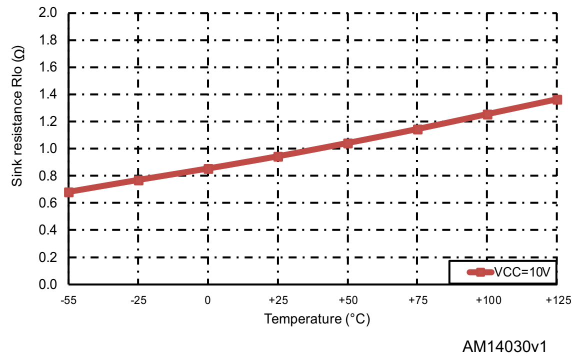


Figure 22. Output resistance vs. current

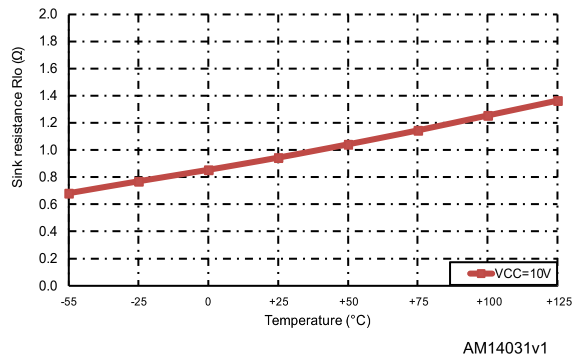


Figure 23. Operating supply current vs. supply voltage (operating frequency = 100 kHz)

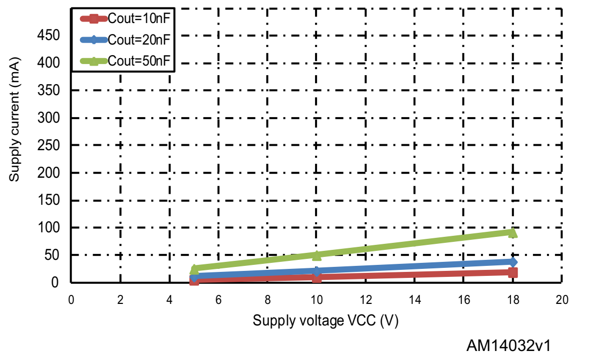


Figure 24. Operating supply current vs. supply voltage (operating frequency = 300 kHz)

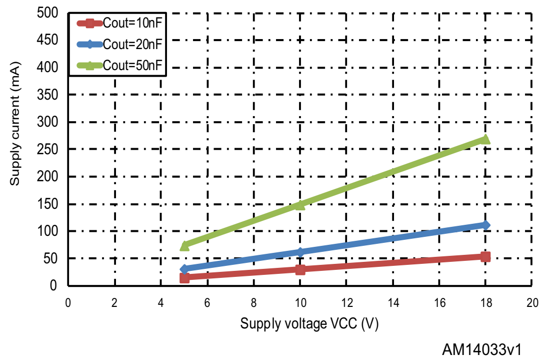


Figure 25. Operating supply current vs. supply voltage (operating frequency = 500 kHz)

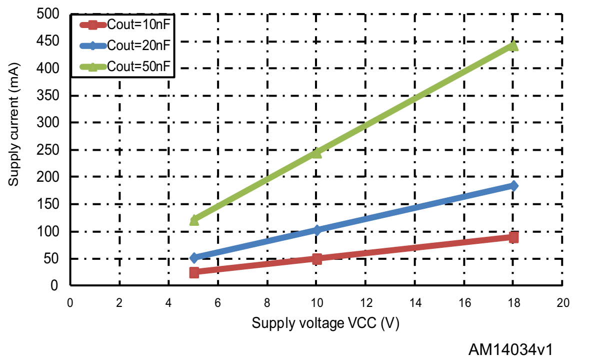
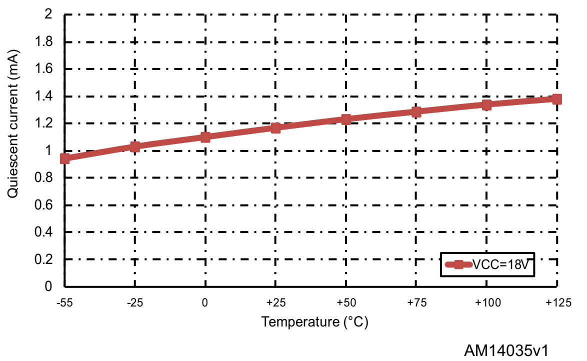


Figure 26. Quiescent current vs. temperature



11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

11.1 FLAT-10 mechanical data

Figure 27. FLAT-10 drawing

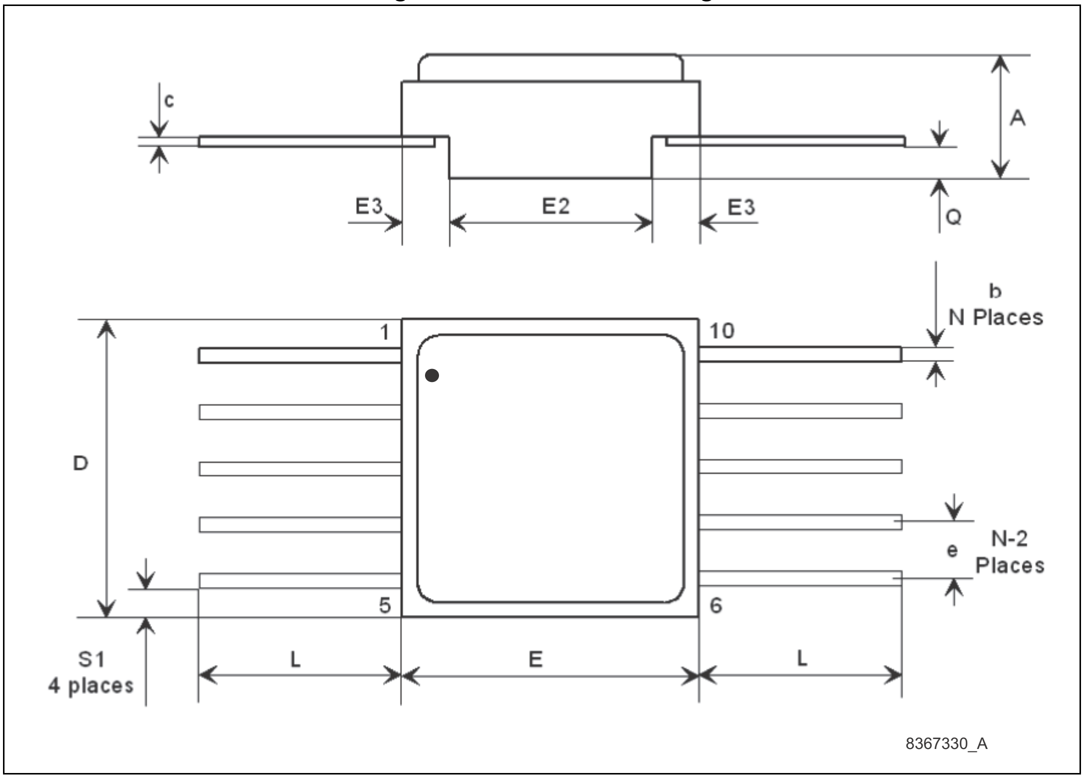


Table 7. FLAT-10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.26	2.44	2.62
b	0.38	0.43	0.48
c	0.102	0.127	0.152
D	6.35	6.48	6.60
E	6.35	6.48	6.60
E2	4.32	4.45	4.58
E3	0.88	1.01	1.14
e		1.27	
L	6.35		9.40
Q	0.66	0.79	0.92
S1	0.16	0.485	0.81
N			

11.2 FLAT-16 mechanical data

Figure 28. FLAT-16 drawing

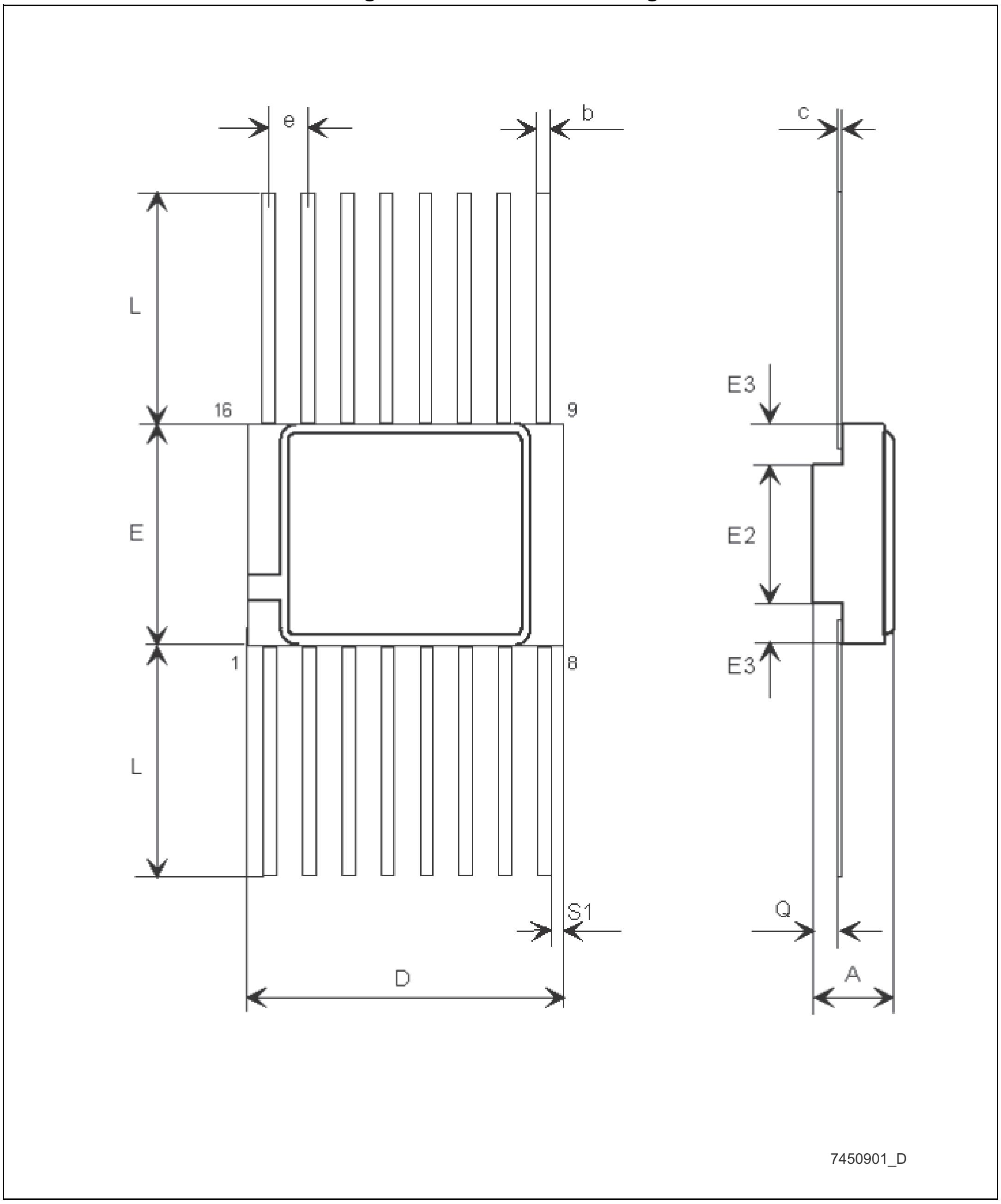


Table 8. FLAT-16 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.42		2.88
b	0.38		0.48
c	0.10		0.18
D	9.71		10.11
E	6.71		7.11
E2	3.30	3.45	3.60
E3	0.76		
e		1.27	
L	6.35		7.36
Q	0.66		1.14
S1	0.13		

12 Ordering information

Table 9. Order codes

Order code	Quality level	Temperature range	Package	Lead finish	Marking	Packing
RHFPM4424LK1[(1)]	Engineering model	-55 to 125 °C	FLAT-10	Gold	RHFPM4424LK1	Strip pack
RHFPM4424K1	Engineering model		FLAT-16	Gold	RHFPM4424K1	Strip pack

1. Under development.

13 Other information

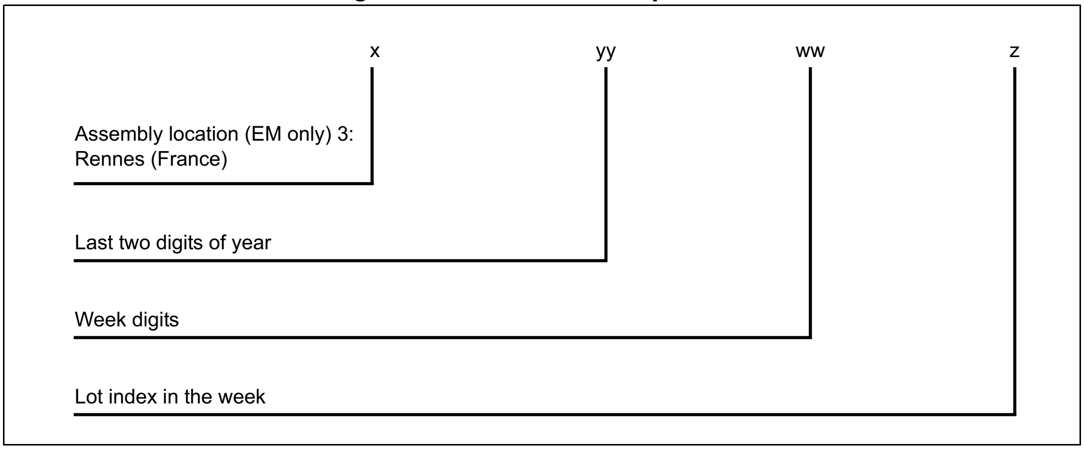
13.1 Date code

The date code is structured as shown below:

- EM xyywwz
- QML-V yywwz

where:

Figure 29. Date code composition



13.2 Documentation

Table 10. Documentation provided

Quality level	Documentation
Engineering model	-
QML-V flight	Certificate of conformance with group C (reliability test) and group D (package qualification) reference – Precap report – PIND[(1)] test summary (test method conformance certificate) – SEM[(2)] report – X-ray report – Screening summary – Failed component list, (list of components that have failed during screening) – Group A summary (QCI[(3)] electrical test) – Group B summary (QCI[(3)] mechanical test) – Group E (QCI[(3)] wafer lot radiation test)

1. QCI = quality conformance inspection.
2. PIND = particle impact noise detection.
3. SEM = scanning electron microscope.

14 Revision history

Table 11. Document revision history

Date	Revision	Changes
20-Jun-2014	1	Initial release.
02-Dec-2014	2	Document status promoted from preliminary data to production data. Updated *Table 6: Radiations*. Minor text changes.