Design note
STCC5011 / STCC5021 / STCC2540 PCB layout recommendation

Main components

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<tr>
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<th>Description</th>
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<tr>
<td>STCC5011,</td>
<td>USB charging controller with integrated power</td>
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<tr>
<td>STCC5021</td>
<td>switch and attach detector</td>
</tr>
<tr>
<td>STCC2540</td>
<td>USB charging controller with integrated power</td>
</tr>
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<td></td>
<td>switch</td>
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Specification
This design note helps to design properly the PCB layout for STCC5011 / STCC5021 / STCC2540 (STCCxxxx in later text) to ensure its high performance, trouble-free operation.

Thermal consideration
The STCCxxxx is a power device generating excessive heat. This heat must be properly conducted from the device thermal pad to inner PCB groundplane using a matrix of vias. The Rds(on) rises with temperature, so proper heat spreading increases not only the safety level but also the system performance.

For recommendation see JEDEC JESD 51-5 and 51-7.

PCB tracks

Power path
In many operation modes, high current flows through the IN and OUT terminals. So the PCB tracks to IN and OUT pads must be rated to a current up to 3 A without generating excessive heat. Also the resistance of these tracks should be as low as possible to benefit from STCCxxxx low Rds(on).

Taking in account the excessive heat only, minimum track width (for ΔT = 10°C) may be 2 mm for 18 µm Cu foil, 1 mm for 35 µm and 0,5 mm for 70 µm. Each centimeter of above defined track adds approximately 5 mΩ to total resistance so using as wide tracks as possible is highly recommended.

The impact of IN track resistance could be eliminated by connecting the power supply feedback loop as close to IN pin as possible. For minimizing the OUT track resistance the best solution is to place the STCCxxxx close to the corresponding USB port.
USB 2.0 High-speed data line

The USB 2.0 high-speed differential line between USB transceiver and STCCxxxx DP_OUT, DM_OUT and between STCC50x1 DP_IN, DM_IN and USB connector D+, D- pins should be as straight and short as possible. It is not recommended to use vias on this line. The track width and spacing must be designed so that differential impedance must be 90 Ω ± 10% and single-ended impedance 45 Ω ± 10%.

ILIM connection

To reach maximum precision of STCCxxxx current limiter, the connection to current limiter programming resistor $R_{\text{ILIM}}$ should be as short as possible. The current flowing through the $R_{\text{ILIM}}$ is very small, so any coupling from other tracks can influence it. It is recommended to avoid high current or high speed lines to be placed close to the ILIM connection and resistor. The capacitance of connection to ILIM track should be as low as possible to avoid compromising the current limiter feedback loop stability.

Other tracks

No special requirements are set for other STCCxxxx connections.

Decoupling components

Input decoupling capacitors

For proper functionality of STCCxxxx device, the supply decoupling capacitors C1 (STCC50x1 only), C2 on Vdd and IN terminals are necessary (see Figure 1).

The input decoupling capacitors should be located as close to the STCCxxxx device as possible, connected with short, low-impedance tracks to Vdd, IN and GND.

Output capacitors

The capacitors connected to STCCxxxx OUT terminal, C3 and C4 (see Figure 1), are not necessary for stable STCCxxxx operation but are recommended to improve the ESD performance and to cover inrush current transients generated on attach and detach of peripheral devices, as requested by the USB specification.

The output capacitors (especially C4) should be located as close as possible to USB connector, connected with short, low-impedance tracks to OUT and GND.

Recommended types and values

It is highly recommended to use low-impedance ceramic capacitors for decoupling (C1 to C3). The capacitance should be 0.1 µF or more. Recommended value is 1 µF. Higher value improves supply decoupling, transients suppression and ESD performance.

The output capacitor C4 should be low-ESR electrolytic type with capacitance in range of 100 µF to 330 µF. Recommended value is 150 µF. Too low capacitance leads to higher voltage droop caused by peripheral device inrush current, too high capacitance may cause malfunction of the attach detector.
Figure 1. Circuit diagram example

Figure 2. PCB layout example

Note: Drawing not to scale. Provided for illustration of component placement only.
## Revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
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<tbody>
<tr>
<td>06-Jun-2013</td>
<td>1</td>
<td>Initial release</td>
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