DT0009
Design tip

Speed up development of the L6699 with the L6599A and flexible PCB layout

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Main components	
L6699	Enhanced high voltage resonant controller
L6599A	Improved high voltage resonant controller

Purpose and benefits

Using the L6699 LLC control IC, power designers can now realize the benefits of higher efficiency and increased reliability due to enhanced protection features incorporated into the device. Because the L6699 needs a constant resonant tank current monitoring signal to operate, it can sometimes be difficult to get the device operating during the initial design stages. This design tip outlines a method to use a previous version of the IC, the L6599A with slight modifications in the PCB layout to speed up development with the new IC.

Description

The L6699, as part of its unique feature set, has the ability to detect if it is operating in destructive capacitive mode by monitoring the resonant tank current to make sure it is lagging the voltage assuring safe and reliable operation. The current signal must be present at the onset of device startup. If it is not of the proper phase and amplitude or has unforeseen noise on it, the IC will shut the converter down to protect the system. When evaluating converter designs with new circuit board layouts and magnetics, it is possible that the current signal will have one or more of the aforementioned problems and frustrate the designer because the converter shuts down constantly. Fortunately, the older L6599A is pin-for-pin compatible with the L6699 and does not need to monitor the phase of the current to operate. Thus it can be used to bring the converter up on a preliminary basis and then the design can be changed over to the L6699 to realize the capacitive mode protection feature. The following provides the details of the differences between the ICs and a procedure to transition from the L6599A over to the L6699.

The main difference between the two ICs lies in the structure of the current sensing section. The typical configuration for the L6599A current sense section using the capacitive divider technique is shown in figure 1. The AC signal coupled through capacitor CA is rectified by the two 1N4148 diodes and filtered. This produces a DC level proportional to the primary tank current on Isense pin (Pin 6). It should be noted from the L6599A data sheet that the Isense pin negative voltage limit is -0.3 volts indicating that the sensing is single ended.

Figure 1. L6599A current sense

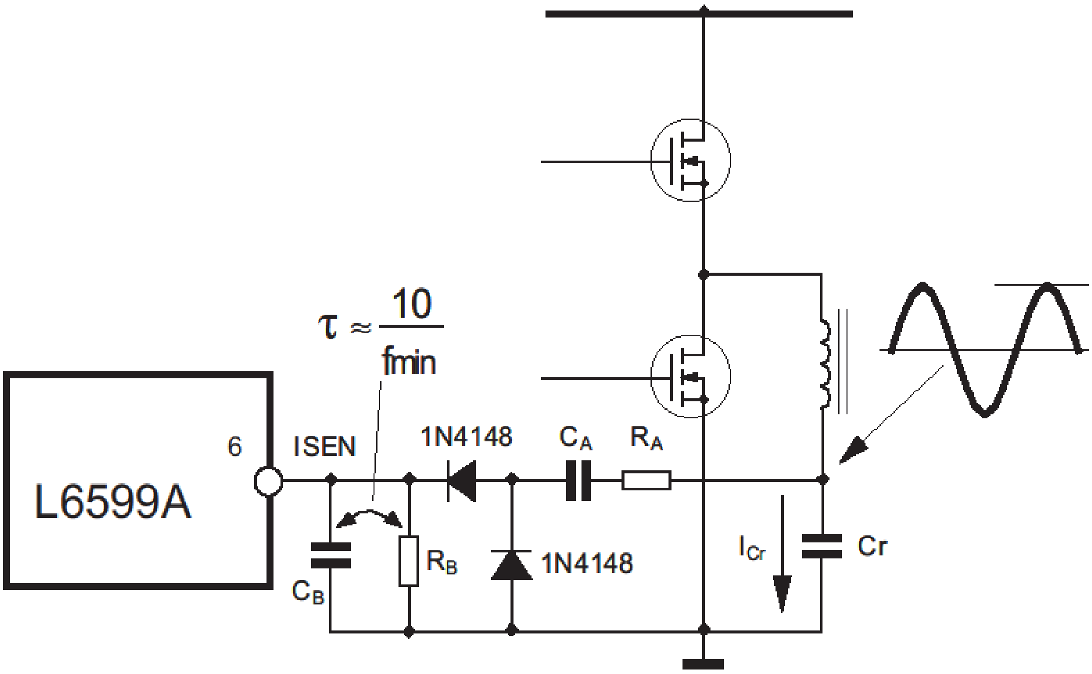
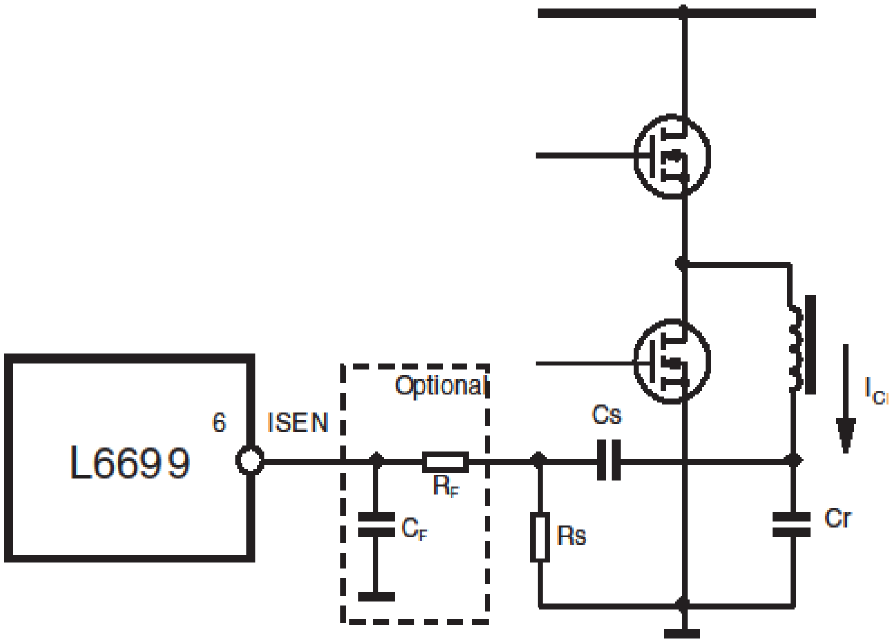


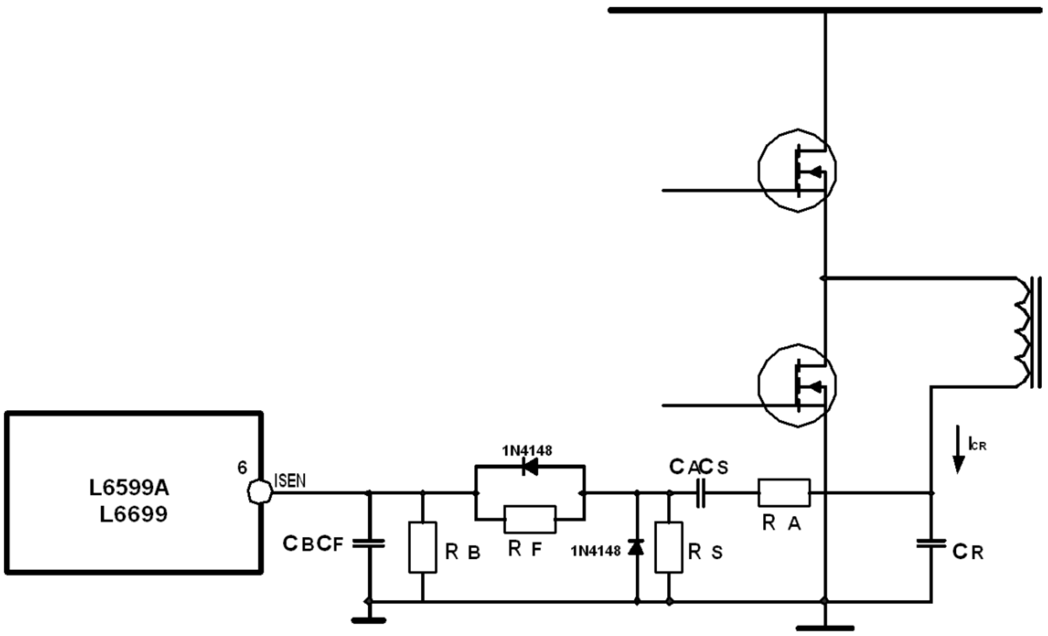
Figure 2. L6699 Current Sense



Similar to the L6599A current sensing scheme shown in figure 1, the L6699 current sensing configuration is shown in figure 2. In this scheme, the same capacitive divider technique is used but there is no rectification. The negative portion of the AC signal is allowed to be sensed by the Isense pin (Pin 6). Accordingly, the absolute maximum ratings section of the L6699 data sheet shows a rating of plus 5 to negative 3 volts indicating a plus and minus input. This is the necessary mechanism to facilitate sensing the tank current phase shift in relation to the half bridge voltage to detect capacitive mode operation.

On a new PCB layout it is possible to have a configuration that allows either of the ICs to be used, as shown in figure 3.

Figure 3. Combination Current Sense



Using this arrangement, the L6599A and its associated components for the current sense circuit shown in figure 1 would be inserted first. Once the converter is operating satisfactorily with the L6599A, the L6699 can be swapped into the circuit board along with the supporting components as shown in figure 2.

When testing a new LLC converter for the first time with the L6599A, the following general procedure is suggested. First, it is recommended that two kinds of lab type power supplies be employed. One should be a low voltage low power type used to supply the L6599A and associated components. An adjustable high voltage supply would be used to supply the power section and should have a fully variable voltage control up to the maximum that the converter is designed for.

The first time the converter is brought up, the gate drives should be running from the low voltage supply. The supply for the power section is set at zero voltage at the onset and is increased slowly so that the converter operation can be monitored and if any malfunction is detected, the supply for the power section can be reduced so that potential damage to the circuit can be avoided. Normally, however, the gate drives will not run under the aforementioned conditions because the LINE input Pin 7 is not at its threshold to enable the drives. To remedy this condition, the pin should be connected to an alternate resistive voltage divider supplied from the low voltage supply. Typically, the divider is configured so that as the supply is turned up to the maximum turn on threshold of the L6599A, the divider reaches the turn on threshold of the LINE pin (nominally 1.22VDC) and the gate drives are enabled. Under this method of operation, the converter will be running at the minimum frequency programmed by the values of Cf capacitor and the Rfmin resistor connected to pins 3 and 4 respectively. The designer should check that this minimum running frequency is above the lower resonant frequency given by the sum of the magnetizing and leakage inductances along with the value of the resonant capacitance. If the running frequency is below the resonant frequency, capacitive mode hard switching will result with the potential for damage to the circuitry.

With the drives enabled, it is also recommended that a modest resistive load be connected. The power section supply can then be increased incrementally and the circuit monitored for proper operation. If possible, the primary transformer current should be monitored with an oscilloscope and current probe combination. Additionally with the LLC topology being a very efficient converter, it is useful to have instrumentation to monitor the input and output power. As the voltage and power levels are increased, any unreasonable power loss or sudden decrease in efficiency should be investigated.

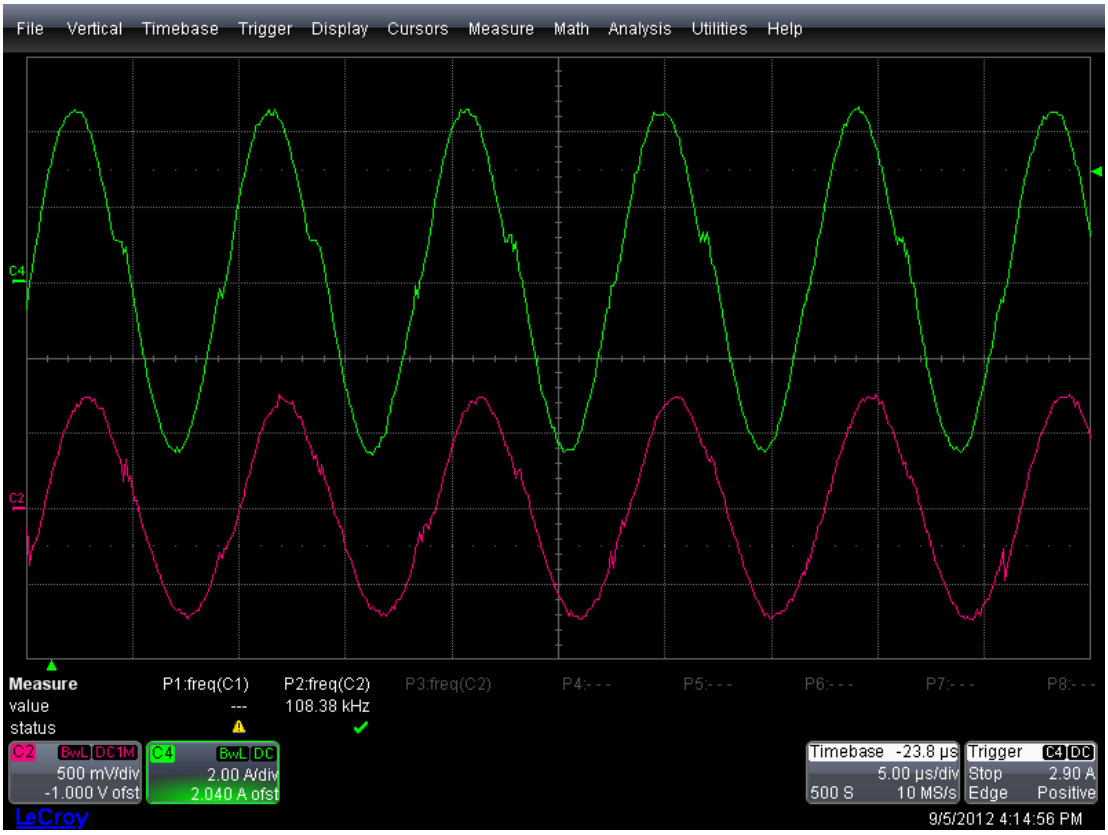
The convertor should be able to run up the maximum specified voltage it was designed for with a small load. The load should be increased incrementally until the full load is achieved. If there is a problem, it will often manifest as a sudden latched shutdown. If this is experienced, the following aspects of the design should be reviewed as follows:

- PCB layout - make sure the power section and control section are adequately separated with individual grounds joined at a star point.
- The proximity and orientation of the half bridge node to the control circuitry – Confirm the dv/dt present on it is easily coupled into the high impedance nodes of the control circuitry.
- Common mode noise – the Y capacitors and appropriate shielding can be employed to deal with this type of issue.

Assuming the L6599A driven convertor has been successfully brought up using the two power supply method, it should then be tested in the intended application. Usually the converter is supplied from a PFC stage. If this is the case, the converter should be loaded at various levels and started from the PFC stage. Aspects of the design that should be examined include the startup and shut down points controlled by the LINE pin. The current limit should be also investigated to see if the overload level is properly adjusted along with the delay pin settings. If these items are satisfactory along with the line and load regulation performance, the design is ready to be migrated over to the L6699.

As mentioned previously, when the L6599A is swapped out for the L6699, the supporting component arrangement, shown in figure 1, needs to be exchanged for the arrangement shown in figure 2. In figure 2, the filter components Rf and Cf are shown as optional. It is recommended that these components always be included. As a starting point for the values of these components, the time constant of 100nS is recommended. Example values would be 1K ohm and 100pF. If the converter does not start successfully or if the gate pulse train has gaps due to capacitive mode detection, the time constant should be increased. Again, it is very useful to have a current probe monitoring the primary current. At the same time, probing the signal at the current sense pin will provide insight on how accurately the current is being monitored by the IC. An example of this is shown in the scope capture of figure 4.

Figure 4. Primary Current and Pin 6 Isense Sense waveforms



In figure 4, the upper green trace is the primary current as measured with a current probe at 2 amps per division. The lower trace is the sensed current present on the Isense pin 6 at 500 millivolts per division. In this capture, the converter is being operated at full load and it is worth noting that the peak amplitude of the Isense signal is just under the 800 millivolt threshold of the Isense where the IC will shift the frequency up to limit the power. This amplitude is typically adjusted with the Rs resistor. Also of note is the lagging phase shift of the sensed signal to the primary current due to Rf, Cf filter. In this instance, a 440 nanosecond time constant (comprised of a 2k ohm resistor and 220pF capacitor) was employed. The design should use the lowest time constant possible to get the converter to work reliably. As the time constant gets longer, the ability to detect capacitive mode operation becomes more compromised.

Using the techniques presented, the designer can have a faster track to getting the enhanced capabilities of the L6699 into their LLC converter. In addition to the capacitive switching mode detection, these include, adaptive dead-time, and enhanced soft start. Additionally, the L6699 has better tolerances on the various thresholds of the IC that enable the designer to have more efficient and reliable LLC designs.

Support material

Documentation
Datasheets L6599A Enhanced high voltage resonant controller, L6699 Improved high voltage resonant controller

Revision history

Date	Version	Changes
30-Apr-2013	1	Initial release