The BlueNRG-2 device limitations

Silicon identification

This errata sheet applies to the following STMicroelectronics BlueNRG-2 devices:

Table 1. Device identification

Oder code	Package	Identification information of the device(1)
BlueNRG-232	QFN32 (5x5 mm)	0x00000100
BlueNRG-234	WLCSP34	0x00000112
BlueNRG-248	QFN48 (6x6 mm)	0x00000112

1. *Value as read from register CKGEN_SOC - DIE_ID register (0x4090001C)*

1 Limitations

1.1 Reduced operating voltage range when brown-out reset (BOR) is enabled

Part number affected: the BlueNRG-232.

Description: when brown-out reset (BOR) is enabled the operating voltage of the device is reduced to 2.1-3.6 V.

Impact: brown-out reset (BOR) threshold prevents the device from being safely used below 2.1 V.

Workaround: the application using brown-out reset (BOR) must restrict operating range to 2.1 V.

1.2 Brown-out reset (BOR) is not enabled by default

Part numbers affected: the BlueNRG-232.

Description: the device brown-out reset (BOR) is not enabled by default.

Impact: brown-out reset (BOR) activation requires a software action.

Workaround: brown-out reset (BOR) can be enabled by the software by setting the BOR_CONFIG=BOR_ON preprocessor option in STSW-BLUENRG1-DK (BlueNRG-1, BlueNRG-2 DK SW package).

1.3 Bit pattern could cause SWD interface not to work

Part numbers affected: the BlueNRG-232.

Description: During debug connection via serial wire debugger (SWD) port, if a specific bit pattern is sent/ received to/from the SWDIO pin, the chip could not answer anymore subsequent SWD requests, thus breaking the connection. The bit pattern represented as 32 bit word is 0x39E6xxxx.

Impact: using serial wire debugger (SWD) during development and/or production to program the Flash memory can cause some issues if the Flash memory image contains a particular pattern.

Workaround: none.

1.4 Extended packet length limitation

Part numbers affected: the BlueNRG-232.

Description: the extended packet length for test mode packets does not work. User mode packets are not impacted.

Impact: the certification can be only performed with the extended data length capability disabled.

Workaround: none.

1.5 Aux ADC end of calibration interrupt flag cannot be cleared

Part numbers affected: the BlueNRG-232.

Description: the ADC end of calibration interrupt flag cannot be cleared, so it cannot be used. STATUS register includes end of calibration information in bit 2.

Impact: no specific issue, since the interrupt of end of calibration does not have a practical use in the real application scenario.

Workaround: since the end of calibration bit cannot be used, keep the interrupt mask bit associated disabled. There is no interest in such bit.

1.6 ADC WDOG status flag / interrupt cannot be cleared

Part numbers affected: the BlueNRG-232.

Description: Aux ADC WDOG status flag / interrupt cannot be cleared in a simple manner and makes the meaning almost not usable.

Impact: Aux ADC WDOG IRQ is not usable.

Workaround: none.

1.7 ADC does not work properly when a 32 MHz system clock is being used

Part numbers affected: the BlueNRG-232, BlueNRG-234 and the BlueNRG-248.

Description: ADC IP does not run correctly with a system clock at 32 MHz.

Impact: ADC cannot be used reliably at 32 MHz system clock.

Workaround: the application, using a 32 MHz quartz and accessing ADC, should configure system clock to 16 MHz.

1.8 ADC SNR degradation

Part numbers affected: the BlueNRG-232.

Description: ADC SNR may be randomly degraded depending on ADC clock generator start-up. Given the clock ratio, the occurrence of the degradation is statistically of ¼ on average.

Impact: SNR degradation is in the range of 6 dB, therefore the effective number of bit of the ADC is reduced by 1 bit.

Workaround: in case of static signal, multiple acquisitions and averaging allow ADC accuracy to be recovered.

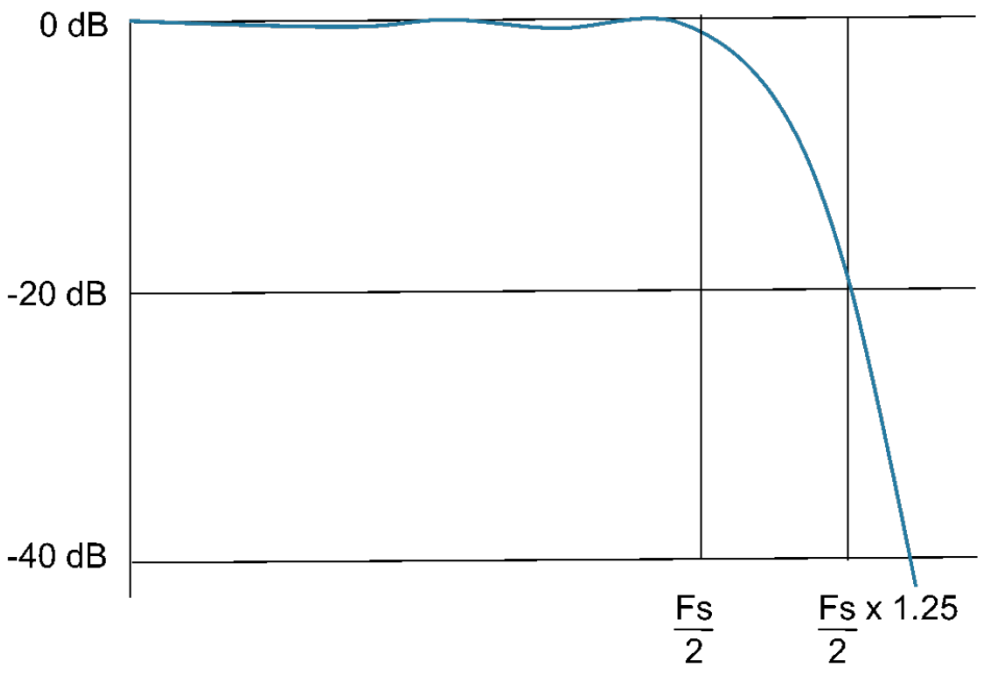
1.9 ADC unwanted aliased signal after decimation filter

Part numbers affected: the BlueNRG-232, BlueNRG-234 and the BlueNRG-248.

Description: the bandwidth of the anti-aliasing filter is slightly broader with respect to the signal bandwidth, potentially thus generating unwanted aliased signal after the decimation filter.

Impact: When a pure sine wave, generated in the [Fs/2; 1.25*Fs/2] range, is being sampled, user can notice an attenuated aliased sine wave in the [0.75*Fs/2; Fs/2] range.

Figure 1. Interpolation filter frequency response



In case of waveform acquisition, especially when audio speech and music is caught, no further degradation has been identified.

F_S is the sampling frequency on the output of the downsampling filter, described as ADC data rate in the datasheet.

Workaround: by choosing an appropriate oversampling factor (OSR), so that maximum frequency of the sampled signal is lower than Fs/2, aliasing may be avoided.

1.10 Incorrect system ROM table detected by debug connection

Part numbers affected: the BlueNRG-232.

Description: system ROM table address is incorrect and prevents a proper recognition as an ST device when connecting to a debugger.

Impact: the debug connection may work incorrectly and the part is not recognized as an ST device.

Workaround: none.

Revision history

Table 2. **Document revision history**

Date	Version	Changes
28-Jun-2018	1	Initial release.

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