Introduction

This reference manual provides complete information for application developers on how to configure the STNRGPF01 digital controller.

STNRGPF01 devices are a part of the STNRG family of STMicroelectronics digital devices designed for advanced power conversion applications. In this case the STNRGPF01 has integrated a complete application for interleaved power factor corrections and it's able to drive up to three interleaved channels.

The STNRGPF01 device contains all the control functions for designing a high efficiency interleaved PFC with sinusoidal line current consumption.

It works in the CCM at fixed frequency with average current mode control and it implements mixed signal (analog/digital) control offering the advantages of very high-end digital solution without typical limits of analog ones.

The STNRGPF01 can be configured by a dedicated software tool (eDesignSuite) in order to be customized for a specific application. So the user has to open the software tool, enters the converter specifications and runs the configurator. The results will be: the schematic, BOM, and binary code.

The binary code can be downloaded into the STNRGPF01 through the available programming interface having a customized device that can be used like an analog device ready to use in the application.

In the following pages will be described how it's possible to customize the device using the eDesignSuite step by step.
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1 Reference document

For hardware information about the STNRGPF01 controller please refer to the product datasheet.

2 Acronyms

Table 1. Acronyms

<table>
<thead>
<tr>
<th>Acronyms</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPFC</td>
<td>Interleaved power factor corrector</td>
</tr>
<tr>
<td>CCM</td>
<td>Continuous conduction mode</td>
</tr>
<tr>
<td>EMI</td>
<td>Electro Magnetic Interference</td>
</tr>
<tr>
<td>IVS</td>
<td>Input voltage sensing</td>
</tr>
<tr>
<td>ICS</td>
<td>Input current sensing</td>
</tr>
<tr>
<td>IOCP</td>
<td>Input overcurrent protection</td>
</tr>
<tr>
<td>OVS</td>
<td>Output voltage sensing</td>
</tr>
<tr>
<td>OCS</td>
<td>Output current sensing</td>
</tr>
<tr>
<td>TWG</td>
<td>Triangular waveform generator</td>
</tr>
<tr>
<td>CL</td>
<td>Current loop</td>
</tr>
<tr>
<td>VL</td>
<td>Voltage loop</td>
</tr>
<tr>
<td>PI</td>
<td>Proportional integral</td>
</tr>
<tr>
<td>BOM</td>
<td>Bill of material</td>
</tr>
</tbody>
</table>
3 Control structure

The STNRGPF01 device performs cascaded control for voltage and current loops in order to regulate the output voltage by acting on the total average inductor current. Figure 1 shows the STNRGPF01 control scheme.

Figure 1. STNRGPF01 control scheme

The device implements mixed signal (analog/digital) control.

The difference between the output voltage feedback $V_{\text{out.fb}}$ and reference $V_{\text{out.ref}}$ is sent to a digital PI which calculates the peak of the total input average current $i_{\text{pk.ref}}$ (digital section, green line).

The PFC current reference is internally generated and comes out from the I/O FFD block as the PWM signal. After filtering it becomes the total average sinusoidal input current reference ($i_{\text{tot.ref}}$) for the inner current loop (analog section, red line).

The difference between $i_{\text{tot.ref}}$ and the input current feedback $i_{\text{tot.fb}}$ is sent to the external analog PI. So the master PWM signal is generated by comparing the analog PI output $V_{\text{ctrl}}$ and a triangular wave $V_{\text{triang}}$ at switching frequency. Finally the interleaving operation is performed and three PWM signals 120° phase shifted (180° for two channels only) are generated. Moreover the I/O FFD block performs an input voltage and load feedforwards in order to improve the PFC transient response.
4 Device customization

In order to customize the device open the eDesignSuite and follow the following path:

Power Conversion
   Power Supply
      AC/DC
      PFC Pre-regulation
      STNRGPF01 CCM IPFC Controller

*Figure 2. Device customization. Project creation*
5 IPFC Specifications

In this section it's possible to insert the interleaved PFC Specifications by editing three subsections: Mains, Output, Other Parameters.

Figure 3. Interleaved PFC Specifications. General window
5.1 Mains

Here the user has to select the range of the input voltage with a specified line connection, for this purpose six combinations are possible:

1. Wide range (115 - 230 V, 50/60 Hz), line-neutral connection
2. EU range 230 V (185 - 265 Vac, 50 Hz), line-neutral connection
3. US range 115 V (90 -140 Vac, 60 Hz), line-neutral connection
4. Wide range (115 - 230 V, 50/60 Hz), line-line connection
5. EU range 230 V (185 - 265 Vac, 50 Hz), line-line connection
6. US range 115 V (90 -140 Vac, 60 Hz), line-line connection

Moreover it's possible to modify the values of the voltage directly in the text box, and the input custom range will appear automatically.
During this selection a red box will alert the user if the limits were exceeded.
5.2 Output

In the Output section six parameters can be selected (see eDesign help for more details):

1. Nominal Output Voltage: it's possible to set the DC bus voltage within the admitted range.
2. Maximum Power or Current: it's possible to define the output power or current.
3. Output Voltage Ripple: this parameter is used for output capacitor dimensioning.
4. Hold-Up Time: this parameter is used for output capacitor dimensioning.
5. Minimum Voltage after line drop: it's the minimum acceptable output voltage after a line interruption.
6. Maximum voltage: maximum admissible output voltage that the IPFC can reach in any condition. This voltage must be lower than the voltage rating of the output capacitor.
5.3 Other Parameters

Other IPFC parameters have to be inserted:
1. Number of Interleaved Channels: two or interleaved configuration.
2. Switching Frequency or Period: it's possible to define the channel switching frequency or period.
3. Inductor Current Ripple Percentage: in the CCM IPFC the inductor current ripple must be defined taking into account the following equation:

**Equation 1**

\[ \Delta I_{\text{ind}} = \Delta I_{\text{tot}} \times N_{\text{CH}} \]

where:
- \( \Delta I_{\text{ind}} \) = inductor current ripple
- \( \Delta I_{\text{tot}} \) = equivalent total input current ripple
- \( N_{\text{CH}} \) = number of interleaved channels

For example: if the total input current ripple is 20% and the number of channels is 3, the inductor current ripple according to **Equation 1** is:

**Equation 2**

\[ \Delta I_{\text{ind}} = 20 \times 3 = 60\% \]

In this input field the user has to insert 60.
5. Expected Average Efficiency: expected efficiency at the nominal voltage and rated output power.
6. Max. Local Ambient Temperature: maximum admissible ambient temperature. When the temperature exceeds this value the device will stop the switching activity.

Once specified all parameters, the user has three options (see **Figure 7**):

1. Custom Design: clicking on this box the Design Wizard will open and will be possible to complete the design in 15 steps.
2. Automatic Design: the design will be done automatically by default parameters.
3. Cancel: the tool will abort the current design.
6 Design steps

For the complex circuit design, usually a step design approach is preferred. Separating the circuit analysis in different sections, the tool can provide detailed information on parameters, which the user could customize, and their effects on the design. If one or more values exceed the specification, the tool shows an error message and stops the design process until errors are removed.

The design tool shows 15 different steps for the complete STNRGPF01 customization and board design. In the following pages, each design step is described.

6.1 Input Stage

In this section it's possible to customize the Input Stage.

![Figure 8. Design Wizard. Input Stage](image)
6.1.1  **Bridge info**  
In this section it's possible to see the maximum RMS current calculated at maximum power and minimum input voltage specified in *Section 5.1 on page 11*. In this way it's easy to select the rated current for the bridge rectifier.

6.1.2  **EMI Filter**  
In this section it's possible to estimate the losses in the common mode choke specifying the DC resistance of the winding.

6.1.3  **Input capacitor**  
In this section it's possible to select the input capacitor Cin. For each design a default value will be displayed, but in any case this value can be customized.

6.1.4  **Bridge Rectifier**  
In this section it's possible to estimate the losses in the input diodes. For the losses calculation the following parameter are considered:

- Input current (Irms)
- Diode dynamic resistance
- Diode forward voltage

The user can evaluate the losses inserting the diodes dynamic resistance (if available) and the forward voltage drop.

For all sections when all parameters are inserted the user has the following choices:

- Next.: the tool will go into the next window
- Prev.: the tool will go into the previous window
- Auto Complete: The tool will go into the final window
- Cancel: the tool will abort the design
6.2  Boost Inductor

In this section it’s possible to customize the boost inductor value and verify if the current ripple is below the target.

Figure 9. Design Wizard. Boost Inductor

Looking to Figure 9 the design tool will display info on: the inductance value, maximum peak current and current ripple percentage.

The user can modify only the inductor value in µH and verify the actual current ripple percentage.

If the user enters an inductance value too low and the ripple percentage is higher than target a warning will appear - see Figure 10.
The warning “actual current ripple percentage differs too much from target” will stop the design and the user has two possibilities now:

1. To increase the inductor in order to have a ripple percentage within the specification.
2. To accept this value by clicking on “Redesign with actual target” see Figure 11. In this way the specification inserted in Section 5.3 on page 14 will be modified with the actual value.
Figure 11. Design Wizard. Boost Inductor redesign
6.3 Power Switch

In this section it's possible to select the power switch for each channel. The user has the possibility to select the MOSFET or IGBT. See Figure 12.

Figure 12. Design Wizard. Switch selection

As it's possible to see in Figure 12, the tool automatically will select a switch. The selection will be done on the minimum losses criteria and the losses estimation will be displayed. However the user can see the complete searching results window, by clicking on the displayed part number.
In this case the window in Figure 13 will open and other switches can also be selected. The user has two possibilities now:

- To select a device by clicking on “Select”.
- To insert a custom MOSFET by clicking on “Cancel” and come back to Figure 12.
Selecting “Define custom MOSFET” (Figure 14) a window will open. See Figure 15.

In this window the user has to insert few parameters and click OK.

The same procedure will be applied for the IGBT selection.
6.4 Boost Diode

In this section it's possible to select the boost diode for each channel. The user has the possibility to include or not for automatic selection the SiC diodes. The automatic selection will be done on minimum losses criteria. The user has three choices - see from Figure 16 to Figure 18.

1. To evaluate the automatic selection.

Figure 16. Design Wizard. Boost Diode selection
2. To select a diode from the proposed ST set.

**Figure 17. Design Wizard. Boost Diode searching results**

![Diode Selection Table]

3. To insert a custom diode.

**Figure 18. Design Wizard. Custom Boost Diode’s parameters**

![Custom Diode’s Parameters]

In this window the user has to insert few parameters and click OK.
6.5 Output Stage
In this section, it is possible to sizing the output capacitor.

6.5.1 Output IPFC Specification
The first set of parameters defines the output voltage features.
Below the parameters that have to be specified:
- Output voltage ripple (absolute value or percentage)
- Hold-up time
- Minimum voltage after line drop

6.5.2 Output capacitor
- Number of parallel capacitors
- Single capacitance

6.5.3 Output Stage Results
The second section shows the results on the following parameters:
- Output capacitance
- Actual output voltage ripple
- Actual hold-up time
- Single output capacitor current rating
Note: A message will indicate the minimum rated voltage of electrolytic capacitors.
6.6 Input Voltage Sensing

In this section the user can design the voltage divider in order to measure input voltage.

6.6.1 IVS Resistor Divider Specification

The first set of parameters defines the resistors divider:
- Lower resistor (RL_IVS)
- Number of upper resistors in series
- Single upper resistance (RH_IVS)

6.6.2 Input Voltage Sensing Results

After the voltage divider specification the user can verify immediately the following parameters:
- IVS Target Voltage (maximum applicable to the pin 31, VIN)
- IVS power losses
- IVS current

![Figure 20. Design Wizard for Input Voltage Sensing](image-url)
6.7 Input Current Sensing

In this section the user can design the circuit to measure the input current for the current control loop and overcurrent protection.

6.7.1 ICS Resistor

The first set of parameters defines the sense, input and feedback resistors.
- Sense resistor (R144)

6.7.2 ICS Op-Amp Resistors

- Input resistors (R146, R147)
- Feedback resistors (R148, R149)

6.7.3 Input Current Sensing Results

In the “Results” section the user can verify the following values:
- ICS Target voltage
- Maximum peak current on R144
- RMS current on R144
- ICS max output voltage (with selected resistors)
- Max peak voltage on R144
- Max power losses on R144
Figure 21. Design Wizard. Input Current Sensing

Design Steps
- Interleaved PFC Specifications
- Input Stage
- Boost Inductor
- Power Switch
- Boost Diode
- Output Stage
- Input Voltage Sensing
- Input Current Sensing
- Input Over Current Protection
- Output Voltage Sensing
- Output Current Sensing
- Triangular Waveform Generator
- Current Control Loop
- Voltage Control Loop
- Additional Features

Input Current Sensing

ICS Resistor
- Sense resistor (R144) 4 mΩ

ICS Op-Amp Resistors
- Input resistors (R146, R147) 8.2 kΩ
- Feedback resistors (R148, R149) 20 kΩ

Input Current Sensing Results
- ICS target voltage: 3 V
- ICS max output voltage: 2.99 V
- Maximum peak current on R144: 30.6 A
- Max peak voltage on R144: 122.39 mV
- RMS current on R144: 16.71 A
- Max power losses on R144: 1.12 W

Diagram of circuit components and values.
6.8 **Input Over Current Protection**

In this section the user can design the circuit to realize the overcurrent protection. The output voltage of sensing circuitry is connected to the OCP1 pin by a voltage divider and a low-pass filter.

6.8.1 **IOCP Resistors Specification**

The first set of parameters defines the circuit resistors.
- IOCP target: maximum current admitted
- Lower resistor (RL_OCP)
- Upper resistor (RH_OCP)

6.8.2 **IOCP RC-Filter**

- Filter resistor (RF_OCP)
- Filter Capacitor (CF_OCP)

6.8.3 **Input Over Current Protection Results**

In the “Results” section the user can verify the following values:
- IOCP real
- Maximum voltage on OCP1 pin
- Cutoff frequency (IOCP filter)
Figure 22. Design Wizard. Input Over Current Protection

Design Steps
- Interleaved PFC Specifications
- Input Stage
- Boost Inductor
- Power Switch
- Boost Diode
- Output Stage
- Input Voltage Sensing
- Input Current Sensing
  - Input Over Current Protection
- Output Voltage Sensing
- Output Current Sensing
- Triangular Waveform Generator
- Current Control Loop
- Voltage Control Loop
- Additional Features

Input Over Current Protection

- Disabled
- IOCP target: 32.21 A

IOCP Resistors Specification
- Lower resistor [RL_IOC]: 6.2 kΩ
- Upper resistor [RH_IOC]: 12 kΩ

IOCP RC-Filter
- Filter resistor [RF_IOC]: 1.1 kΩ
- Filter Capacitor [CF_IOC]: 560 pF

Input Over Current Protection Results
- IOCP real: 32.07 A
- Maximum voltage on CCP1 pin: 1.07 V
- Cutoff frequency: 258.37 kHz
6.9 Output Voltage Sensing
In this section the user can design the circuit to measure the output voltage.

6.9.1 OVS Resistor Divider Specification
In this section the voltage divider resistors are defined.
- Lower resistor (RL_OVS)
- Upper resistor in series
- Single upper resistance (RH_OVS)

6.9.2 Output Voltage Sensing Results
In the “Results” section the user can verify the following values:
- OVS Target Voltage (maximum applicable to the pin 34, VOUT)
- OVS power losses
- OVS current

Figure 23. Design Wizard. Output Voltage Sensing
6.10 Output Current Sensing
In this section it is possible to customize the output current sense circuit.

6.10.1 OCS Resistor
In this section the output sensing resistor is defined.
- Sense resistor (R9)

6.10.2 OCS Op-Amp Resistors
- Input resistors (R25, R28)
- Feedback resistors (R26, R36)

6.10.3 Output Current Sensing Result
In the “Results” section the user can verify the following values:
- OCS Target voltage (maximum applicable to the pin 33, IOUT)
- Max peak current on R9
- RMS current on R9
- OCS max output voltage
- Max peak voltage on R9
- Max power losses on R9
Figure 24. Design Wizard. Output Current Sensing

Design Wizard

- Design Steps
  - Interleaved PFC Specifications
  - Input Stage
  - Boost Inductor
  - Power Switch
  - Boost Diode
  - Output Stage
  - Input Voltage Sensing
  - Input Current Sensing
  - Input Over Current Protection
  - Output Voltage Sensing
  - Output Current Sensing
  - Triangular Waveform Generator
  - Current Control Loop
  - Voltage Control Loop
  - Additional Features

Output Current Sensing

- OCS Resistor
  - Sense resistor [R9]: 28 mΩ

- OCS Op-Amp Resistors
  - Input resistors (R25, R28): 42 kΩ
  - Feedback resistors (R26, R36): 330 kΩ

Output Current Sensing Results

- OCS Target Voltage: 1.25 V
- OCS max output voltage: 1.23 V
- Max peak current on R9: 8.25 A
- Max peak voltage on R9: 231 mV
- RMS current on R9: 7.5 A
- Max power losses on R9: 1.58 W

Diagram:

- TSV911LT
- Components and connections

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6.11 Triangular Waveform Generator

In this section it's possible to customize the triangular waveform generator.

6.11.1 TWG Op-Amp Specification

The triangular generator hardware components that can be customized are:
- Parallel capacitor (C56)
- Feedback resistor (R137)

6.11.2 TWG Resistor Divider Specification

Moreover the triangular generator voltage divider can be customized.
- Lower resistor (R142)
- Higher resistor (R141)

6.11.3 Triangular Waveform Generator Results

In the “Results” section the user can verify the following values:
- Input resistor (R140)
- TWG Target peak voltage
Figure 25. Design Wizard. Triangular Waveform Generator
6.12 Current control loop

In this section it’s possible to customize the analog current compensator.

6.12.1 Current loop specification

The user has to insert the current open loop specifications:
- Required CL bandwidth
- Required CL phase margin

6.12.2 Op-amp compensator specification

Hardware components of the analog compensator can be specified:
- Feedback capacitor (C_{fz})
- Input resistor (R_i)
- Feedback resistor (R_f)
- Feedback capacitor (C_{fp})

Figure 26. Design wizard. PI type II op-amp compensator

The user can proceed in two ways:
- Inserting the specification (bandwidth and phase margin) and obtaining the hardware components values.
- Selecting hardware components (R_i, R_f, C_{fz}, C_{fp}) and verifying the resulting bandwidth and phase margin.
6.12.3 **Current Control Loop Results**

In the “Results” section the user can verify the current open loop specifications and resulting Bode Diagram (see Figure 27).

![Figure 27. Design Wizard. Current Control Loop](image)

6.13 **Voltage Control Loop**

In this section it's possible to customize the digital PI controller for the PFC output voltage regulation.

6.13.1 **Voltage Loop Specification**

The user has to define the voltage open loop specifications:

- Required VL bandwidth
- Required VL phase margin
6.13.2 Digital PI Parameters Specification

In this case digital parameters are:
- Digital Kp (proportional gain)
- Digital Ki (integral gain)

The user can proceed in two ways:
- Selecting voltage loop specifications (bandwidth and phase margin) and obtaining parameters Kp and Ki
- Selecting Kp and Ki and verifying the bandwidth and phase margin

6.13.3 Voltage Control Loop Results

In the “Results” section the user can verify the voltage open loop specifications as well as the Bode Diagram.

Figure 28. Design Wizard. Voltage controller
6.14 Additional Features

In this section it’s possible to configure the following features (see the STNRGPF01 datasheet):

- TINRUSH: inrush current limiter time (pin 21)
- Min power for fan: the power level able to start the fan or an other cooling system (pin 20)
- Max power switch 1 -> 2 channels: the transition power level from one to two channels operations
- Max power switch 2 -> 3 channels: the transition power level from two to three channels operations
- Max power startup: the maximum resistive load that can be connected at the start-up (see eDesign help)
- Min voltage burst: the minimum level of the output voltage during the burst operation
- Max voltage burst: the maximum level of the output voltage during the burst operation

![Figure 29. Design Wizard. Additional design Features](image)

Once all parameters have been inserted, when the user clicks on the OK button, the design is completed.
7 Design summary

At the end of the design steps tool it’s possible to have a summary of the entire project.

Figure 30. Design summary. Overview

7.1 PFC Specifications pane

The PFC Specifications pane provides a summary of the selected high-level specification.

Figure 31. Design summary. The Specification pane

Click on “Change Specifications” to modify design specifications and generate an updated design.
7.2 **Actuals pane**

The Actuals pane displays ([Figure 10 on page 18](#)) the predicted performance of the design based on the I/O operating conditions you can select using the icon.

![Figure 32. Design summary. The Actuals pane](image1)

![Figure 33. Design summary. The Actuals pane - detail](image2)

A warning icon appears if some values do not match the design target, and these values are displayed in red.
7.3 Schematic: annotated, interactive and hierarchical

This pane (Figure 34) shows the full schematic of your design. The schematic is annotated with the values for each element of the circuit.

Figure 34. Design summary. Interactive and hierarchical schematic

By interacting with the schematic, you can customize components (identified by the light blue script) and the subnetwork (identified by icon), or to go into the subnet on the block which shows the hand cursor.

Figure 35. Design summary. Schematic of the Output Current Sensing
For example, if the user clicks on $V_{CC}$ (Figure 36) a new design for the auxiliary power supply will start.

In this case the ALTAIR05T-800 device is used.
Figure 38. Design summary. Converter Specifications
7.4 BOM

The bill of materials (BOM) view provides an effective user interface (table format) for all circuit components and their characteristics (Figure 15 on page 22). You can customize the design by interacting with the BOM view.

![Figure 39. Design summary: BOM](image)

<table>
<thead>
<tr>
<th>Type</th>
<th>Reference</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bridge Rectifier</td>
<td>BR_diode</td>
<td>100 mΩ</td>
<td>Vθ=7.1 V</td>
</tr>
<tr>
<td>Capacitor C15</td>
<td>220 nF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor C17</td>
<td>220 nF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor C18</td>
<td>100 nF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor C23</td>
<td>10 nF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor C24</td>
<td>100 nF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor C25</td>
<td>330 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor C26</td>
<td>1.5 nF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor C33</td>
<td>100 nF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor C33_1</td>
<td>100 nF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor C54</td>
<td>1 μF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor C54_1</td>
<td>1 μF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor C54_2</td>
<td>1 μF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7.5 Analysis diagrams

Based on the selected operating conditions, analysis diagrams will display the following entities:

- Losses
- Bode diagram from analog current control loop
- Digital voltage control loop

![Figure 40. Design summary. Analysis diagrams](image)

Click on the enlarge icon to display more details about the selected analysis diagram.
7.5.1 Power Losses

In the analysis diagram menu the user has the possibility to evaluate the losses in the main circuitual parts.

Figure 41. Design summary. Power Losses menu

By clicking on the icon the tool will display more details about the losses and an estimation of the system efficiency.

Figure 42. Design summary. Power Losses Details

By clicking on the icon of the Schematic window the design summary page will be displayed (see Figure 30 on page 41).
7.5.2 Current loop

In the analysis diagram menu the user can analyze the current open loop Bode diagram.

**Figure 43. Design summary. Current open loop Bode diagram**

![Current open loop Bode diagram](image)

By clicking on the icon the tool will display Bode diagram details.

**Figure 44. Design summary. Current open loop Bode diagram details**

![Current open loop Bode diagram details](image)

By clicking on the icon of the Schematic window the design summary page will be displayed (see Figure 30 on page 41).
7.5.3 Voltage loop

In the analysis diagram menu the user can analyse the voltage open loop Bode diagram loop design.

Figure 45. Design summary. Voltage open loop Bode diagram

![Voltage open loop Bode diagram]

By clicking on the icon the tool will display Bode diagram details.

Figure 46. Design summary. Voltage open loop Bode diagram details

![Voltage open loop Bode diagram details]

By clicking on the icon of the Schematic window the design summary page will be displayed (see Figure 30 on page 41).
7.6 Design commands

Near the eDesignSuite logo the tool offers a set of commands to manage the design.

Figure 47. Design summary for design commands

- **Redesign** button: opens the first design step
- **Save** button: opens a drop down menu

Figure 48. Design summary. Save menu

- **Save**: allows saving the current design project on the ST server
- **Save As**: allows saving the current design project with a different name on the ST server
- **Export to File**: allows exporting the current design project on a local system file
- **Export BOM as XML**: allows exporting the bill of materials as an XML file
- **Export to PSpice**: allows exporting the current design project for the PSpice simulation (command available only for some designs)
- **Print** button generates a printable report of the current design project
- **Disclaimer** button displays the STMicroelectronics disclaimer
7.7 Firmware

Each time the user creates or redefine a design, the tool generates a customized firmware, which can be saved on a remote PC in a *.hex file format.

Firmware downloading *.hex file

The firmware button placed into the IC box starts the downloading process by clicking on the Firmware icon.

**Figure 49. Design summary. Download procedure**

Confirm the downloading operation.

**Figure 50. Design summary. Download confirmation**

Select the folder and file name.
Figure 51 shows the window opened after the downloading confirmation. Please select the folder name, the output file name and by clicking on the “Save” icon save locally the personalized firmware.
8  STNRGPF01 programming

To complete the process described in Section 7.7, STMicroelectronics offers an additional hardware and software utility to download the *.hex file into the STNRGPF01.

Warning: The programming procedure described below must be performed only when the interleaved PFC is NOT CONNECTED TO THE MAINS.

- Insert an FTDI cable into the USB port of the PC.
- Insert the adapter board into the programming ports PTX and PRX of the STNRGPF01 (see Figure 52).

Figure 52. Adapter board - control board connection

- Connect the adapter board with the FTDI cable (see Figure 53).
As soon as the adapter will be connected with the cable FTDI, the LED on the top will be lit.

- Open the STNRGPF01 loader utility
- Select the PC COM port

Open the file folder and select the "*.hex file."
Figure 55. STNRGPF01 programming: *.hex file selection

- Click on the “Download” button.

Figure 56. STNRGPF01 programming. Download

Now the programming procedure is completed.
9 Revision history

Table 2. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>21-Apr-2017</td>
<td>1</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>