TN0946
Technical note

Results of the conformance tests performed on the STM8 LIN software package release 5.1

Introduction

This document describes the tests that were performed on the STM8 LIN software package (STSW-STM8A-LIN) release 5.1 to check the conformance with LIN specification.

Table 1. Applicable software

Type	Part number
Software	STSW-STM8A-LIN

Table 2. Reference documents

Document name	Version
LIN conformance test specification for the LIN specification package revision 2.0 (in particular LIN OSI Layer 2 – Data Link Layer)	1.0 [01/08/2004]
LIN specification package revision 2.1 of LIN consortium	2.1 [24/11/2006]
Release note RN0086, “Description of STM8 LIN software package (STSW-STM8A-LIN) release 5.1”	2.0
LIN specification package revision 2.0 of LIN consortium	2.0 [18/09/2003]
C cross compiler user guide for STM8 (delivered inside the compiler package)	4.3.9
LIN conformance test specification for LIN specification package 2.1	2.1 [10/10/2008]

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1 Hardware requirements

The following figures and tables illustrate the hardware used and the connections for performing the conformance tests on STM8 LIN package release 5.1.

STM8/128-EVAL board:

- *Figure 1* and *Table 3* show the hardware connections required on STM8/128-EVAL for testing STM8 LIN package release 5.1 using the UART1 on STM8AF devices for slave and master nodes.
- *Figure 2* and *Table 4* show the hardware connections required on STM8/128-EVAL for testing STM8 LIN package release 5.1 using UART2 or UART3 on STM8AF devices for slave and master nodes.

Figure 1. Hardware requirements for testing LIN driver on STM8AF UART1

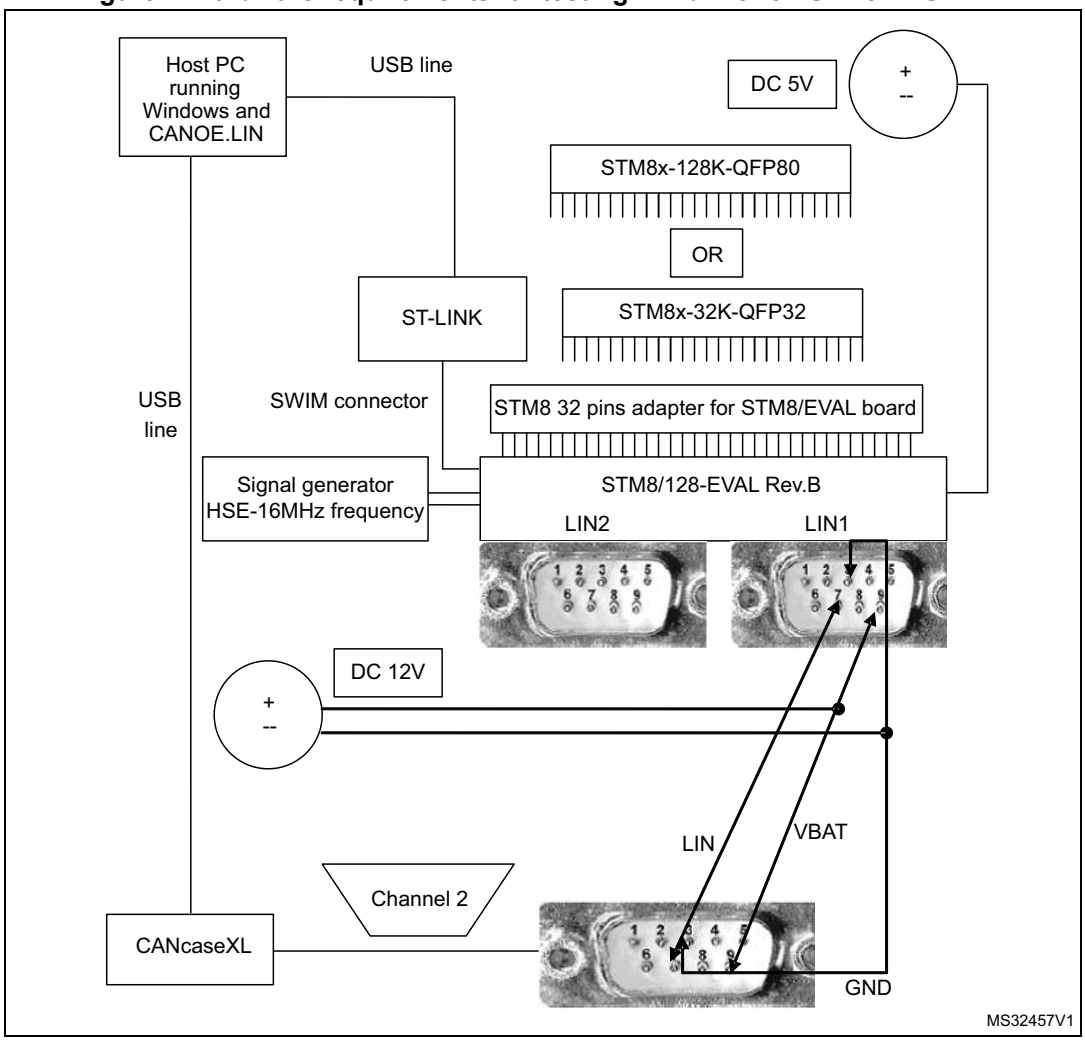


Figure 2. Hardware configuration for testing LIN driver on STM8AF UART2 or UART3

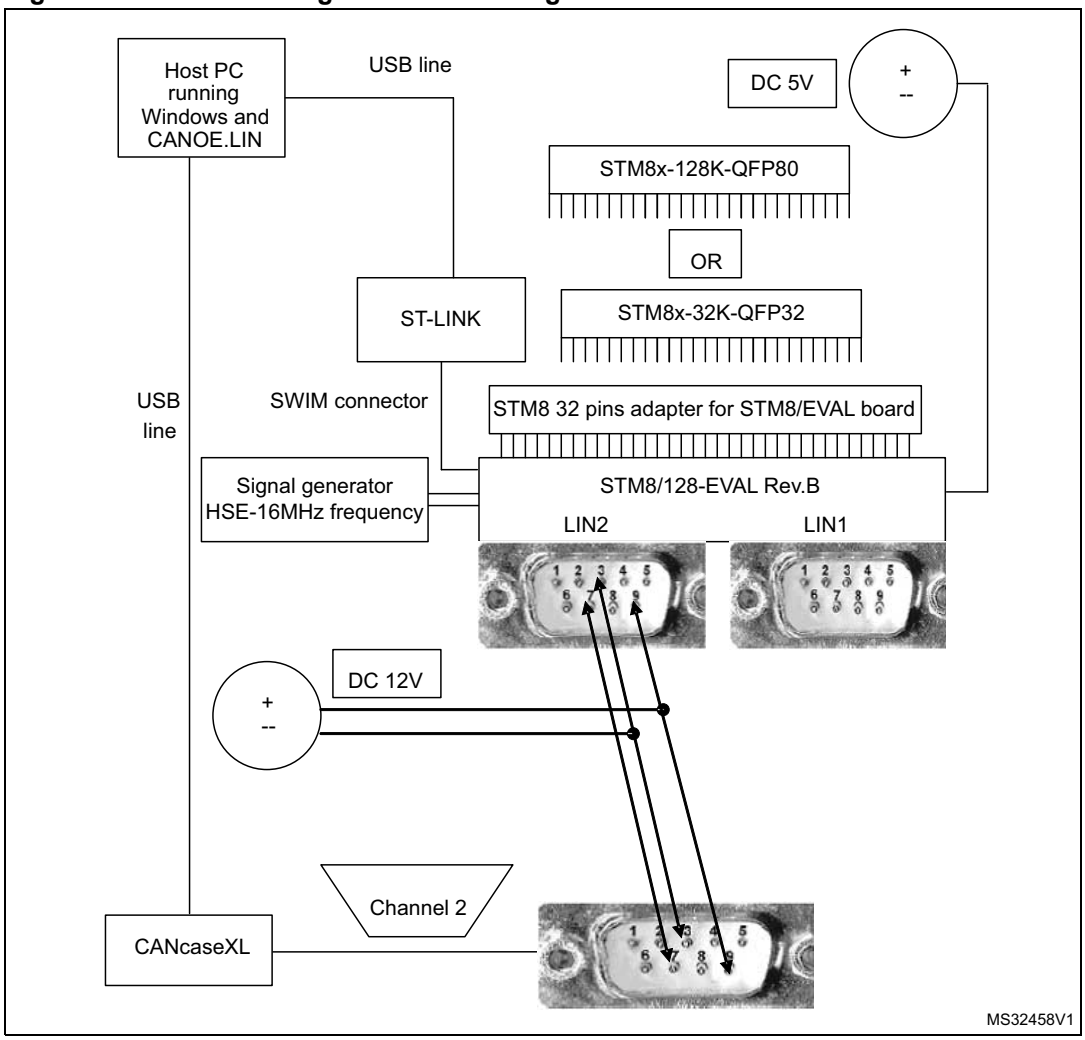


Table 3. Connections between CANcaseXL and STM8/128-EVAL rev. B board for testing STM8 LIN package V5.1 on UART1

STM8/128-EVAL rev. B	CANcaseXL	Node tested
USART/UART1 - LIN_SCI2 serial interface		
LIN1 RS232 PIN 3 (GND)	Channel 2 RS232 PIN 3 (GND)	Master / Slave
LIN1 RS232 PIN 7 (LIN)	Channel 2 RS232 PIN 7 (LIN)	Master / Slave
LIN1 RS232 PIN 9 (VBAT)	Channel 2 RS232 PIN 9 (VBAT)	Master / Slave

Table 4. Connections between CANcaseXL and STM8/128-EVAL rev. B board for testing STM8 LIN package V5.1 on UART2 or UART3

STM8/128-EVAL rev. B	CANcaseXL	To use to test with
LINUART/UART2 or UART3 - LIN_SCI1 serial interface		
LIN2 RS232 PIN 3 (GND)	Channel 2 RS232 PIN 3 (GND)	Master / Slave
LIN2 RS232 PIN 7 (LIN)	Channel 2 RS232 PIN 7 (LIN)	Master / Slave
LIN2 RS232 PIN 9 (VBAT)	Channel 2 RS232 PIN 9 (VBAT)	Master / Slave

Table 5. Connections between signal generator and STM8/128-EVAL board rev. B

Signal Generator	Phytec Minimodule	Note
HSE SIGNAL	PA1	OSCIN
GND	Every ground	

Table 6. Jumper settings for STM8/128-EVAL board rev. B

Jumper location	Jumper name	Description
STM8/128-EVAL rev. B	JP3 (1+2) and (3+4) shorted	Power connector/daughter board jumper
STM8/128-EVAL rev. B	CN1 pin 10 shorted with CN1 pin 12	CN1 pin 10 == PG6 CN1 pin 12 == GND PG6 shorted to GND redirects LINUART/UART2 or UART3 TX/RX signals (LIN_MULTIPLEXER_1) to LIN2 port connector (CN14 DB9-male LIN2).
STM8/128-EVAL rev. B	CN1 pin 22 shorted with CN1 pin 49	CN1 pin 22 == PG3 CN1 pin 49 == D5V PG3 shorted to D5V enables LIN_EN_2 signal to enable LIN2 transceiver on LIN2 port connector (CN14 DB9-male LIN2).
STM8/128-EVAL rev. B	CN1 pin 22 shorted with CN1 pin 49	CN1 pin 34 == PC2 CN1 pin 36 == PC0 PC0 is connected to the button present on the evaluation board. When using the 32-pin adapter, PC2 must be shorted to PC0. This button is needed to test the events.
STM8/128-EVAL rev. B	CN5 pin 19 shorted with CN5 pin 28	CN5 pin 19 == D5V CN5 pin 28 == PF7 PF7 shorted to D5V enables LIN_EN_1 signal to enable LIN1 transceiver on LIN1 port connector (CN11 DB9-male LIN1).
STM8/128-EVAL rev. B	CN5 pin 31 and CN5 pin 29 shorted with CN5 pin 50	CN5 pin 29 == PF6 CN5 pin 31 == PF5 CN5 pin 50 == GND PF5 and PF6 shorted to GND redirects USART/UART1 TX/RX signals (USART_MULTIPLEXER_1 and USART_MULTIPLEXER_2) to LIN1 port connector (CN11 DB9-male LIN1).

STM8A-DISCOVERY:

Figure 3 and *Table 7* shows the hardware connections required on the STM8AL board of STM8A-DISCOVERY for testing STM8 LIN package release 5.1 using the USART on the STM8AL device for Slave.

Figure 4 and *Table 7* shows the hardware connections required on the STM8AF board of STM8A-DISCOVERY for testing STM8 LIN package release 5.1 using the LINUART on the STM8AF device for Master.

Hardware configuration for testing LIN driver on STM8AF board of STM8A-DISCOVERY

Table 7. Connections between CANcaseXL and STM8AL or STM8AF board of STM8A-DISCOVERY for testing STM8 LIN package V5.1 on USART

STM8A-DISCOVERY (STM8AF/STM8AL board)	CANcaseXL	Node tested
USART – LIN_SCI1 serial interface		
CN3 or CN4 Pin 1 (GND)	Channel 1 Pin 3	Master/Slave
CN3 or CN4 Pin 4 (LIN)	Channel 1 Pin 7	Master/Slave
CN3 or CN4 Pin 2 (VBAT)(1)	Channel 1 Pin 9	Master/Slave

1. +12 V must be supplied on STM8A-DISCOVERY CN3 or CN4 Pin 2 (VBAT).

Figure 3. Hardware configuration for testing LIN driver on STM8AL board of STM8A-DISCOVERY

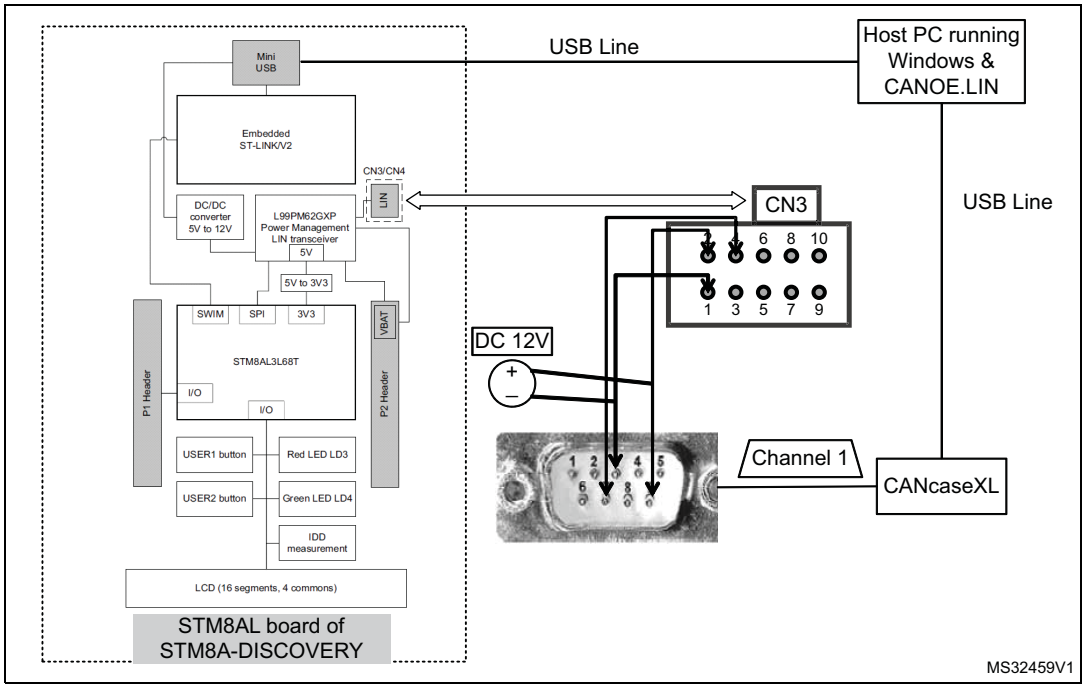
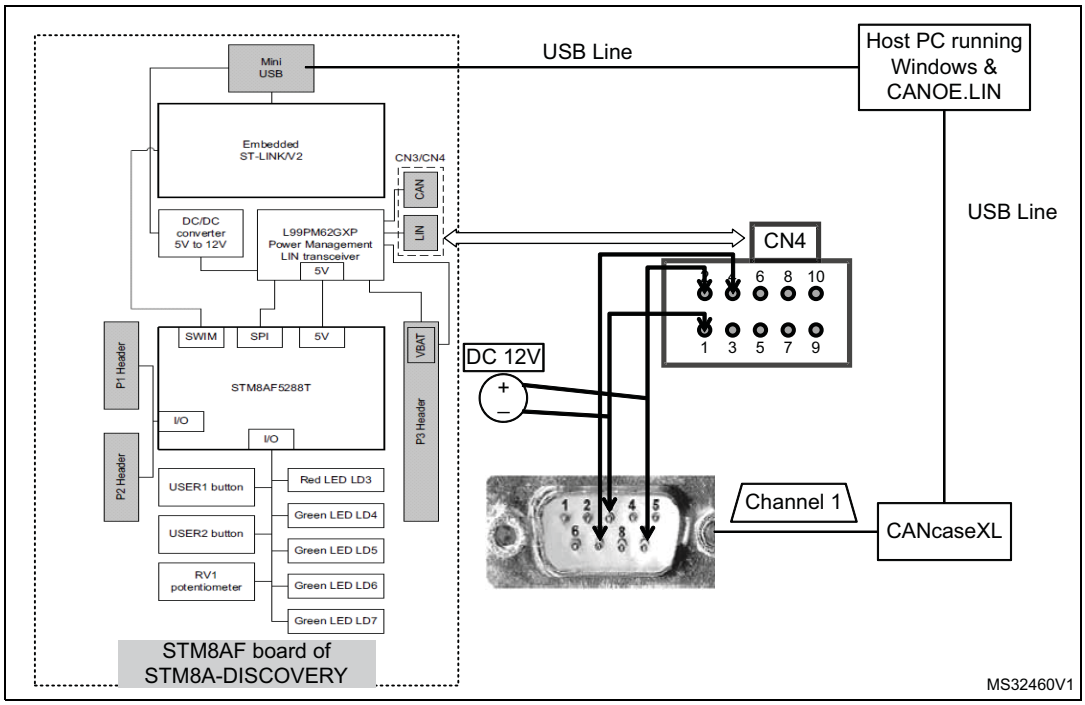


Figure 4. Hardware configuration for testing LIN driver on STM8AF board of STM8A-DISCOVERY



2 Software requirements

Table 8. Software environment

Item	Note	Version
STM8 LIN package	It includes the LIN driver (Master & Slave) for STM8A on UART1, UART2 or UART3 and LIN driver (Slave) for STM8AL on USART	5.1(1)
STVD7	ST7 Visual Develop	4.3.3
Compiler	CXSTM8 COSMIC C compiler	4.3.9
CANOE.LIN	Version 6.0.63 (SP3) has been used to test LIN 2.0 slave conformance while version 7.2.42 (SP1) is used to test the LIN 2.1 slave conformance and the LIN 2.0 master conformance.	7.2.42 (SP1) or 6.0.63 (SP3)
Lingen	Application allowing to generate lin_cfg.c, lin_cfg.h and lin_cfg_types.h files.	3.5.0.STM

1. Some compiler optimizations have been done in *demo* → *stm8_128-eval* → *slave* for STM8AF6223 and STM8AF6226T devices.

3 Tested configurations

The following configuration has been tested to verify the conformance of the STM8AF52AA microcontroller with LIN 2.0 master and LIN 2.x slave:

- LIN 2.0 conformance for master node
- LIN 2.0 and LIN 2.1 conformance for slave node
- UART1 (only for master node) and UART2 or UART3 (master and slave)
- Baudrate: 2400, 9600, 10417, 19200, 20000 bps
- Clock: 16 MHz external clock (quartz) for master node, 16 MHz internal RC oscillator (for slave node)
- Autosync (only for UART2 or UART3 slave nodes): enabled
- 128-Kbyte STM8AF52AA microcontroller in LQFP80 package.

The following configuration has been tested to verify the conformance of the STM8AL microcontroller with LIN 2.x slave:

- LIN 2.0 and LIN 2.1 conformance for slave node
- USART (for slave node)
- Baudrate: 2400, 9600, 10417, 19200, 20000 bps
- Clock: 16 MHz external clock (quartz)
- 32-Kbyte STM8AL microcontroller in LQFP 48 pin package.

The following configuration has been tested to verify the conformance of the STM8AF6226 microcontroller with Lin 2.0 & 2.1 slave:

- LIN 2.0 and LIN 2.1 conformance for slave node
- LINUART (for slave node)
- Baudrate: 2400, 9600, 10417, 19200, 20000 bps
- Clock: 16 MHz Internal RC oscillator
- 8 Kbyte STM8AF6226T microcontroller (in LQFP32 package).

4 Results of LIN 2.0 slave conformance tests

The following tables give the results of the tests performed on STM8AF LINUART and STM8AL USART.

4.1 LIN 2.0 slave – LIN OSI layer 2 – data link layer

Table 9. LIN 2.0 slave test list: LIN OSI layer 2 – data link layer

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
2	**Timing parameters**						
2.2.1	Variation of length of SYNCH BREAK LOW PHASE	PASS	PASS	PASS	PASS	PASS	
2.2.2	Variation of length of SYNCH BREAK LOW PHASE	PASS	PASS	PASS	PASS	PASS	
2.2.3	Variation of length of SYNCH BREAK LOW PHASE	PASS	PASS	PASS	PASS	PASS	
2.4.1	Variation of length of SYNCH BREAK DELIMITER	PASS	PASS	PASS	PASS	PASS	
2.4.2	Variation of length of SYNCH BREAK DELIMITER	PASS	PASS	PASS	PASS	PASS	
2.4.3	Variation of length of SYNCH BREAK DELIMITER	PASS	PASS	PASS	PASS	PASS	
2.6.1	Variation of length of Header	PASS	PASS	PASS	PASS	PASS	
2.6.2	Variation of length of Header	PASS	PASS	PASS	PASS	PASS	
2.6.3	Variation of length of Header	PASS	PASS	PASS	PASS	PASS	
2.6.4	Variation of length of Header	PASS	PASS	PASS	PASS	PASS	
2.8	Oscillator tolerance without making use of Synchronization	PASS	PASS	PASS	PASS	PASS	
2.9	Oscillator tolerance with making use of Synchronization	PASS	PASS	PASS	PASS	PASS	
2.10	Length of Frame, IUT as Slave answering to a Master request	PASS	PASS	PASS	PASS	PASS	
2.10.1	IUT as Slave	PASS	PASS	PASS	PASS	PASS	

Table 9. LIN 2.0 slave test list: LIN OSI layer 2 – data link layer (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
3	**Communication without failure**						
3.1	Variation of LIN Identifier	PASS	PASS	PASS	PASS	PASS	
3.1.2	IUT as Slave	PASS	PASS	PASS	PASS	PASS	
3.2	Transmission of the Checksum Byte	PASS	PASS	PASS	PASS	PASS	
3.2.1	IUT as Slave	PASS	PASS	PASS	PASS	PASS	
3.3	Extended Frame, Reserved	PASS	PASS	PASS	PASS	PASS	
3.5	Command Frame ‘Master Request’	PASS	PASS	PASS	PASS	PASS	
3.7	Command Frame ‘Slave Response Frame’	PASS	PASS	PASS	PASS	PASS	
3.8	Supported Frames according to the IUT specification	PASS	PASS	PASS	PASS	PASS	
4	**Communication with failure**						
4.1.1	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.2	Bit Error	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 1-2 with Bit 1 inverted – Not Applicable
4.1.3	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.4	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.5	Bit Error	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 2-3 with Bit 1 inverted – Not Applicable
4.1.6	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.7	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.8	Bit Error	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 3-4 with Bit 1 inverted – Not Applicable
4.1.9	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.10	Bit Error	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Data Byte 4, with Bit 4 inverted - Dominant bit inversion (not applicable)

Table 9. LIN 2.0 slave test list: LIN OSI layer 2 – data link layer (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
4.1.11	Bit Error	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 4-5 with Bit 1 inverted – Not Applicable
4.1.12	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.13	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.14	Bit Error	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 5-6 with Bit 1 inverted – Not Applicable
4.1.15	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.16	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.17	Bit Error	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 6-7 with Bit 1 inverted – Not Applicable
4.1.18	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.19	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.20	Bit Error	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 7-8 with Bit 1 inverted – Not Applicable
4.1.21	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.22	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.1.23	Bit Error	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 8-CS with Bit 1 inverted – Not Applicable
4.1.24	Bit Error	PASS	PASS	PASS	PASS	PASS	
4.2	Checksum Error	PASS	PASS	PASS	PASS	PASS	
5	**Event triggered frames**						
5.1.1	Without trigger event	PASS	PASS	PASS	PASS	PASS	
5.1.2	With trigger event	PASS	PASS	PASS	PASS	PASS	

4.2 LIN 2.0 slave – node configuration / network management

Table 10. LIN 2.0 slave test list: node configuration / network management

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
2	**Status management**						
2.1	Error in Received frame	PASS	PASS	PASS	PASS	PASS	
2.2	Error in Transmitted frame	PASS	PASS	PASS	PASS	PASS	
2.3	Error in Transmitted frame with collision	PASS	PASS	PASS	PASS	PASS	
3	**Sleep / wakeup tests**						
3.2	Receive Command Frame ‘Sleep Mode Command’	PASS	PASS	PASS	PASS	PASS	
3.4	Receive a Wake Up request	PASS	PASS	PASS	PASS	PASS	
3.5	Send a Wake up request	PASS	PASS	PASS	PASS	PASS	
3.5.1	IUT as Slave	PASS	PASS	PASS	PASS	PASS	
3.5.2	No Following Frame Header from a master	PASS	PASS	PASS	PASS	PASS	Where LIN_WAKEUP_RETRIES_MAX is 3
3.5.3	Frame Header from a Master following	PASS	PASS	PASS	PASS	PASS	
3.6	Sleep Mode after Bus Idle	PASS	PASS	PASS	PASS	PASS	
4	**Node configuration**						
4.1	Frame ID Assignment	PASS	PASS	PASS	PASS	PASS	
4.1.1	With indirect response	PASS	PASS	PASS	PASS	PASS	
4.1.2	With direct response	PASS	PASS	PASS	PASS	PASS	
4.2	LIN Product ID	PASS	PASS	PASS	PASS	PASS	
4.2.1	With direct response	PASS	PASS	PASS	PASS	PASS	

Table 10. LIN 2.0 slave test list: node configuration / network management (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
4.2.2	With indirect response	PASS	PASS	PASS	PASS	PASS	
4.3	Read by Identifier Command	PASS	PASS	PASS	PASS	PASS	
4.3.1	With correct NAD	PASS	PASS	PASS	PASS	PASS	
4.3.2	With incorrect NAD	PASS	PASS	PASS	PASS	PASS	
4.3.2.1	With incorrect NAD	PASS	PASS	PASS	PASS	PASS	
4.3.3.1	With incorrect Supplier ID	PASS	PASS	PASS	PASS	PASS	
4.3.4.1	With incorrect Function ID	PASS	PASS	PASS	PASS	PASS	
4.4	NAD Assignment	PASS	PASS	PASS	PASS	PASS	
4.4.1	Followed by “Read by Identifier”	PASS	PASS	PASS	PASS	PASS	
4.4.2	With positive response	PASS	PASS	PASS	PASS	PASS	
4.4.3	Conditional change NAD	PASS	PASS	PASS	PASS	PASS	

5 Results of LIN 2.0 master conformance tests

The following tables give the results of the tests performed on STM8AF UART1.

5.1 LIN 2.0 master – LIN OSI layer 2 – data link layer

Table 11. Master test list: LIN OSI layer 2 - data link layer

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
2	**Timing parameters**						
2.1	Length of SYNCH BREAK LOW PHASE	PASS	PASS	PASS	PASS	PASS	
2.3	Length of SYNCH BREAK DELIMITER	PASS	PASS	PASS	PASS	PASS	See (1)
2.5	Length of Header	PASS	PASS	PASS	PASS	PASS	
2.7	Oscillator tolerance	PASS	PASS	PASS	PASS	PASS	
2.10	Length of frame	PASS	PASS	PASS	PASS	PASS	
2.10.2	IUT as Master with a slave task	PASS	PASS	PASS	PASS	PASS	
3	**Communication without failure**						
3.1	Variation of LIN Identifier	PASS	PASS	PASS	PASS	PASS	
3.1.1	IUT as Master	PASS	PASS	PASS	PASS	PASS	
3.1.3	IUT as Master with Slave task	PASS	PASS	PASS	PASS	PASS	
3.2	Transmission of the Checksum Byte	PASS	PASS	PASS	PASS	PASS	
3.2.2	IUT as Master with a slave task	PASS	PASS	PASS	PASS	PASS	

Table 11. Master test list: LIN OSI layer 2 - data link layer (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
3.4	Command Frame ‘Master Request’	PASS	PASS	PASS	PASS	PASS	
3.6	Command Frame ‘Slave Response Frame’	PASS	PASS	PASS	PASS	PASS	

1. For baudrate 10417 and 2400 bps, CANOE software considers this test as failed, and outputs the following messages:
“T[syndel] measured is not in the allowed range [>=420]. T[syndel] measured = 410 (in µs)“ (for 2400 bps);
“T[syndel] measured is not in the allowed range [>=100]. T[syndel] measured = 90 (in µs)“ (for 10417 bps).
However, when measuring with an oscilloscope the duration between two consecutive bits of the synch byte 0x55 of a Master node transmitted frame, we can see that:
- at 2400 bps, duration = 835 µs à the average bit length is 835/2 = 417.5 µs (expected value should be 1/2400 = 416 µs);
- at 10417 bps, duration = 192.2 µs à the average bit length is 192.2/2 = 96.1 µs (expected value should be 1/10417= 95.96 µs).
As a results, despite what CANOE reports, this test is considered as passed.

5.2 LIN 2.0 master – node configuration / network management

Table 12. Master test list: node configuration/network management

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
3	**Sleep / wakeup tests**						
3.1	Send Command Frame ‘Sleep Mode Command’	PASS	PASS	PASS	PASS	PASS	
3.3	Receive a Wake Up request	PASS	PASS	PASS	PASS	PASS	
3.5	Send a Wake up request	PASS	PASS	PASS	PASS	PASS	
3.5.1	IUT as Master with slave task	PASS	PASS	PASS	PASS	PASS	

6 Results of LIN 2.1 slave conformance tests

The following tables give the results of the tests performed on STM8AF LINUART and STM8AL USART.

6.1 LIN 2.1 slave – LIN OSI layer 2 – data link layer

Table 13. LIN 2.1 slave test List: LIN OSI layer 2 – data link layer

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
2	**Essential test cases before test start**						
2.1	Diagnostic frame 'Master Request'	PASS	PASS	PASS	PASS	PASS	
2.2	Command Frame 'Slave Response Frame'	PASS	PASS	PASS	PASS	PASS	
2.3	Error in Received Frame	PASS	PASS	PASS	PASS	PASS	
3	**Timing parameters**						
3.2	Variation of Length of break field low phase	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	
3.4.1	Variation of Length of break delimiter. Sync Break = 13 bit (min), Sync Delimiter = 1 bit (min), Interbyte = 0 bit (min)	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	
3.4.2	Variation of Length of break delimiter. Sync Break = 13 bit (min), Sync Delimiter = 14 bit (max), Interbyte = 0 bit (min)	PASS	PASS	PASS	PASS	PASS	
3.4.3	Variation of Length of break delimiter. Sync Break = 13 bit (min), Sync Delimiter = 10 bit, Interbyte = 0 bit (min)	PASS	PASS	PASS	PASS	PASS	
3.5	Inconsistent break field error	PASS	PASS	PASS	PASS	PASS	
3.6.1	Inconsistent Sync Byte Field error. Sync Byte Field = 0x54	PASS	PASS	PASS	PASS	FAIL	CANOE internal error!

Table 13. LIN 2.1 slave test List: LIN OSI layer 2 – data link layer (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
3.6.2	Inconsistent Sync Byte Field error. Sync Byte Field = 0x5D	PASS	PASS	PASS	PASS	PASS	
3.8.1	Incomplete frame reception. Break field only	PASS	PASS	PASS	PASS	PASS	
3.8.2	Incomplete frame reception. Break and Sync Byte fields only	PASS	PASS	PASS	PASS	PASS	
3.8.3	Incomplete frame reception. Header of Rx-frame only	PASS	PASS	PASS	PASS	PASS	
3.8.4	Incomplete frame reception. Header of Rx-frame with the first data byte only	PASS	PASS	PASS	PASS	PASS	
3.9.1	Unknown frame reception. Header of unknown frame only	PASS	PASS	PASS	PASS	PASS	
3.9.2	Unknown frame reception. Header of unknown frame with the first data byte only	PASS	PASS	PASS	PASS	PASS	
3.9.3	Unknown frame reception. Unknown frame with wrong checksum	PASS	PASS	PASS	PASS	PASS	
3.11.1	Variation of header length. Header = 34 bit; Sync Break = 13 bit (min), Sync Del = 1 bit (min), Interbyte = 0 bit, minimum bit rate	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	
3.11.2	Variation of header length. Header = 47 bit; Sync Break = 19 bit, Sync Del = 2 bit, Interbyte = 6 bit, maximum bit rate	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	
3.11.3	Variation of header length. Header = 40 bit; Sync Break = 15 bit, Sync Del = 3 bit, Interbyte = 2 bit, nominal bit rate	PASS	PASS	PASS	PASS	PASS	
3.11.4	Variation of header length. Header = 47 bit; Sync Break = 13 bit (min), Sync Del = 1 bit (min), Interbyte = 13 bit, maximum bit rate	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	

Table 13. LIN 2.1 slave test List: LIN OSI layer 2 – data link layer (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
3.13.1	Bit rate tolerance, IUT without making use of synchronization. Master deviation from nominal bit rate = + 0.5%	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	
3.13.2	Bit rate tolerance, IUT without making use of synchronization. Master deviation from nominal bit rate = - 0.5%	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	
3.14.1	Bit rate tolerance, IUT with making use of synchronization. Master deviation from nominal bit rate = + 0.5%	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	
3.14.2	Bit rate tolerance, IUT with making use of synchronization. Master deviation from nominal bit rate = - 0.5%	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	
3.15.1	Length of response	PASS	PASS	PASS	PASS	PASS	
3.15.3.1	Acceptance of response field. Response space = 0 bits, each inter-byte space = 0 bits	PASS	PASS	PASS	PASS	PASS	
3.15.3.2	Acceptance of response field. Response space = 4 bits, each inter-byte space = 4 bits	PASS	PASS	PASS	PASS	PASS	
3.15.3.3	Acceptance of response field. Response space = 0 bits, inter-byte space between data bytes 7 and 8 = 36 bits	PASS	PASS	PASS	PASS	PASS	
3.15.3.4	Acceptance of response field. Response space = 36 bits, each inter-byte space = 0 bits	PASS	PASS	PASS	PASS	PASS	
3.17	Sample Point Test	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	
4	**Communication without failure**						
4.1.2	Variation of LIN Identifier of subscribed frames	PASS	PASS	PASS	PASS	PASS	
4.1.3	Variation of LIN Identifier of published frames	PASS	PASS	PASS	PASS	PASS	

Table 13. LIN 2.1 slave test List: LIN OSI layer 2 – data link layer (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
4.2.1	Transmission of the Checksum Byte classic checksum	PASS	PASS	PASS	PASS	PASS	
4.2.2	Transmission of the Checksum Byte enhanced checksum	PASS	PASS	PASS	PASS	PASS	
4.3.2	Unused bits	PASS	PASS	PASS	PASS	PASS	
4.4.1	Reserved Frame	PASS	PASS	PASS	PASS	PASS	
4.4.2	Reserved Frame with error	PASS	PASS	PASS	PASS	PASS	
4.6.1	Supported Tx Frames according to the IUT specification	PASS	PASS	PASS	PASS	PASS	
4.6.2	Supported Rx Frames according to the IUT specification	PASS	PASS	PASS	PASS	PASS	
5	**Communication with failure**						
5.1.1	Bit error. Byte 1, Stop bit	PASS	PASS	PASS	PASS	PASS	
5.1.2	Bit error. Byte 1, Bit 1	PASS	PASS	PASS	PASS	PASS	
5.1.3	Bit error. Interbyte Data 1-2, Bit 1	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 1-2 with Bit 1 inverted – Not Applicable
5.1.4	Bit error. Byte 2, Stop bit	PASS	PASS	PASS	PASS	PASS	
5.1.5	Bit error. Byte 2, Bit 2	PASS	PASS	PASS	PASS	PASS	
5.1.6	Bit error. Interbyte Data 2-3, Bit 1	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 2-3 with Bit 1 inverted – Not Applicable
5.1.7	Bit error. Byte 3, Stop bit	PASS	PASS	PASS	PASS	PASS	
5.1.8	Bit error. Byte 3, Bit 3	PASS	PASS	PASS	PASS	PASS	
5.1.9	Bit error. Interbyte Data 3-4, Bit 1	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 3-4 with Bit 1 inverted – Not Applicable
5.1.10	Bit error. Byte 4, Stop bit	PASS	PASS	PASS	PASS	PASS	

Table 13. LIN 2.1 slave test List: LIN OSI layer 2 – data link layer (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
5.1.11	Bit error. Byte 4, Bit 6	PASS	PASS	PASS	PASS	PASS	
5.1.12	Bit error. Interbyte Data 4-5, Bit 1	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 4-5 with Bit 1 inverted – Not Applicable
5.1.13	Bit error. Byte 5, Stop bit	PASS	PASS	PASS	PASS	PASS	
5.1.14	Bit error. Byte 5, Bit 5	PASS	PASS	PASS	PASS	PASS	
5.1.15	Bit error. Interbyte Data 5-6, Bit 1	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 5-6 with Bit 1 inverted – Not Applicable
5.1.16	Bit error. Byte 6, Stop bit	PASS	PASS	PASS	PASS	PASS	
5.1.17	Bit error. Byte 6, Bit 4	PASS	PASS	PASS	PASS	PASS	
5.1.18	Bit error. Interbyte Data 6-7, Bit 1	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 6-7 with Bit 1 inverted – Not Applicable
5.1.19	Bit error. Byte 7, Stop bit	PASS	PASS	PASS	PASS	PASS	
5.1.20	Bit error. Byte 7, Bit 7	PASS	PASS	PASS	PASS	PASS	
5.1.21	Bit error. Interbyte Data 7-8, Bit 1	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 7-8 with Bit 1 inverted – Not Applicable
5.1.22	Bit error. Byte 8, Stop bit	PASS	PASS	PASS	PASS	PASS	
5.1.23	Bit error. Byte 8, Bit 8	PASS	PASS	PASS	PASS	PASS	
5.1.24	Bit error. Interbyte Data 8-Checksum, Bit 1	N.A.	N.A.	N.A.	N.A.	N.A.	Bit Error - Interbyte Data 8-CS with Bit 1 inverted – Not Applicable
5.1.25	Bit error. Checksum field, Stop bit	PASS	PASS	PASS	PASS	PASS	
5.2	Framing error in header of published frame	PASS	PASS	PASS	PASS	PASS	
5.3	Framing error in response field of subscribed frame	PASS	PASS	PASS	PASS	PASS	
5.4	Checksum error by inversion	PASS	PASS	PASS	PASS	PASS	
5.5	Checksum error by carry	PASS	PASS	PASS	PASS	PASS	

Table 13. LIN 2.1 slave test List: LIN OSI layer 2 – data link layer (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
6	**Event triggered frames**						
6.1	Event Triggered Frame	PASS	PASS	PASS	PASS	PASS	
6.2.1	Event Triggered Frame with collision resolving	PASS	PASS	PASS	PASS	PASS	
6.2.2	Event Triggered Frame with errors in collision resolving	PASS	PASS	PASS	PASS	PASS	
6.4	Error in Transmitted Frame with Collision	PASS	PASS	PASS	PASS	PASS	

6.2 LIN 2.1 slave – node configuration / network management

Table 14. LIN 2.1 slave test list: node configuration / network management

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
7	**Status management**						
7.1	Error in Received frame	PASS	PASS	PASS	PASS	PASS	
7.2.1	Error in Transmitted frame. Inverted checksum	PASS	PASS	PASS	PASS	PASS	
7.2.2	Error in Transmitted frame. Inverted stop bit of Byte 1	PASS	PASS	PASS	PASS	PASS	
7.3	Response error bit handling	PASS	PASS	PASS	PASS	PASS	
8	**Sleep / wakeup tests**						
8.2.1	Receive 'Goto Sleep Command' with data bytes 2 to 8 filled with 0xFF	PASS	PASS	PASS	PASS	PASS	
8.2.2	Receive 'Goto Sleep Command' with data bytes 2 to 8 not filled with 0xFF	PASS	PASS	PASS	PASS	PASS	

Table 14. LIN 2.1 slave test list: node configuration / network management (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
8.4.1	Receive a Wake up signal - 250us	PASS	PASS	PASS	PASS	PASS	
8.4.2	Receive a Wake up signal - 5ms	PASS	PASS	PASS	PASS	PASS	
8.4.3	Receive a Wake up signal - 5 nominal bit times	PASS	PASS	PASS	PASS	PASS	
8.5.1	Send a Wake up signal	PASS	PASS	PASS	PASS	PASS	
8.5.2	Send a block of wake up signals	PASS	PASS	PASS	PASS	PASS	For 2400 bps only, LIN_WAKEUP_TIMEOUT_VAL_SHORT is set to 153, instead of 150.
8.5.3	Wait after one block of wakeup signals	PASS	PASS	PASS	PASS	PASS	
8.5.4	Send a Wake up signal, Frame header from a Master following	PASS	PASS	PASS	PASS	PASS	
8.6.1.1	Sleep Mode after Bus Idle, recessive level after Slave Response	PASS	PASS	PASS	PASS	PASS	
8.6.1.2	Sleep Mode after Bus Idle, recessive level after wake up	PASS	PASS	PASS	PASS	PASS	
8.6.1.3	Sleep Mode after Bus Idle, dominant level after wake up	PASS	PASS	PASS	PASS	PASS	
8.6.1.4	Sleep Mode after Bus Idle, recessive level after Break and Sync fields	PASS	PASS	PASS	PASS	PASS	
8.6.1.5	Sleep Mode after Bus Idle, dominant level after Break and Sync fields	PASS	PASS	PASS	PASS	PASS	
8.6.1.6	Sleep Mode after Bus Idle, recessive level after response error in master request	PASS	PASS	PASS	PASS	PASS	
8.6.1.7	Sleep Mode after Bus Idle, dominant level after response error in master request	PASS	PASS	PASS	PASS	PASS	
8.6.2	Sleep Mode after Bus Idle, recessive level after power up wake up	PASS	PASS	PASS	PASS	PASS	
8.7	Timeout after Bus Idle	PASS	PASS	PASS	PASS	PASS	

Table 14. LIN 2.1 slave test list: node configuration / network management (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
9	**Node configuration**						
9.1.1	Frame ID range assignment with indirect response	PASS	PASS	PASS	PASS	PASS	
9.1.2	Frame ID range unassignment with indirect response	PASS	PASS	PASS	PASS	PASS	
9.2.1	LIN Product ID with direct response	PASS	PASS	PASS	PASS	PASS	
9.2.2	LIN Product ID with delayed response	PASS	PASS	PASS	PASS	PASS	
10	**Wildcards**						
10.1.1	Request with NAD as wildcard	PASS	PASS	PASS	PASS	PASS	
10.1.2	Request with Supplier ID as wildcard	PASS	PASS	PASS	PASS	PASS	
10.1.3	Request with Function ID as wildcard	PASS	PASS	PASS	PASS	PASS	
10.1.4	Request with Supplier ID and Function ID as wildcard	PASS	PASS	PASS	PASS	PASS	
11	**Read by identifier command**						
11.1	Correct addressing. All Identifiers	PASS	PASS	PASS	PASS	PASS	
11.2.1	Incorrect addressing; Incorrect NAD	PASS	PASS	PASS	PASS	PASS	
11.2.2	Incorrect addressing; Incorrect Supplier ID MSB	PASS	PASS	PASS	PASS	PASS	
11.2.3	Incorrect addressing; Incorrect Supplier ID LSB	PASS	PASS	PASS	PASS	PASS	
11.2.4	Incorrect addressing; Incorrect Function ID MSB	PASS	PASS	PASS	PASS	PASS	
11.2.5	Incorrect addressing; Incorrect Function ID LSB	PASS	PASS	PASS	PASS	PASS	
12	**NAD assignment**						
12.1	NAD Assignment - followed by Read by Identifier command	PASS	PASS	PASS	PASS	PASS	
12.2	NAD Assignment - with positive response	PASS	PASS	PASS	PASS	PASS	

Table 14. LIN 2.1 slave test list: node configuration / network management (continued)

TC ref.	Name	Baudrate / Test status					Comment
		20000	19200	10417	9600	2400	
12.3	Conditional change NAD	PASS	PASS	PASS	PASS	PASS	
13	**Transport layer**						
13.1	Transport layer Functional Request	PASS	PASS	PASS	PASS	PASS	
13.2.1	Aborting diagnostic communication with new diagnostic request	PASS	PASS	PASS	PASS	PASS	
13.2.2	Aborting diagnostic communication with corrupted diagnostic request	PASS	PASS	PASS	PASS	PASS	
13.3	Receiving segmented request as specified	PASS	PASS	PASS	PASS	PASS	
13.4.1	Receiving segmented request if user frames between request parts	PASS	PASS	PASS	PASS	PASS	
13.4.2	Receiving segmented request with functional request between request parts	PASS	PASS	PASS	PASS	PASS	
13.5.1	Ignoring segmented requests after timeout	PASS	PASS	PASS	PASS	PASS	
13.5.2	Observing Transport Layer timeout	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	NOT TESTED	
13.6	Ignoring segmented requests with wrong sequence numbering	PASS	PASS	PASS	PASS	PASS	
13.7	Responding with correct segmented response	PASS	PASS	PASS	PASS	PASS	
13.8.1	Sending segmented response with user frames between response parts	PASS	PASS	PASS	PASS	PASS	
13.8.2	Sending segmented response with functional request between response parts	PASS	PASS	PASS	PASS	PASS	
13.9	Not responding to 0x3D if there is no request before	PASS	PASS	PASS	PASS	PASS	
13.10	Not responding to 0x3D if the response is already sent	PASS	PASS	PASS	PASS	PASS	
13.11	Aborting segmented response after timeout	PASS	PASS	PASS	PASS	PASS	

7 Revision history

Table 15. Document revision history

Date	Revision	Changes
03-Dec-2012	1	Initial release.
23-Jul-2013	2	Updated *Section : Introduction*. Updated *Section 1: Hardware requirements*, including *Figure 1*, *Figure 2*, *Table 3*, *Table 4* and *Table 7* titles. Added *Figure 3* and *Figure 4*. Updated *Table 8: Software environment*. Added 3rd paragraph in *Section 3: Tested configurations* Updated some part numbers in *Section 3: Tested configurations* Updated *Section 4: Results of LIN 2.0 slave conformance tests* introduction. Updated *Section 5: Results of LIN 2.0 master conformance tests* introduction. Updated *Section 6: Results of LIN 2.1 slave conformance tests* introduction.