TN1286
Technical note

SPC58NG84C3GXC0X documentation addendum

Introduction

The SPC58NG84C3GXCOX is a custom device with an extended version of the SPC58NG84C3GECOX family provided by ST for the Continental Project VW ICAS.

This custom device offers the additional features as described in this document.

All technical aspects related to the additional features and described in the documents listed in *Reference documents*, must be considered.

Contents

1 Serial communication configuration (Standard option)

The configuration includes 8x ISO CAN FD, FlexRay and Ethernet 0.

2 Additional RAM (135 Kbyte)

In addition to the System RAM and Local RAM available on the SPC58xGx device (total of 768 Kbyte) this custom device features additional peripheral RAM which can be used by the application for data storage. It should be considered that the access time to these peripheral RAM blocks is slower and must be evaluated by the customer if it matches its application's needs.

2.1 71 K (Timer RAM)

Following are the address spaces of the required RAM.

Table 1. Timer RAM memory allocation

Ram Partition	Start Address	End Address	N. of words	Data width
timer_fifo	0xF7D1_9000	0xF7D1_9FFF	1024	29
timer_ram0_0	0xF7D3_8000	0xF7D3_9FFF	2048	32
timer_ram0_1	0xF7D4_0000	0xF7D4_1FFF	2048	32
timer_ram0_2	0xF7D4_8000	0xF7D4_9FFF	2048	32
timer_ram0_3	0xF7D5_0000	0xF7D5_1FFF	2048	32
timer_ram0_4	0xF7D5_8000	0xF7D5_9FFF	2048	32
timer_ram1_0	0xF7D3_A000	0xF7D3_AFFF	1024	32
timer_ram1_1	0xF7D4_2000	0xF7D4_2FFF	1024	32
timer_ram1_2	0xF7D4_A000	0xF7D4_AFFF	1024	32
timer_ram1_3	0xF7D5_2000	0xF7D5_2FFF	1024	32
timer_ram1_4	0xF7D5_A000	0xF7D5_AFFF	1024	32
timer_dpll_ram1a	0xF7D2_8200	0xF7D2_83FF	96	24
timer_dpll_ram1b	0xF7D2_8400	0xF7D2_8BFF	384	24
timer_dpll_ram2	0xF7D2_C000	0xF7D2_DFFF	2048	24

AC0_DC0 clock divisor register is needed for enabling the Timer Ram (it will allow the Timer to be on, which RAM is part of)

Note: Access time to the timer RAM is slower as to the SRAM and depends on the clock and application configuration. Therefore if access time is critical an evaluation with the application specific SW should performed to ensure it meets application's performance requirements.

The additional dynamic consumption caused by the Timer RAM must be considered in the application.

2.2 32 K (AMU RAM)

AMU RAM is located in two different chunks of memory (PBRIDGE2):

AMU_LMEM1: 0xF40C0000 – 0xF40C3FFF

AMU_LMEM2: 0xF40C4000 – 0xF40C7FFF

In case those address spaces are not yet initialized, user can enable them by writing zero (from debugger for example)

Note: Access time to the AMU RAM is slower as to the SRAM and depends on the clock and application configuration. Therefore if access time is critical an evaluation with the application specific SW should performed to ensure it meets application's performance requirements.

The additional dynamic consumption caused by the AMU RAM must be considered in the application.

2.3 32 K (Overlay RAM)

Two chunks of Overlay RAM are available in PFLASH_0 and PFLASH_1 area.

Overlay RAM0: 0x0D000000 – 0x0D003FFF

Overlay RAM1: 0x0D004000 – 0X0D007FFF

Overlay RAM can be enable by initializing the address space to zero (from debugger for example)

Note: Access time to the Overlay RAM is slower as to the SRAM and depends on the clock and application configuration. Therefore if access time is critical an evaluation with the application specific SW should performed to ensure it meets application's performance requirements.

The additional dynamic consumption caused by the Overlay RAM must be considered in the application.

Appendix A Reference documents

Table 2. Reference documents

Doc name	ID	Title	Revision
RM0391	027214	32-bit Power Architecture® microcontroller for automotive ASILD applications	3
DS11646	029333	32-bit Power Architecture® microcontroller for automotive ASIL-D applications	3
ES0397	030696	SPC58xEx device errata JTAG_ID = 0x1111_0041	2
AN4845	029112	SPC58xEx Safety Manual	4
AN4827	028960	Failure Modes Effects and Diagnostic Analysis for SPC58NE84x	3

Revision history

Table 3. Document revision history

Date	Revision	Changes
18-Feb-2019	1	Initial release.