Introduction

The STM32G081B-EVAL Evaluation board is a high-end development platform for Arm® Cortex®-M0+ core-based STM32G081RBT6 microcontroller with USB Type-C™ and Power Delivery controller interfaces (UCPD) compliant with USB Type-C r1.2 and USB PD specification r3.0, two I2Cs, two SPIs, five USARTs, one LP UART, one 12-bit ADC, two 12-bit DACs, two GP comparators, two LP timers, internal 32KB SRAM and 128KB Flash, CEC, SWD debugging support.

The full range of hardware features on the STM32G081B-EVAL Evaluation board includes the mother board, the legacy peripheral daughterboard and the USB Type-C and Power Delivery daughterboard, which help to evaluate all peripherals (USB Type-C connector with USB PD, motor control connector, RS232, RS485, Audio DAC, microphone ADC, TFT LCD, IrDA, IR LED, IR receiver, LDR, microSD™ card, CEC on two HDMI connectors, smartcard slot, RF E2PROM and temperature sensor… etc.) and to develop applications. An ST-LINK/V2-1 is integrated on the board as embedded in-circuit debugger and programmer for the STM32 MCU.

The daughterboard and extension connectors provide an easy way to connect a daughterboard or wrapping board for your specific application.

The USB Type-C and Power Delivery daughterboard features two independent USB-C ports controlled by STM32G0. USB-C port 1 is dual role power (DRP) and can provide up-to 45W of power. USB-C Port 2 is sink only. Both supports USB PD protocol and alternate mode functionality.

![Figure 1. STM32G081B-EVAL board with legacy peripheral daughterboard](image1)

![Figure 2. STM32G081B-EVAL board with UCPD daughterboard](image2)

Pictures are not contractual.
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1 Features

Mother board

- STM32G081RBT6 Arm®(a) Cortex®-M0+ core-based microcontroller with 128 Kbytes of Flash memory and 32 Kbytes of RAM in LQFP64 package
- MCU voltage choice fixed 3.3 V or adjustable from 1.65 V to 3.6 V
- I²C compatible serial interface
- RTC with backup battery
- 8-Gbyte or more SPI interface microSD™ card
- Potentiometer
- 4 color user LEDs and one LED as MCU low-power alarm
- Reset, Tamper and User buttons
- 4-direction control and selection joystick

Board connectors:
- 5 V power jack
- RS-232 and RS485 communications
- Stereo audio jack including analog microphone input
- microSD™ card
- Extension I²C connector
- Motor-control connector

Board extension connectors:
- Daughterboard connectors for legacy peripheral daughterboard or USB Type-C and Power Delivery daughterboard
- Extension connectors for daughterboard or wire-wrap board

Flexible power-supply options:
- 5 V power jack
- ST-LINK/V2-1 USB connector
- Daughterboard

On-board ST-LINK/V2-1 debugger/programmer with USB enumeration capability: mass storage, virtual COM port and debug port

Comprehensive free software libraries and examples available with the STM32Cube package

Support of a wide choice of Integrated Development Environments (IDEs) including IAR™, Keil®, GCC-based IDEs.

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(a) Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
Legacy peripheral daughterboard
- IrDA transceiver
- IR LED and IR receiver
- Light dependent resistor (LDR)
- Temperature Sensor
- Board connectors:
  - Two HDMI connectors with DDC and CEC
  - Smartcard slot

USB Type-C and Power Delivery daughterboard
- Multiplexer for USB3.1 Gen1 / DisplayPort™ input and Type-C port1 output
- Multiplexer for Type-C port2 input and DisplayPort output / USB2.0
- VCONN on Type-C port1
- USB PD on Type-C port1
- Board connectors:
  - Type-C port1 DRP (Dual Role Port)
  - Type-C port2 sink
  - DisplayPort input
  - DisplayPort output
  - USB 3.1 Gen1 Type-B receptacle
  - USB2.0 Type-A receptacle
  - 19 V power jack for USB PD
2 Product marking

Evaluation tools marked as “ES” or “E” are not yet qualified and are therefore not ready to be used as reference design or in production. Any consequences arising from such usage will not be at STMicroelectronics’ charge. In no event will STMicroelectronics be liable for any customer usage of these engineering sample tools as reference designs or in production.

‘E’ or ‘ES’ marking examples of location:

- on the targeted STM32 that is soldered on the board (for illustration of STM32 marking, refer to the section Package information in the STM32 datasheet at www.st.com).
- next to the evaluation tool ordering part number, that is stuck or silkscreen printed on the board.

3 System requirements

- Windows® OS (7, 8 and 10), Linux® 64-bit or macOS®(a)
- USB Type-A to Micro-B cable

4 Development toolchains

- Keil® MDK-ARM(b)
- IAR™ EWARM(b)
- GCC-based IDEs

5 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board MCU, is preloaded in the STM32 Flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from the www.st.com web page.

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a. macOS® is a trademark of Apple Inc., registered in the U.S. and other countries.

b. On Windows only
6 Ordering information

To order the STM32G081B-EVAL Evaluation board, refer to Table 1.

Table 1. Ordering information

<table>
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<th>Order code</th>
<th>Target STM32</th>
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<tr>
<td>STM32G081B-EVAL</td>
<td>STM32G081RB</td>
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7 Delivery recommendations

Some verifications are needed before using the board for the first time, to make sure that no damage occurred during shipment and that no components are unplugged or lost.

When the board is extracted from its plastic bag, check that no component remains in the bag. The main component to verify is microSD card which may have been ejected from the connector CN8 (right side of the board).

Caution: There is an explosion risk if the battery is replaced by an incorrect one. Make sure to dispose of used batteries according to the instructions.
8 Hardware layout and configuration

The STM32G081B-EVAL Evaluation board is designed around the STM32G081RBT6 (64-pin LQFP package). The hardware block diagram Figure 3 illustrates the connection between STM32G081RBT6 and peripherals (motor control connector, RS232, RS485, Audio DAC, microphone ADC, TFT LCD, CAN, IrDA, IR LED, IR receiver, LDR, MicroSD card, CEC on two HDMI connectors, Smartcard slot, Temperature sensor… etc.) and Figure 4 help users to locate these features on the Evaluation board.

Figure 3. Hardware block diagram
Figure 4. STM32G081B-EVAL Evaluation board layout
Figure 5. Legacy peripheral daughterboard

Figure 6. USB Type-C and Power Delivery daughterboard
8.1 Embedded ST-LINK/V2-1

The ST-LINK/V2-1 programming and debugging tool is integrated on the STM32G081B-EVAL Evaluation board. Compared to ST-LINK/V2 the changes are listed below.

The new features supported on ST-LINK/V2-1 are:

- USB software enumeration
- Virtual COM port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100 mA power on USB

This feature is no longer supported on ST-LINK/V2-1:

- SWIM interface

For all general information concerning debugging and programming features common between V2 and V2-1 refer to ST-LINK/V2 in-circuit debugger/programmer for STM8 and STM32 User manual (UM1075) in the www.st.com website.

Note: It is possible to power the board via CN6 (Embedded ST-LINK/V2-1 USB connector) even if an external tools is connected to CN12 or CN13 (External SWD connector).

8.1.1 Drivers

The ST-LINK/V2-1 requires a dedicated USB driver, which can be found on www.st.com for Windows PC (7, 8 or 10).

In case the STM32G081B-EVAL Evaluation board is connected to the PC before the driver is installed, some STM32G081B-EVAL interfaces may be declared as “Unknown” in the PC device manager. In this case, the user must install the driver files, and update the driver of the connected device from the device manager.

Note: Prefer using the “USB Composite Device” handle for a full recovery.

![Figure 7. USB Composite Device](image)

8.1.2 ST-LINK/V2-1 firmware upgrade

The ST-LINK/V2-1 embeds a firmware upgrade mechanism for in-situ upgrade through the USB port. As the firmware may evolve during the lifetime of the ST-LINK/V2-1 product (for example new functionality, bug fixes, support for new microcontroller families), it is recommended to visit the www.st.com website before starting to use the STM32G081B-EVAL board and periodically, to stay up-to-date with the latest firmware version.
8.2 Power supply

The STM32G081B-EVAL Evaluation mother board is designed to be powered by 5 V DC power supply and is protected by PolyZen from wrong power plug-in event. It is possible to configure the mother board to use any of the following four sources for the power supply:

- 5 V DC power adapter connected to CN16, the power Jack on the board (Power Supply Unit on silk screen of JP17 (PSU)). The external power supply is not provided with the board.
- 5 V DC power with 500 mA limitation from CN6, the USB Micro-B connector of STLINK/V2-1 (USB 5 V power source on silkscreen of JP17 (STlk)). If the USB enumeration succeeds, the ST-LINK U5V power is enabled, by asserting the PWR_EN pin. This pin is connected to a power switch, which powers the board. This power switch features also a current limitation to protect the PC in case of short-circuit on the board. If overcurrent (more than 500 mA) happens on the board, the LED LD5 lights up.
- 5 V DC power from CN6 directly, the USB Micro-B connector of STLINK/V2-1 (USB 5 V power source on silkscreen of JP17 (USV)).
- 5 V DC power from CN5 or CN9, the extension connector for daughterboard power source (D5V) on silkscreen of JP19).

The UCPD daughterboard uses its own 19 V power adapter to support USB PD, in this case the mother board uses D5V from the UCPD daughterboard to supply all circuits on STM32G081B-EVAL Evaluation board. D5V of the UCPD daughterboard has three sources as below:

- 19 V DC power adapter connected to CN3 on the UCPD daughterboard
- Power from Type-C Port1 CN7 on the UCPD daughterboard
- Power from Type-C port2 CN5 on the UCPD daughterboard

19 V DC power adapter and Type-C Port1 sources are automatically selected by circuit (D8 and T10 on the UCPD daughterboard). Refer to Table15 for detail.
The STM32G081B-EVAL Evaluation board can be powered from the ST-LINK/V2-1 USB connector CN6 with a PC, but only the ST-LINK/V2-1 circuit has the power before USB enumeration, because the host PC only provides 100 mA to the boards at that time. During the USB enumeration, the STM32G081B-EVAL board requires 300 mA power from the host PC. If the host is able to provide the required power, the enumeration succeeds, the power transistor U5 is switched ON, the red LED LD7 is turned ON, and thus the STM32G081B-EVAL board is powered and can consume maximum 300 mA current. If the host PC is not able to provide the requested current, the enumeration fails. Therefore the STM32 part including the extension board is not powered. As a consequence the red LED LD7 remains turned OFF. In this case it is mandatory to use an external power supply to supply extra power.

E5V (from PSU) or D5V can be used as external power supply in case current consumption of the STM32G081B-EVAL board exceeds the allowed current on USB. In this condition it is still possible to use USB for communication, for programming or debugging only, but it is mandatory to power the board first using E5V or D5V, and then connecting the USB cable to the PC. Proceeding this way ensures that the enumeration succeeds thanks to the external power source.

The following power sequence procedure must be respected:
1. Connect jumper JP17 for PSU or D5V side
2. Check that JP5 is removed
3. Connect the external power source to PSU or D5V (daughterboard mounted)
4. Check red LED LD7 is turned ON
5. Connect the PC to USB connector CN6

If this order is not respected, the board may be powered by VBUS first then E5V or D5V, and the following risks may be encountered:

1. If more than 300 mA current is needed by the board, the PC may be damaged or current can be limited by PC. As a consequence the board is not powered correctly.
2. 300 mA is requested at enumeration (since JP5 must be OFF), so there is risk that request is rejected and enumeration does not succeed if PC can't provide such current. Consequently the board is not powered (LED LD7 remains OFF).

In case the STM32G081B-EVAL board is powered by an USB charger through CN6, there is no USB enumeration needed. User can set JP17 to U5V to allow the board to be powered anyway from CN6.

The power source is selected by setting the related jumpers JP17, JP15 and JP16 as described in table 2.

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
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</table>
| JP17   | JP17 is used to select one of the four possible power supply resources. Only for power supply from USB (CN6) of ST-LINK/V2-1 to STM32G081B-EVAL, JP17 is set as shown on the right:  
|        | ![JP17 Setting](image) |
|        | Only for power supply from the **daughterboard connectors**(CN5 or CN9) to STM32G081B-EVAL, JP17 is set as shown on the right: (default Setting) |
|        | ![JP17 Setting](image) |
|        | Only for **power supply jack**(CN16) to the STM32G081B-EVAL, JP17 is set as shown on the right: |
|        | ![JP17 Setting](image) |
|        | Only for power supply from USB (CN6) to STM32G081B-EVAL without current limited, JP17 is set as shown on the right: |
|        | ![JP17 Setting](image) |
Table 2. Power source related Jumpers (continued)

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<th>Jumper</th>
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<tbody>
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<td>The Vbat pin of STM32G081RBT6 is connected to VDD when JP15 is set as shown on the right (default setting):</td>
</tr>
<tr>
<td></td>
<td>The Vbat pin of STM32G081RBT6 is connected to 3V battery when JP15 is set as shown on the right:</td>
</tr>
<tr>
<td>JP16</td>
<td>The VDD pin of STM32G081RBT6 is connected to 3.3V when JP16 is set as shown on the right (default setting), when the UCPD daughterboard is used, this setting is mandatory:</td>
</tr>
<tr>
<td></td>
<td>The VDD pin of STM32G081RBT6 is connected to VDD_ADJ when JP16 is set as shown on the right:</td>
</tr>
</tbody>
</table>

Note: The VDD_MCU Idd measurement can be done by current meter which mounted on JP11 when it is open. But JP11 is not allowed to be opened without current meter; otherwise STM32G081RBT6 would be damaged due to lacking of power supply on its power pins.

Note: LD8 is lit when VDD < 2.7 V and in this case IOs and some Analog IPs of STM32G081RBT6 work with degraded performances.

Note: The UCPD daughterboard works with VDD=3.3V, so it is mandatory to close JP16 pin1 and pin2.

The LED LD7 is lit when the STM32G081B-EVAL Evaluation board is powered by the 5V correctly.

Table 3 shows the low voltage limitations that might apply depending on the characteristics of some peripheral components. Components might work incorrectly when the power level is lower than the limitation.

Table 3. Low voltage limitation

<table>
<thead>
<tr>
<th>Board</th>
<th>peripheral</th>
<th>component</th>
<th>IO name</th>
<th>Low voltage limitation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mother board</td>
<td>Audio amplifier</td>
<td>U17</td>
<td>Audio input</td>
<td>2.2V</td>
</tr>
<tr>
<td>Mother board</td>
<td>Microphone amplifier</td>
<td>U12</td>
<td>Audio output</td>
<td>2.7V</td>
</tr>
<tr>
<td>Legacy daughterboard</td>
<td>Smartcard</td>
<td>CN2</td>
<td>USART1</td>
<td>2.7V</td>
</tr>
</tbody>
</table>
8.3 Clock references

Two clock sources are available on STM32G081B-EVAL Evaluation board for STM32G081RBT6 and RTC embedded.

- X2, 32KHz Crystal for embedded RTC
- X3, 8MHz Crystal for the STM32G081RBT6 microcontroller, it can be disconnected by removing R45 and R46 when internal RC clock is used

**Table 4. 32 KHz crystal X2 related solder bridges**

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB18</td>
<td>PC14 is connected to 32KHz crystal when SB18 is open (default setting).</td>
</tr>
<tr>
<td></td>
<td>PC14 is connected to extension connector CN9 when SB18 is closed. In such case R43 must be removed to avoid disturbance due to the 32Khz quartz.</td>
</tr>
<tr>
<td>SB19</td>
<td>PC15 is connected to 32KHz crystal when SB19 is open (default setting).</td>
</tr>
<tr>
<td></td>
<td>PC15 is connected to extension connector CN9 when SB19 is closed. In such case R44 must be removed to avoid disturbance due to the 32Khz quartz.</td>
</tr>
</tbody>
</table>

**Table 5. 8 MHz crystal X3 related solder bridges**

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB20</td>
<td>PF0 is connected to 8MHz crystal when SB20 is open (default setting).</td>
</tr>
<tr>
<td></td>
<td>PF0 is connected to extension connector CN10 when SB20 is closed. In such case R45 must be removed to avoid disturbance due to the 8Mhz quartz.</td>
</tr>
<tr>
<td>SB21</td>
<td>PF1 is connected to 8MHz crystal when SB21 is open (default setting).</td>
</tr>
<tr>
<td></td>
<td>PF1 is connected to extension connector CN10 when SB21 is closed. In such case R46 must be removed to avoid disturbance due to the 8Mhz quartz.</td>
</tr>
</tbody>
</table>

8.4 Reset source

The general reset of the STM32G081B-EVAL Evaluation board is active low and the reset sources include:

- Reset button B1
- Debugging Tools from SWD connector CN12 and CN13
- Daughterboard from CN4
- Embedded ST-LINK/V2-1
- RS232 connector CN11 for ISP.

**Note:** The jumper JP12 to be closed for RESET handled by pin8 of RS232 connector CN11 (CTS signal), please refer to Section 8.6.2 for detail.
8.5 **Boot Option**

The STM32G081B-EVAL Evaluation board is able to boot from:
- Embedded User Flash
- System memory with boot loader for ISP
- Embedded SRAM for debugging

The boot option is configured by closing JP9 pin2-3 and setting one jumper cap on CN10 among pin 17, pin 19 and pin 21 and one option bit (see Table 6 and Table 7).

<table>
<thead>
<tr>
<th>Jumper configuration</th>
<th>Bit25 in USER OPTION BYTES</th>
<th>Boot from</th>
</tr>
</thead>
<tbody>
<tr>
<td>CN10 pin 19 and pin 17 closed by jumper</td>
<td>X</td>
<td>STM32G081B-EVAL boot from <strong>User Flash</strong> (default setting)</td>
</tr>
<tr>
<td>CN10 pin 19 and pin 21 closed by jumper</td>
<td>0</td>
<td>STM32G081B-EVAL boot from <strong>Embedded SRAM</strong></td>
</tr>
<tr>
<td>CN10 pin 19 and pin 21 closed by jumper</td>
<td>1</td>
<td>STM32G081B-EVAL boot from <strong>System Memory</strong></td>
</tr>
</tbody>
</table>

**Table 6. Boot related jumper**

**Table 7. Boot0 related jumpers**

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP9</td>
<td>PA14-BOOT0 is used as SWCLK when JP9 is set as shown on the right (default setting). The Bootloader_BOOT0 is managed by pin 6 of connector CN11 (RS232 DSR signal) and it is connected to PA14-BOOT0 when JP9 is set as shown on the right. This configuration is used for boot loader application only.</td>
</tr>
</tbody>
</table>

8.6 **Peripherals on mother board**

8.6.1 **Audio**

The STM32G081B-EVAL Evaluation board supports stereo audio playback and microphone recording by an external headset connected on audio jack CN15. Audio play is connected to DAC output of STM32G081RBT6 through an audio amplifier and microphone on headset is connected to ADC input of STM32G081RBT6 through a microphone amplifier. Audio amplifier can be enabled or disabled by setting of JP18 and mono/stereo playback can be chosen by setting of JP6, refer to Table 8 for detail.
Audio amplifier operates correctly when VDD > 2.2 V and microphone amplifier operates correctly when VDD > 2.7 V.

### 8.6.2 RS232 and RS485

Communication through RS232 (with Hardware flow control CTS and RTS) and RS485 is supported by D-type 9-pins RS232/RS485 connector CN11, which is connected to USART1 of STM32G081RBT6 on STM32G081B-EVAL Evaluation board. The signal Bootloader_RESET (shared with CTS signal) and Bootloader_BOOT0 (shared with DSR signal) are added on RS232 connector CN11 for ISP support.

By default, PC4 and PC5 are connected as TX and RX signals. PA9 and PA10 are also can be connected as these two signals for bootloader which is NOT supported on PC4 and PC5 by setting of jumpers in Table 9.

#### Table 8. Audio related jumpers

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
</table>
| JP18   | Speaker amplifier U17 is enabled when JP18 is closed (default setting)  
        | Speaker amplifier U17 is disabled when JP18 is open                    |
| JP19   | PA4 is connected to VIN1 of Audio amplifier when JP19 is closed (default setting)  
        | PA4 is disconnected to VIN1 of Audio amplifier when JP19 is open       |
| JP6    | Mono playback is enabled when JP6 is set as shown on the right (default setting): ![Mono](image1)  
        | Stereo playback is enabled when JP6 is set as shown on the right: ![Stereo](image2) |

Audio amplifier operates correctly when VDD > 2.2 V and microphone amplifier operates correctly when VDD > 2.7 V.

#### Table 9. RS232 and RS485 related jumpers

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
</table>
| JP14   | RS232_RX is connected to RS232 transceiver and RS232 communication is enabled when JP14 is set as shown on the right (default setting): ![RS232](image3)  
        | RS485_RX is connected to RS485 transceiver and RS485 communication is enabled when JP14 is set as shown on the right: ![RS485](image4) |
| JP10   | PC4 is connected as TX signal **without** bootloader being supported when JP10 is set as shown on the right (Default setting): ![PC4](image5)  
        | PA9 is connected as TX signal **with** bootloader being supported when JP10 is set as shown on the right (CN1 motor control connector is needed to be open in this case): ![PA9](image6) |
The RS485 communication is supported by RS485 transceiver ST3485EBDR which connected to pin4 and pin9 of D-type 9-pins connector CN11 (share same connector with USART1).

Table 9. RS232 and RS485 related jumpers (continued)

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP8</td>
<td>PC5 is connected as RX signal without bootloader being supported when JP8 is set as shown on the right (default setting):</td>
</tr>
<tr>
<td></td>
<td>PA10 is connected as RX signal with bootloader being supported when JP8 is set as shown on the right (in this case, CN1 motor control connector must be open):</td>
</tr>
</tbody>
</table>

The RS485 communication is supported by RS485 transceiver ST3485EBDR which connected to pin4 and pin9 of D-type 9-pins connector CN11 (share same connector with USART1).

Table 10. RS485 related solder bridges

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB29,SB31</td>
<td>The external failsafe biasing are enabled when solder bridges SB29 and SB31 was closed. Default Setting: Not fitted</td>
</tr>
<tr>
<td>SB32</td>
<td>The bus termination is enabled when solder bridge SB32 is closed. Default Setting: Not fitted</td>
</tr>
<tr>
<td>SB30</td>
<td>The AC termination is disabled when solder bridge SB30 is closed for high baud rate communication. Default Setting: Not fitted</td>
</tr>
</tbody>
</table>

8.6.3 **microSD card**

The 8-GB (or more) microSD card connected to SPI1 port (shared with color LCD) of STM32G081RBT6 is available on the board. microSD card detection is managed by standard IO port PC9 and it must be set with internal pull-up.

8.6.4 **Analog Input**

The two-pin header CN17 and 10K ohm potentiometer RV3 was connected to PB2 of STM32G081RBT6 as analog input. A low pass filter can be implemented by replacing of R111 and C90 with right value of resistor and capacitor as requested by end user's application.

8.6.5 **External I2C Connector**

The I2C1 bus of the STM32G081RBT6 is connected to CN2 on the STM32G081B-EVAL. The I2C functional daughterboard can be mounted on the CN2 connector and accessed by the microcontroller through the I2C1 bus, it shares same I2C1 bus with Temperature sensor U3 and DDC on HDMI_Source connector CN3 on legacy peripheral daughterboard.

The pull up voltage level of I2C1 bus is automatically decided by the daughterboard (the legacy peripheral daughterboard or the UCPD daughterboard) on CN4 and CN5. If there is
no daughterboard on these connector, pin17 must be closed to pin18 on both CN4 and CN5 by jumpers. Thus I2C pull up voltage and reset pull up voltage on CN2 would be the voltage of VDD.

8.6.6 Motor Control

The STM32G081B-EVAL Evaluation board supports both asynchronous and synchronous three-phase brushless motor control via a 34-pins connector CN1, which provides all required control and feedback signals to and from motor power-driving board.

Available signals on this connector includes emergency stop, motor speed, 3 phase motor current, bus voltage, power heatsink coming from the motor driving board and 6 channels of PWM control signal going to the motor driving circuit.

Daughterboard on CN4 and CN5 must be removed and some jumpers set for motor control application:

8.6.7 Display and Input devices

The 2.4” color TFT LCD connected to SPI1 port of STM32G081RBT6 and 4 general purpose color LED's (LD 1,2,3,4) are available as display device. The 4-direction joystick (B3) with selection key which connected to PA0 and supports wakeup feature. Tamper button (B2) are also available as input devices.

Table 11. LCD modules

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Pin connection</th>
<th>Pin</th>
<th>Description</th>
<th>Pin connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CS</td>
<td>PB8</td>
<td>9</td>
<td>VDD</td>
<td>3.3V</td>
</tr>
<tr>
<td>2</td>
<td>SCL</td>
<td>PB3</td>
<td>10</td>
<td>VCI</td>
<td>3.3V</td>
</tr>
<tr>
<td>3</td>
<td>SDI</td>
<td>PA7</td>
<td>11</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>RS</td>
<td></td>
<td>12</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>WR</td>
<td></td>
<td>13</td>
<td>BL_VDD</td>
<td>5V</td>
</tr>
<tr>
<td>6</td>
<td>RD</td>
<td></td>
<td>14</td>
<td>BL_Control</td>
<td>5V</td>
</tr>
<tr>
<td>7</td>
<td>SDO</td>
<td>PB4</td>
<td>15</td>
<td>BL_GND</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>RESET</td>
<td>RESET#</td>
<td>16</td>
<td>BL_GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

Note: The bi-directional voltage translator is implemented on SPI MOSI signal between STM32G081RBT6 and LCD to support 3-wires serial interface of LCD panel only supports 3-wire SPI port. The direction of this voltage translator is controlled by IO PC12 (the IO PA7 is working as MOSI when PC12 is high or as MISO when PC12 is LOW).
8.7 Peripherals on legacy peripheral daughterboard

8.7.1 LDR (Light dependent resistor)

The VDD is divided by resistor bridge of LDR VT9ON1 and 8.2 K resistor and connected to PA1 (COM1_IN+/ADC IN1) as shown Figure 9 on STM32G081B-EVAL Evaluation board.

![Figure 9. GP comparator 1](image)

It's possible to compare LDR output with ¼ band gap, 1/2 band gap, 3/4 band gap, band gap and DAC1 OUT and to connect LDR output to ADC IN1 for AD conversion.

8.7.2 Temperature sensor

A temperature sensor STLM75M2F is connected to the I2C1 bus of the STM32G081RBT6, and shares same I2C1 bus with EXT I2C connector (on mother board) and DDC on HDMI_Source connector CN3 (on legacy board).

I2C address of temperature sensor is 0b100100(A0), A0 can be 0 or 1 depends on the setting of SB7.

Table 12. Temperature sensor related solder bridge

<table>
<thead>
<tr>
<th>Solder Bridge</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB7</td>
<td>I2C address A0 is 0 when SB7 is open.</td>
</tr>
<tr>
<td></td>
<td>(Default setting)</td>
</tr>
<tr>
<td></td>
<td>I2C address A0 is 1 when SB7 is closed.</td>
</tr>
</tbody>
</table>

Note: The temperature result measured from STLM75M2F would be a little higher than the ambient temperature due to the power dissipation of components on the board.
8.7.3 Smartcard

STMicroelectronics smartcard interface chip ST8024L is used on STM32G081B-EVAL Evaluation board for asynchronous 1.8V, 3V and 5V smartcards. It performs all supply protection and control functions based on the connections with STM32G081RBT6 listed in Table 13.

Table 13. Connection between ST8024L and STM32G081RBT6

<table>
<thead>
<tr>
<th>Signals of ST8024L</th>
<th>Description</th>
<th>Connect to STM32G081RBT6</th>
</tr>
</thead>
<tbody>
<tr>
<td>5V/3V</td>
<td>Smartcard power supply selection pin</td>
<td>PB15</td>
</tr>
<tr>
<td>I/OUC</td>
<td>MCU data I/O line</td>
<td>PA2</td>
</tr>
<tr>
<td>XTAL1</td>
<td>Crystal or external clock input</td>
<td>PD4</td>
</tr>
<tr>
<td>OFF</td>
<td>Detect card presence, Interrupt to MCU</td>
<td>PB12</td>
</tr>
<tr>
<td>RSTIN</td>
<td>Card reset input from MCU</td>
<td>PA15</td>
</tr>
<tr>
<td>CMDVCC</td>
<td>Start activation sequence input (Active Low)</td>
<td>PB0</td>
</tr>
<tr>
<td>1.8V</td>
<td>1.8 V Vcc operation selection. Logic high selects 1.8 V operation and overrides any setting on the 5V/3V pin.</td>
<td>PA3</td>
</tr>
</tbody>
</table>

Smartcard operates correctly when VDD > 2.7 V.

8.7.4 HDMI CEC

Two HDMI connectors CN1 and CN3 are available on STM32G081B-EVAL legacy peripheral daughterboard.

- The connector CN1 is HDMI sink connector with
  - DDC connected to I2C2 of STM32G081RBT6
  - HPD controlled by IO PD2 through transistor T1
  - CEC connected to PB10 through transistor T4
- The connector CN3 is HDMI source connector with
  - DDC connected to I2C1 of STM32G081RBT6 and shared with Temperature sensor and EXT I2C connector
  - HPD controlled by IO PD3
  - CEC connected to PB10 through transistor T4
  - HDMI 5V powered by power switch U1

The signals TDMS D+[0..2], TDMS_CLK+, TDMS D-[0..2], TDMS_CLK- on these two HDMI connectors are connected together.

The CEC injector mode can be enabled by some PCB reworks for debugging purpose only:

- Remove resistors R3, R4, R7, R9, R10, R15 and R22.
- Close solder bridges SB3, SB4, SB5 and SB6.

**Note:** The I/O PD2 must be set in open-drain output mode by firmware when working as an HPD signal control on the HDMI sink connector CN1.
8.7.5 IR LED and IR receiver

The IR receiver TSOP34836 is connected to PC6 of STM32G081RBT6 and a current around 100mA on IR LED is driven by PB9 through transistors T2 and T3 on the board.

Note: IR LED may be driven by PB9 directly with 20mA current when SB1 is closed and SB2 is open.

8.8 USB Type-C and Power Delivery daughterboard

The UCPD daughterboard is a development platform composed of STM32G081B-EVAL Evaluation board. This daughterboard is used for demonstrating the functionalities of the USB Type-C and USB Power Delivery (USB PD) technologies, facilitating the users to develop their solutions. Refer to Figure 3 for daughterboard structure.

Note: The USB PD reference design on the UCPD daughterboard is used to demonstrate the capability of STM32G081RBT6. This USB PD circuit may not pass all USB PD certifications.

Note: The UCPD daughterboard works with VDD=3.3V. So JP16 pin1-2 must be closed on mother board.

Note: The UCPD daughterboard conflicts with legacy peripheral daughterboard and Motor control on STM32G081B-EVAL Evaluation board.

8.8.1 USB Type-C receptacles

Two USB Type-C certified receptacles CN7 and CN5 are present on the UCPD daughterboard, representing respectively the PORT 1 and PORT 2. PORT 1 can be used as DRP (Dual-Role Port), which is eligible to supply another platform plugged by a USB Type-C cable when they are configured as Provider or, otherwise, to be supplied in case of Consumer configuration. PORT 2 can only be used as SINK.

Video signals on display port input connector (CN6) and data signals on USB3.1 Gen1 Type-B connector (CN4) are multiplexed on Type-C PORT 1 thanks to a crosspoint switch IC TUSB546-DCI. These signals on CN6 or on CN4 have to be generated by an external computer or notebook to evaluate the alternate mode (AM) capability of the USB PD technology. The crosspoint switch can be configured through I2C bus, and its I2C address is 0b1000100. The cable which is plugged into CN4 can be detected by PA15.

Same as Type-C PORT1, video signals on display port output connector (CN2) are connected to Type-C PORT 2 through another crosspoint switch IC CBTL08GP053 and DisplayPort Linear Redriver IC SN65DP141. I2C address of CBTL08GP053 is 0b0110000 and SN65DP141’s default I2C address is 0b0000000. A Type-A receptacle's (CN1) D+ and D- signals are also connected to Type-C PORT 2 directly. Its VBUS can be set by JP3 in Table 14.
8.8.2 Power Delivery and local power management

The UCPD daughterboard has its own external power jack (CN3, 19V/4A input) to support power delivery function and to provide up to 15V/3A on Type-C port1 (CN7).

The STM32G081B-EVAL Evaluation board can be powered by D5V from the UCPD daughterboard as shown in Figure 5. D5V on the UCPD daughterboard can be generated by three resources, 19V from external power jack, VBUS on Port 1 and VBUS on Port 2. A circuit is implemented on the UCPD daughterboard to automatically select external 19V power supply or VBUS on Port1, because external 19V and VBUS on Port1 are the two power sources for Port1 to D5V. A jumper JP5 is used to select D5V resources in Table 15.

8.8.3 VBUS management and discharge mechanism

Type-C port1 (CN7) can be used as DRP (Dual-Role Port), its VBUS can be managed for supplying other platforms as Provider, or to be supplied as Consumer. Two MOSFETs T6 and T7 are set in back-to-back configuration to protect and isolate the VBUS supplying path on both directions.

If the CN7 acts as Provider, the VBUS is on the supply path by mean of the discrete load switch (T6 and T7) driven by the STM32G081RBT6 (GPIO, PD3). For the Consumer case, the same VBUS path is managed by PD3 of STM32G081RBT6 enabling the discrete load switch.

All power profiles are listed in Table 16.
Moreover, the VBUS path on PORT1 presents a discharge mechanism implemented by the MOSFET T8 and an RC filter and controlled by PB13, and the VBUS path on PORT2 presents a discharge mechanism implemented by the MOSFET T9 and an RC filter and controlled by PB14.

### 8.8.4 VBUS voltage-sensing and current-sense stage

Each Type-C port is equipped by a voltage-sensing and a current-sensing stage which are matched with the voltage sensing carried by the STM32G081RBT6 ADC peripherals. Refer to Table 17 for detail. They are able to monitor the right power level applied on the port VBUS.

<table>
<thead>
<tr>
<th>CN7 role</th>
<th>Solder bridges setting</th>
<th>Power level</th>
<th>Source control signal</th>
<th>Voltage control signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Provider</td>
<td>SB2, SB3, SB23, SB26 ON SB13, SB14, SB15 OFF</td>
<td>PWM Mode: PWM voltage-3A</td>
<td>PD3 High</td>
<td>PC1-PWM signal</td>
</tr>
<tr>
<td></td>
<td>SB13, SB14, SB15 ON SB2, SB3, SB23, SB26 OFF</td>
<td>GPIO Mode: 5V / 9V / 15V-3A</td>
<td>PD3 High</td>
<td>5V: PC1(VSOURCE-9V) and PA1(VSOURCE-15V) tristate 9V: PC1(VSOURCE-9V) low 15V: PA1 (VSOURCE-15V) low</td>
</tr>
<tr>
<td>Consumer</td>
<td>-</td>
<td>Decided by Provider which is connected through Type-C cable</td>
<td>PD3 low</td>
<td>-</td>
</tr>
</tbody>
</table>

Moreover, the VBUS path on PORT1 presents a discharge mechanism implemented by the MOSFET T8 and an RC filter and controlled by PB13, and the VBUS path on PORT2 presents a discharge mechanism implemented by the MOSFET T9 and an RC filter and controlled by PB14.

### Table 17. VBUS Power Delivery profiles

<table>
<thead>
<tr>
<th>CN7 role</th>
<th>Solder bridges setting</th>
<th>Power level</th>
<th>Source control signal</th>
<th>Voltage control signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Provider</td>
<td>SB2, SB3, SB23, SB26 ON SB13, SB14, SB15 OFF</td>
<td>PWM Mode: PWM voltage-3A</td>
<td>PD3 High</td>
<td>PC1-PWM signal</td>
</tr>
<tr>
<td></td>
<td>SB13, SB14, SB15 ON SB2, SB3, SB23, SB26 OFF</td>
<td>GPIO Mode: 5V / 9V / 15V-3A</td>
<td>PD3 High</td>
<td>5V: PC1(VSOURCE-9V) and PA1(VSOURCE-15V) tristate 9V: PC1(VSOURCE-9V) low 15V: PA1 (VSOURCE-15V) low</td>
</tr>
<tr>
<td>Consumer</td>
<td>-</td>
<td>Decided by Provider which is connected through Type-C cable</td>
<td>PD3 low</td>
<td>-</td>
</tr>
</tbody>
</table>

### 8.8.5 CC management

Dead battery, VCONN output and fast role swap functions are supported on CC signal of Type-C PORT 1.

1. Dead battery enable
   Dead battery function is supported by OVP chip U17 and U16. And this function also
embedded in STM32G081RBT6. When OVP part U17 is bypassed, dead battery function in STM32G081RBT6 can be enable or disable through enable signals by set JP2 (CC1) or JP1 (CC2). Refer to Table 18 for detail.

**Table 18. Dead battery related jumpers**

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP1</td>
<td>Embed dead battery function is enable when JP1 is set as shown on the right (default setting).</td>
</tr>
<tr>
<td></td>
<td>Embed dead battery function is disable when JP1 is set as shown on the right.</td>
</tr>
<tr>
<td>JP2</td>
<td>Embed dead battery function is enable when JP2 is set as shown on the right (default setting).</td>
</tr>
<tr>
<td></td>
<td>Embed dead battery function is disable when JP2 is set as shown on the right.</td>
</tr>
</tbody>
</table>

2. VCONN output control

When the full-featured cable is connected to PORT 1, the VCONN is directly managed by the STM32G081RBT6 by mean of the PD4 or PB9 and the load switches STMPS2161 U10 and U14.

3. Fast role swap

Type-C PORT 1 can be configure to action fast role swap managed by STM32G081RBT6 through PA2 (CC1) and PB0 (CC2).
9 Connectors

9.1 Connectors on mother board

9.1.1 Motor control connector CN1

Table 19. Motor control connector CN1

<table>
<thead>
<tr>
<th>Description</th>
<th>Pin of STM32G081RBT6</th>
<th>Pin number of CN1</th>
<th>Pin number of CN1</th>
<th>Pin of STM32G081RBT6</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emergency STOP</td>
<td>PB12</td>
<td>1</td>
<td>2</td>
<td>-</td>
<td>GND</td>
</tr>
<tr>
<td>PWM-UH</td>
<td>PA8</td>
<td>3</td>
<td>4</td>
<td>-</td>
<td>GND</td>
</tr>
<tr>
<td>PWM-UL</td>
<td>PD2</td>
<td>5</td>
<td>6</td>
<td>-</td>
<td>GND</td>
</tr>
<tr>
<td>PWM-VH</td>
<td>PA9</td>
<td>7</td>
<td>8</td>
<td>-</td>
<td>GND</td>
</tr>
<tr>
<td>PWM-VL</td>
<td>PD3</td>
<td>9</td>
<td>10</td>
<td>-</td>
<td>GND</td>
</tr>
<tr>
<td>PWM-WH</td>
<td>PA10</td>
<td>11</td>
<td>12</td>
<td>-</td>
<td>GND</td>
</tr>
<tr>
<td>PWM-WL</td>
<td>PD4</td>
<td>13</td>
<td>14</td>
<td>PA1</td>
<td>BUS VOLTAGE</td>
</tr>
<tr>
<td>PHASE A CURRENT</td>
<td>PA2</td>
<td>15</td>
<td>16</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>PHASE B CURRENT</td>
<td>PA6</td>
<td>17</td>
<td>18</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>PHASE C CURRENT</td>
<td>PB10</td>
<td>19</td>
<td>20</td>
<td>-</td>
<td>GND</td>
</tr>
<tr>
<td>NTC BYPASS RELAY</td>
<td>PB9</td>
<td>21</td>
<td>22</td>
<td>-</td>
<td>GND</td>
</tr>
<tr>
<td>DISSIPATIVE BRAKE PWM</td>
<td>PB15</td>
<td>23</td>
<td>24</td>
<td>-</td>
<td>GND</td>
</tr>
<tr>
<td>+5V power</td>
<td>-</td>
<td>25</td>
<td>26</td>
<td>PA3</td>
<td>Heatsink temperature</td>
</tr>
<tr>
<td>PFC SYNC2</td>
<td>PD0</td>
<td>27</td>
<td>28</td>
<td></td>
<td>3.3V power</td>
</tr>
<tr>
<td>PFC SYNC1</td>
<td>PC1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PFC PWM</td>
<td>PB1</td>
<td>29</td>
<td>30</td>
<td>-</td>
<td>GND</td>
</tr>
</tbody>
</table>
9.1.2 External I2C connector CN2

Figure 11. I2C EXT connector CN2 (front view)

Table 19. Motor control connector CN1 (continued)

<table>
<thead>
<tr>
<th>Description</th>
<th>Pin of STM32G081RBT6</th>
<th>Pin number of CN1</th>
<th>Pin number of CN1</th>
<th>Pin of STM32G081RBT6</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Encoder A</td>
<td>PC6</td>
<td>31</td>
<td>32</td>
<td>-</td>
<td>GND</td>
</tr>
<tr>
<td>Encoder B</td>
<td>PB5</td>
<td>33</td>
<td>34</td>
<td>PB0</td>
<td>Encoder Index</td>
</tr>
</tbody>
</table>

Table 20. RF E2PROM connector CN2

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I2C1_SDA (PB7)</td>
<td>5</td>
<td>PWR (Define by daughterboard on CN5, or VDD when short CN5 pin17 and pin18)</td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td>6</td>
<td>NC</td>
</tr>
<tr>
<td>3</td>
<td>I2C1_SCL (PB6)</td>
<td>7</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>EX_RESET(PC0)</td>
<td>8</td>
<td>NC</td>
</tr>
</tbody>
</table>

9.1.3 Daughterboard connector CN4 and CN5

Two 18-pins male headers CN4 and CN5 are designed to connect with the legacy peripheral daughterboard or the UCPD daughterboard to STM32G081B-EVAL Evaluation mother board. All GPI/Os are available on CN4, CN5 and extension connector CN9, CN10.

Each pin on CN4 and CN5 can be used by a daughterboard after disconnecting it from the corresponding function block on STM32G081B-EVAL Evaluation board. Please refer to Table 21 and Table 22 for detail.
### Table 21. Daughterboard connector CN4

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Mother board Function</th>
<th>Legacy daughterboard Function (CN5)</th>
<th>UCPD daughterboard Function (CN9)</th>
<th>How to disconnect with function block on mother board</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PA1</td>
<td>MC_BusVoltage</td>
<td>LDR_OUT</td>
<td>V_CTL2</td>
<td>Keep JP1 open</td>
</tr>
<tr>
<td>2</td>
<td>PA15</td>
<td>-</td>
<td>Smartcard RST</td>
<td>USB3_DET</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>PB6</td>
<td>I2C1_SCL</td>
<td>I2C1_SCL</td>
<td>I2C1_SCL</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>PB7</td>
<td>I2C1_SDA</td>
<td>I2C1_SDA</td>
<td>I2C1_SDA</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>RESET#</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>PC6</td>
<td>MC_ENA</td>
<td>IR_IN</td>
<td>Display port</td>
<td>HPD_SOURCE</td>
</tr>
<tr>
<td>8</td>
<td>PB13</td>
<td>-</td>
<td>I2C2_SCL</td>
<td>DISCHARGE 1</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>PB14</td>
<td>-</td>
<td>I2C2_SDA</td>
<td>DISCHARGE 2</td>
<td>-</td>
</tr>
<tr>
<td>10</td>
<td>PB1</td>
<td>MC_PFCpwm</td>
<td>-</td>
<td>VSENSE 1</td>
<td>-</td>
</tr>
<tr>
<td>11</td>
<td>PB10</td>
<td>MC_CurrentC</td>
<td>HDMI_CEC</td>
<td>ISENSE 1</td>
<td>-</td>
</tr>
<tr>
<td>12</td>
<td>PA3</td>
<td>MC_heatsinkTemp</td>
<td>Smartcard 1V8</td>
<td>VSENSE 2</td>
<td>Keep JP2 open</td>
</tr>
<tr>
<td>13</td>
<td>PB12</td>
<td>MC_EmergencyST_OP</td>
<td>Smartcard OFF</td>
<td>ISENSE 2</td>
<td>Keep JP3 open</td>
</tr>
<tr>
<td>14</td>
<td>*3V3</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>15</td>
<td>PB11</td>
<td>Daughterboard detection</td>
<td>Daughterboard detection</td>
<td>Daughterboard detection &amp; USB PD output VSENSE</td>
<td>-</td>
</tr>
<tr>
<td>16</td>
<td>VDD_ANA</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>17</td>
<td>I2C_PU</td>
<td>I2C pull up power of CN2</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>18</td>
<td>VDD</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

### Table 22. Daughterboard connector CN5

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Mother board Function</th>
<th>Legacy daughterboard Function (CN4)</th>
<th>UCPD daughterboard Function (CN8)</th>
<th>How to disconnect with function block on mother board</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PA8</td>
<td>MC_UH</td>
<td>-</td>
<td>PORT1_CC1</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>PB15</td>
<td>MC_Dissipative brake</td>
<td>Smartcard 3/5 V</td>
<td>PORT1_CC2</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>PA9</td>
<td>MC_VH/USART1_TX_BOOT</td>
<td>-</td>
<td>PORT1_DB1</td>
<td>Keep JP10 pin2-3 open</td>
</tr>
<tr>
<td>4</td>
<td>PA10</td>
<td>MC_WH/USART1_RX_BOOT</td>
<td>-</td>
<td>PORT1_DB2</td>
<td>Keep JP8 pin2-3 open</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>PD4</td>
<td>MC_WL</td>
<td>Smartcard CK</td>
<td>VCONN_EN1</td>
<td>-</td>
</tr>
</tbody>
</table>
Table 22. Daughterboard connector CN5 (continued)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Mother board Function</th>
<th>Legacy daughterboard Function (CN4)</th>
<th>UCPD daughterboard Function (CN8)</th>
<th>How to disconnect with function block on mother board</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PB9</td>
<td>MC_NTC</td>
<td>IR_OUT</td>
<td>VCONN_EN2</td>
<td>-</td>
</tr>
<tr>
<td>8</td>
<td>PA2</td>
<td>MC_Current A</td>
<td>Smartcard TX</td>
<td>FRS_TX1</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>PB0</td>
<td>MC_ENINDEX</td>
<td>Smartcard CMDVCC</td>
<td>FRS_TX2</td>
<td>-</td>
</tr>
<tr>
<td>10</td>
<td>+5V</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>11</td>
<td>PB5</td>
<td>MC_ENB</td>
<td>Temp Sensor INT</td>
<td>Display port</td>
<td>HPD_IN</td>
</tr>
<tr>
<td>12</td>
<td>PC1</td>
<td>MC_PFCsync1</td>
<td>-</td>
<td>V_CTL1</td>
<td>-</td>
</tr>
<tr>
<td>13</td>
<td>PD0</td>
<td>MC_PFCsync2</td>
<td>-</td>
<td>PORT2_CC1</td>
<td>-</td>
</tr>
<tr>
<td>14</td>
<td>PD2</td>
<td>MC_UL</td>
<td>HDMI_HPD_SINK</td>
<td>PORT2_CC2</td>
<td>-</td>
</tr>
<tr>
<td>15</td>
<td>PD3</td>
<td>MC_VL</td>
<td>HDMI_HPD_SOURCE</td>
<td>SOURCE_EN</td>
<td>-</td>
</tr>
<tr>
<td>16</td>
<td>D5V</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>17</td>
<td>EXT I2C PWR</td>
<td>Power of CN2</td>
<td>5V</td>
<td>VDD</td>
<td>-</td>
</tr>
<tr>
<td>18</td>
<td>VDD</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

9.1.4 ST-LINK/V2-1 USB Micro-B connector CN6

The USB Micro-B connector CN6 is used to connect embedded ST-LINK/V2-1 to PC for debugging of board.

Figure 12. USB Micro-B connector CN6 (front view)

Table 23. USB Micro-B connector CN6

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VBUS (power)</td>
<td>4</td>
<td>ID</td>
</tr>
<tr>
<td>2</td>
<td>DM</td>
<td>5</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>DP</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
9.1.5 **ST-LINK/V2-1 programming connector CN7**

The connector CN7 is used only for embedded ST-LINK/V2-1 programming during board manufacturing. It is not populated by default and not for end user.

9.1.6 **microSD connector CN8**

![microSD connector CN8 (front view)](image)

**Figure 13. microSD connector CN8 (front view)**

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NC</td>
<td>5</td>
<td>MicroSDcard_CLK (PB3)</td>
</tr>
<tr>
<td>2</td>
<td>MicroSDcard_CS (PD1)</td>
<td>6</td>
<td>Vss/GND</td>
</tr>
<tr>
<td>3</td>
<td>MicroSDcard_DIN(PA7)</td>
<td>7</td>
<td>MicroSDcard_DOUT(PB4)</td>
</tr>
<tr>
<td>4</td>
<td>+3V3</td>
<td>8</td>
<td>NC</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>10</td>
<td>MicroSDcard_detect (PC9)</td>
</tr>
</tbody>
</table>

9.1.7 **Extension connector CN9 and CN10**

Two 22-pin male headers CN9 and CN10 can be used to connect with daughterboard or standard wrapping board to STM32G081B-EVAL Evaluation board. The standard width between CN9 pin1 and CN10 pin1 is 2700mils (68.58mm). The standard was implemented on the majority of Evaluation boards.

Each pin on CN9 and CN10 can be used by a daughterboard after disconnecting it from the corresponding function block on STM32G081B-EVAL Evaluation board. Please refer to Table 25 and Table 26 for detail.

**Table 24. microSD connector CN9**

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NC</td>
<td>5</td>
<td>MicroSDcard_CLK (PB3)</td>
</tr>
<tr>
<td>2</td>
<td>MicroSDcard_CS (PD1)</td>
<td>6</td>
<td>Vss/GND</td>
</tr>
<tr>
<td>3</td>
<td>MicroSDcard_DIN(PA7)</td>
<td>7</td>
<td>MicroSDcard_DOUT(PB4)</td>
</tr>
<tr>
<td>4</td>
<td>+3V3</td>
<td>8</td>
<td>NC</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>10</td>
<td>MicroSDcard_detect (PC9)</td>
</tr>
<tr>
<td>Pin</td>
<td>Description</td>
<td>Alternative Function</td>
<td>How to disconnect with function block on STM32G081B-EVAL board</td>
</tr>
<tr>
<td>-----</td>
<td>----------------------</td>
<td>----------------------</td>
<td>---------------------------------------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>PD8</td>
<td>LED3</td>
<td>Close SB11, Open SB14, SB34</td>
</tr>
<tr>
<td>3</td>
<td>PC7</td>
<td>GPIO_JOY_RIGHT</td>
<td>Open SB40</td>
</tr>
<tr>
<td>5</td>
<td>PA12</td>
<td>USART_1_RTS</td>
<td>Open SB16</td>
</tr>
<tr>
<td>7</td>
<td>PC9</td>
<td>GPIO_SD_DETECT</td>
<td>Open SB8</td>
</tr>
<tr>
<td>9</td>
<td>PD5</td>
<td>LED1</td>
<td>Open SB36</td>
</tr>
<tr>
<td>11</td>
<td>PD6</td>
<td>LED2</td>
<td>Open SB35</td>
</tr>
<tr>
<td>13</td>
<td>PC4</td>
<td>USART_1_TX</td>
<td>Open JP10 pin1-2</td>
</tr>
<tr>
<td>15</td>
<td>PC10</td>
<td>VCP_USART_3_TX</td>
<td>Open SB5</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>19</td>
<td>PC14</td>
<td>OSC32_IN</td>
<td>Remove R43, Close SB18</td>
</tr>
<tr>
<td>21</td>
<td>PC13</td>
<td>Button (Tamp, Wakeup2)</td>
<td>Open SB42</td>
</tr>
<tr>
<td>2</td>
<td>PD9</td>
<td>LED4</td>
<td>Close SB10, Open SB13, SB33</td>
</tr>
<tr>
<td>4</td>
<td>PA11</td>
<td>USART_1_CTS</td>
<td>Open SB28</td>
</tr>
<tr>
<td>6</td>
<td>PC8</td>
<td>GPIO_JOY_LEFT</td>
<td>Open SB39</td>
</tr>
<tr>
<td>8</td>
<td>PD1</td>
<td>GPIO_SD_CS</td>
<td>Open SB9</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>12</td>
<td>PC5</td>
<td>USART_1_RX</td>
<td>Open JP8 pin1-2</td>
</tr>
<tr>
<td>14</td>
<td>PB4</td>
<td>LCD/SD1_MISO</td>
<td>Open SB12</td>
</tr>
<tr>
<td>16</td>
<td>PC11</td>
<td>VCP_USART_3_RX</td>
<td>Open JP7</td>
</tr>
<tr>
<td>18</td>
<td>PC15</td>
<td>OSC32_OUT</td>
<td>Remove R44, Close SB19</td>
</tr>
<tr>
<td>20</td>
<td>D5V</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>22</td>
<td>+3V3</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Alternative Function</th>
<th>How to disconnect with function block on STM32G081B-EVAL board</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PA7</td>
<td>LCD/SD1_MOSI</td>
<td>Open SB24</td>
</tr>
<tr>
<td>3</td>
<td>PA5</td>
<td>AUDIO_OUT_DAC1_OUT2</td>
<td>Open JP6 pin2-3</td>
</tr>
<tr>
<td>5</td>
<td>PA13</td>
<td>SWDIO</td>
<td>Open SB4, Remove R48</td>
</tr>
<tr>
<td>7</td>
<td>PB8</td>
<td>GPIO_LCD_CS</td>
<td>Open SB27</td>
</tr>
<tr>
<td>9</td>
<td>PA0</td>
<td>JOY_SEL_TAMP_WKUP1</td>
<td>Open SB38</td>
</tr>
<tr>
<td>11</td>
<td>PC2</td>
<td>GPIO_JOY_UP</td>
<td>Open SB41</td>
</tr>
<tr>
<td>13</td>
<td>PF1</td>
<td>OSC_OUT</td>
<td>Remove R46, Close SB21</td>
</tr>
<tr>
<td>15</td>
<td>PF0</td>
<td>OSC_IN</td>
<td>Remove R45, Close SB20</td>
</tr>
</tbody>
</table>
### Table 26. Extension connector CN10 (continued)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Alternative Function</th>
<th>How to disconnect with function block on STM32G081B-EVAL board</th>
</tr>
</thead>
<tbody>
<tr>
<td>17</td>
<td>GND</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>19</td>
<td>PA14-BOOT SWCLK</td>
<td></td>
<td>BOOT0</td>
</tr>
<tr>
<td>21</td>
<td>VDD</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>PB2 POTENTIOMETER_ADC_IN10</td>
<td>Open SB43</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PA6 AUDIO_IN_ADC_IN6/ MC_CurrentB</td>
<td>Open JP4, Keep CN1 disconnected</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PA4 AUDIO_OUT_DAC1_OUT1</td>
<td>Open JP6 pin1-2, JP19</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>PB3 LCD/SD1_SCK</td>
<td>Open SB25</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>12</td>
<td>PC0 GPIO_EXT_RST</td>
<td>Remove R12, Keep CN2 disconnected</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>PC3 GPIO_JOY_DOWN</td>
<td>Open SB37</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>PC12 GPIO_LCD/SD_MOSI_DIR</td>
<td>Open SB26</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>PF2-NRST RESER</td>
<td>Open SB23</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>PF3-VBAT VBAT</td>
<td>Open JP15</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>PF4-VREF+ VREF+</td>
<td>Open SB17, SB22</td>
<td></td>
</tr>
</tbody>
</table>

### 9.1.8 RS232 and RS485 connector CN11

**Figure 14. RS232 and RS485 connector CN11 (front view)**

![RS232 and RS485 connector CN11](MS30720V1)

### Table 27. RS232 & RS485 connector CN11

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NC</td>
<td>6</td>
<td>Bootloader_BOOT0</td>
</tr>
<tr>
<td>2</td>
<td>RS232_RX (PC5 or PA10)</td>
<td>7</td>
<td>RS232_RTS(PA12)</td>
</tr>
<tr>
<td>3</td>
<td>RS232_TX (PC4 or PA9)</td>
<td>8</td>
<td>RS232_CTS(PA11) / Bootloader_RESET</td>
</tr>
</tbody>
</table>
9.1.9 Standard SWD connector CN12

Figure 15. Standard SWD debugging connector CN12 (top view)

Table 28. Standard SWD debugging connector CN12

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>2</td>
<td>VDD</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>4</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td>6</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>SWDAT(PA13)</td>
<td>8</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>SWCLK(PA14)</td>
<td>10</td>
<td>GND</td>
</tr>
<tr>
<td>11</td>
<td>10K pull-down</td>
<td>12</td>
<td>GND</td>
</tr>
<tr>
<td>13</td>
<td>NC</td>
<td>14</td>
<td>GND</td>
</tr>
<tr>
<td>15</td>
<td>RESET#</td>
<td>16</td>
<td>GND</td>
</tr>
<tr>
<td>17</td>
<td>10K pull-down</td>
<td>18</td>
<td>GND</td>
</tr>
<tr>
<td>19</td>
<td>10K pull-down</td>
<td>20</td>
<td>GND</td>
</tr>
</tbody>
</table>
9.1.10 High density SWD connector CN13

Figure 16. High density SWD debugging connector CN13 (top view)

Table 29. High density SWD debugging connector CN13

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>2</td>
<td>SWDAT(PA13)</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>4</td>
<td>SWCLK(PA14)</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>6</td>
<td>NC</td>
</tr>
<tr>
<td>7</td>
<td>KEY</td>
<td>8</td>
<td>NC</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>10</td>
<td>RESET#</td>
</tr>
</tbody>
</table>

9.1.11 TFT LCD connector CN14

A TFT color LCD board is mounted on CN14. Please refer to Section 1.6.7 for detail.

9.1.12 Audio jack CN15

A 3.5mm Stereo audio jack CN15 connected to audio DAC and ADC is available on STM32G081B-EVAL board.

9.1.13 5 V Power connector CN16

STM32G081B-EVAL Evaluation mother board can be powered from a DC 5V power supply via the external power supply jack (CN16) shown in Figure 17. The central pin of CN16 must be positive.

Figure 17. Power-supply connector CN16 (front view)
9.1.14 Analog input connector CN17

Table 30. Analog input-output connector CN17

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Analog input-output PB2</td>
<td>2</td>
<td>GND</td>
</tr>
</tbody>
</table>

9.2 Connectors on legacy peripheral daughterboard

9.2.1 HDMI sink connector CN1

Table 31. HDMI sink connector CN1

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,3,4,6,7,9,10,12</td>
<td>TMDS differential signal pair connected to CN3</td>
<td>16</td>
<td>i2C2_SDA (PB14)</td>
</tr>
<tr>
<td>13</td>
<td>CEC (PB10)</td>
<td>2,5,8,11,17</td>
<td>GND</td>
</tr>
<tr>
<td>14</td>
<td>NC</td>
<td>18</td>
<td>HDMI_5V_Sink</td>
</tr>
<tr>
<td>15</td>
<td>i2C2_SCL (PB13)</td>
<td>19</td>
<td>HPD (PD2 through transistor)</td>
</tr>
</tbody>
</table>
9.2.2  Smartcard connector CN2

Figure 20. Smartcard connector CN2 (top view)

Table 32. Smartcard connector CN2

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>5</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>RST</td>
<td>6</td>
<td>NC</td>
</tr>
<tr>
<td>3</td>
<td>CLK</td>
<td>7</td>
<td>I/O</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>8</td>
<td>NC</td>
</tr>
<tr>
<td>17</td>
<td>Card presence detection pin</td>
<td>18</td>
<td>Card presence detection pin</td>
</tr>
</tbody>
</table>
9.2.3 HDMI source connector CN3

Figure 21. HDMI source connector CN3 (front view)

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,3,4,6,7,9,10,12</td>
<td>TMDS differential signal pair connected to CN1</td>
<td>16</td>
<td>I2C1_SDA (PB7)</td>
</tr>
<tr>
<td>13</td>
<td>CEC (PB10)</td>
<td>2,5,8,11,17</td>
<td>GND</td>
</tr>
<tr>
<td>14</td>
<td>NC</td>
<td>18</td>
<td>HDMI_5V_Source from power switch U3</td>
</tr>
<tr>
<td>15</td>
<td>I2C1_SCL (PB6)</td>
<td>19</td>
<td>HPD (PD3)</td>
</tr>
</tbody>
</table>

9.2.4 Daughterboard female connector CN4 and CN5

Two female connectors CN4 and CN5 are used to implement the legacy peripheral daughterboard on the mother board. CN4 on legacy daughterboard is connected to CN5 on mother board, and CN5 on legacy daughterboard is connected to CN4 on mother board. Please refer to Section 9.1.3 for detail signal definition of these connectors.

9.3 Connectors on UCPD daughterboard

9.3.1 USB Type A connector CN1

Figure 22. USB Type A connector CN1 (front view)

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VBUS (power)</td>
<td>3</td>
<td>D+</td>
</tr>
<tr>
<td>2</td>
<td>D-</td>
<td>4</td>
<td>GND</td>
</tr>
</tbody>
</table>
9.3.2 DisplayPort source connector CN2

Figure 23. DisplayPort source connector CN2 (front view)

Table 35. DisplayPort source connector CN2

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LANE0_P</td>
<td>13</td>
<td>CONFIG1</td>
</tr>
<tr>
<td>3</td>
<td>LANE0_N</td>
<td>14</td>
<td>CONFIG2</td>
</tr>
<tr>
<td>4</td>
<td>LANE1_P</td>
<td>15</td>
<td>AUX_CH_P</td>
</tr>
<tr>
<td>6</td>
<td>LANE1_N</td>
<td>17</td>
<td>AUX_CH_N</td>
</tr>
<tr>
<td>7</td>
<td>LANE2_P</td>
<td>18</td>
<td>HPD (PC6)</td>
</tr>
<tr>
<td>9</td>
<td>LANE2_N</td>
<td>19</td>
<td>RETURN</td>
</tr>
<tr>
<td>10</td>
<td>LANE3_P</td>
<td>20</td>
<td>DP_PWR</td>
</tr>
<tr>
<td>12</td>
<td>LANE3_N</td>
<td>2,5,8,11,16</td>
<td>GND</td>
</tr>
</tbody>
</table>

9.3.3 19 V Power connector CN3

The UCPD daughterboard can be powered from a DC 19 V power supply via the external power supply jack (CN3) shown in Figure 24. And it is used for USB PD.

Figure 24. 19 V Power connector CN3 (front view)
9.3.4  USB3.1 Gen1 Type B connector CN4

Figure 25. USB3.1 Gen1 Type B connector CN4 (front view)

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VBUS (power)</td>
<td>5</td>
<td>SSTX-</td>
</tr>
<tr>
<td>2</td>
<td>D-</td>
<td>6</td>
<td>SSTX+</td>
</tr>
<tr>
<td>3</td>
<td>D+</td>
<td>7</td>
<td>GND_DRAIN</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>8</td>
<td>SSRX-</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>9</td>
<td>SSRX+</td>
</tr>
</tbody>
</table>

9.3.5  USB Type-C connector PORT2 CN5

Figure 26. USB Type-C connector PORT2 CN5 (front view)

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>GND</td>
<td>B1</td>
<td>GND</td>
</tr>
<tr>
<td>A2</td>
<td>TX1+</td>
<td>B2</td>
<td>TX2+</td>
</tr>
<tr>
<td>A3</td>
<td>TX1-</td>
<td>B3</td>
<td>TX2-</td>
</tr>
<tr>
<td>A4</td>
<td>VBUS</td>
<td>B4</td>
<td>VBUS</td>
</tr>
<tr>
<td>A5</td>
<td>CC1 (PD0)</td>
<td>B5</td>
<td>CC2 (PD2)</td>
</tr>
<tr>
<td>A6</td>
<td>D+</td>
<td>B6</td>
<td>D+</td>
</tr>
<tr>
<td>A7</td>
<td>D-</td>
<td>B7</td>
<td>D-</td>
</tr>
</tbody>
</table>
### Table 37. USB Type-C connector PORT2 CN5 (continued)

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A8</td>
<td>SBU1</td>
<td>B8</td>
<td>SBU2</td>
</tr>
<tr>
<td>A9</td>
<td>VBUS</td>
<td>B9</td>
<td>VBUS</td>
</tr>
<tr>
<td>A10</td>
<td>RX2-</td>
<td>B10</td>
<td>RX1-</td>
</tr>
<tr>
<td>A11</td>
<td>RX2+</td>
<td>B11</td>
<td>RX1+</td>
</tr>
<tr>
<td>A12</td>
<td>GND</td>
<td>B12</td>
<td>GND</td>
</tr>
</tbody>
</table>

### 9.3.6 Display port sink connector CN6

**Figure 27. DisplayPort sink connector CN6 (front view)**

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LANE3_N</td>
<td>13</td>
<td>CONFIG1</td>
</tr>
<tr>
<td>3</td>
<td>LANE3_P</td>
<td>14</td>
<td>CONFIG2</td>
</tr>
<tr>
<td>4</td>
<td>LANE2_N</td>
<td>15</td>
<td>AUX_CH_P</td>
</tr>
<tr>
<td>6</td>
<td>LANE2_P</td>
<td>17</td>
<td>AUX_CH_N</td>
</tr>
<tr>
<td>7</td>
<td>LANE1_N</td>
<td>18</td>
<td>HPD (PB5)</td>
</tr>
<tr>
<td>9</td>
<td>LANE1_P</td>
<td>19</td>
<td>RETURN</td>
</tr>
<tr>
<td>10</td>
<td>LANE0_N</td>
<td>20</td>
<td>DP_PWR</td>
</tr>
<tr>
<td>12</td>
<td>LANE0_P</td>
<td>2,5,8,11,16</td>
<td>GND</td>
</tr>
</tbody>
</table>
9.3.7 USB Type-C connector PORT1 CN7

Figure 28. USB Type-C connector PORT1 CN7 (front view)

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>GND</td>
<td>B1</td>
<td>GND</td>
</tr>
<tr>
<td>A2</td>
<td>TX1+</td>
<td>B2</td>
<td>TX2+</td>
</tr>
<tr>
<td>A3</td>
<td>TX1-</td>
<td>B3</td>
<td>TX2-</td>
</tr>
<tr>
<td>A4</td>
<td>VBUS</td>
<td>B4</td>
<td>VBUS</td>
</tr>
<tr>
<td>A5</td>
<td>CC1 (PA8)</td>
<td>B5</td>
<td>CC2 (PB15)</td>
</tr>
<tr>
<td>A6</td>
<td>D+</td>
<td>B6</td>
<td>D+</td>
</tr>
<tr>
<td>A7</td>
<td>D-</td>
<td>B7</td>
<td>D-</td>
</tr>
<tr>
<td>A8</td>
<td>SBU1</td>
<td>B8</td>
<td>SBU2</td>
</tr>
<tr>
<td>A9</td>
<td>VBUS</td>
<td>B9</td>
<td>VBUS</td>
</tr>
<tr>
<td>A10</td>
<td>RX2-</td>
<td>B10</td>
<td>RX1-</td>
</tr>
<tr>
<td>A11</td>
<td>RX2+</td>
<td>B11</td>
<td>RX1+</td>
</tr>
<tr>
<td>A12</td>
<td>GND</td>
<td>B12</td>
<td>GND</td>
</tr>
</tbody>
</table>

9.3.8 Daughterboard female connector CN8 and CN9

Two female connectors CN8 and CN9 are used to implement the UCPD daughterboard on mother board. CN8 on UCPD the daughterboard is connected to CN5 on the mother board, and CN9 on the UCPD daughterboard is connected to CN4 on the mother board. Please refer to Section 9.1.3 for detail signal definition of these connectors.
Appendix A  Electrical schematics

This chapter provides design schematics for the STM32G081B-EVAL key features to help users to implement these features in application designs:

- Figure 29: STM32G081B-EVAL mother board top on page 48
- Figure 30: STM32G081B-EVAL MCU on page 49
- Figure 31: STM32G081B-EVAL power on page 50
- Figure 32: STM32G081B-EVAL audio on page 51
- Figure 33: STM32G081B-EVAL LCD microSD on page 52
- Figure 34: STM32G081B-EVAL motor-control on page 53
- Figure 35: STM32G081B-EVAL peripherals on page 54
- Figure 36: STM32G081B-EVAL RS232 and RS485 on page 55
- Figure 37: STM32G081B-EVAL extension connectors on page 56
- Figure 38: STM32G081B-EVAL ST-LINK V2-1 on page 57
- Figure 39: STM32G081B-EVAL SWD on page 58
- Figure 40: STM32G081B-EVAL legacy peripheral daughterboard on page 59
- Figure 41: STM32G081B-EVAL legacy peripheral daughterboard HDMI and CEC on page 60
- Figure 42: STM32G081B-EVAL legacy peripheral daughterboard Smartcard and IR on page 61
- Figure 43: STM32G081B-EVAL legacy peripheral daughterboard temperature sensor and LDR on page 62
- Figure 44: STM32G081B-EVAL UCPD daughterboard top on page 63
- Figure 45: STM32G081B-EVAL UCPD daughterboard CC and VCONN on page 64
- Figure 46: STM32G081B-EVAL UCPD daughterboard port1 DP USB3 on page 65
- Figure 47: STM32G081B-EVAL UCPD daughterboard Type-C source con on page 66
- Figure 48: STM32G081B-EVAL UCPD daughterboard port2 DP on page 67
- Figure 49: STM32G081B-EVAL UCPD daughterboard Type-C sink con on page 68
- Figure 50: STM32G081B-EVAL UCPD daughterboard USB PD on page 69
- Figure 51: STM32G081B-EVAL UCPD daughterboard power on page 70
- Figure 52: STM32G081B-EVAL UCPD daughterboard source power on page 71
Figure 29. STM32G081B-EVAL mother board top
Figure 30. STM32G081B-EVAL MCU
Figure 31. STM32G081B-EVAL power
Figure 32. STM32G081B-EVAL audio

- VDD_ANA > 2.2V
  - Audio OUT
- VDD_ANA > 2.7V
  - Audio IN

Components listed include:
- C47: 180pF
- C51: 100nF
- R66: 100K
- R69: 100K
- TP8: MIC +
- TP9: MIC OUT
- R74: 1K
- R72: 100
- R73: 2.2K
- C54: 47pF
- R67: 15K
- RV1: [N/A]
- C46: [N/A]
- R62: 0
- R61: 510
- Audio_IN
- U12: TS461CLT
- C61: 10uF
- C59: 4.7uF
- R68: 18K
- R59: 82K
- R70: 680
- C58: 4.7uF
- PA6: VDD_ANA
- R108: 10K
- JP18: C69: 1uF
- C66: 330nF
- R89: 20K
- Audio_OUT_L
- C65: [N/A]
- C80: 330nF
- R93: 0
- C78: [N/A]
- R90: 4.7K
- C73: 1.5nF
- R94: 4.7K
- C76: 1.5nF
- C68: 220uF
- R86: 1K
- C77: 220uF
- R92: 1K
- C75: 1uF
- Default setting: close

Pin connections:
- PA4, PA5, PA6: VI13, V13, VOUT1
- 9: VCC
- 8: GND
- 7: VIN
- 2: VOUT2
- 3: Shutdown6
- 4: Bypass4
- 5: VIN2
- 1: VIN1
Figure 33. STM32G081B-EVAL LCD microSD
Figure 34. STM32G081B-EVAL motor-control
Figure 35. STM32G081B-EVAL peripherals

- Potentiometer
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Figure 36. STM32G081B-EVAL RS232 and RS485

[Diagram of STM32G081B-EVAL RS232 and RS485 connections]

- Component labels and pin connections for RS232 and RS485 interfaces.
Figure 38. STM32G081B-EVAL ST-LINK V2-1
Figure 40. STM32G081B-EVAL legacy peripheral daughterboard
Figure 41. STM32G081B-EVAL legacy peripheral daughterboard HDMI and CEC

Source
Sink

Open drain pin!

HDMI_5V_Sink
R20 1K
R7 1K
HDMI_5V_Sink
I2C2_SDA_5V
I2C2_SCL_5V
R9 47K
R10 47K

+3V3
R18 27K

HDMI_CEC_3V3

U1 STMPS2141STR@54

Sink Source
R22 1M
HDMI_HPD_Source_5V
I2C1_SCL_5V
I2C1_SDA_5V
R4 1.8K
R3 1.8K

+5V
R15 0

PD2
PB13
PB14
PB10
PD3
PB6
PB7

TMDS_Data2+
TMDS_Data2-
TMDS_Data1+
TMDS_Data1-
TMDS_Data0+
TMDS_Data0-
TMDS_Clock+
TMDS_Clock-

R8 1K

Open drain pin!

CN3
HD119F-3A09200

CN1
HD119F-3A09200

R11
4K

C2 4.7uF
GND

IN5
EN
OUT
FAULT

SB3
SB4
SB5
SB6

T1
9012

SD
SD

G
G

2N7002

HDMI_5V_Sink
PD2

FT pin & Open Drain mode needed

Figure 41. STM32G081B-EVAL legacy peripheral daughterboard HDMI and CEC

Source
Sink

Open drain pin!
Figure 42. STM32G081B-EVAL legacy peripheral daughterboard Smartcard and IR

Smart Card

IR

IR_LED

IR_Receiver
Figure 43. STM32G081B-EVAL legacy peripheral daughterboard temperature sensor and LDR

- Temperature sensor
- LDR
- Photo resistor
- Address (controlled)
- Reference: MB1351A0
- Date: 17-MAY-17
- Variant name is not interpreted until output
- Project: STM32G081B-EVAL Legacy peripheral daughter board

Components:
- STLM75M2F
- +5V
- C7: 100nF
- R23: 10K
- VDD
- I2C1_SCL_5V
- I2C1_SDA_5V
- A2: Pin 5
- A1: Pin 6
- A0: Pin 7
- VDD_ANA
- SB7
- R2: 8.2K
- PA1
- R1
- VT9ON1
- Address (controlled)
Figure 44. STM32G081B-EVAL UCPD daughterboard top

Mother board connectors

ADC input PB11: 0V: Daughter board detection: 1.35V  
DCDC_EN=0: U18 output measurement 0.43V-3.3V  
DCDC_EN=1: U18 output measurement 0.43V-3.3V
Figure 45. STM32G081B-EVAL UCPD daughterboard CC and VCONN

TYPE-C Source port CC management

VCONN power
Figure 46. STM32G081B-EVAL UCPD daughterboard port1 DP USB3

[Diagram of STM32G081B-EVAL UCPD daughterboard port1 DP USB3]
Figure 47. STM32G081B-EVAL UCPD daughterboard Type-C source con
Figure 48. STM32G081B-EVAL UCPD daughterboard port2 DP
Figure 49. STM32G081B-EVAL UCPD daughterboard Type-C sink con
Figure 50. STM32G081B-EVAL UCPD daughterboard USB PD

Power Delivery management (TypeC Port1)

Power Delivery management (TypeC Port2)
Figure 51. STM32G081B-EVAL UCPD daughterboard power
Figure 52. STM32G081B-EVAL UCPD daughterboard source power

Source Power

<table>
<thead>
<tr>
<th>Mode</th>
<th>Mount</th>
<th>Removed</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO</td>
<td>SB13, SB14, SB15</td>
<td>SB2, SB13, SB21, SB26</td>
</tr>
<tr>
<td>PWM (Default)</td>
<td>SB2, SB13, SB21, SB26</td>
<td>SB11, SB14, SB15</td>
</tr>
</tbody>
</table>

Step 1: DCDC_EN detects its voltage to ensure PSU 19V exist
Step 2: PWM_CTL provides about 0V level before DCDC_EN=1
Step 3: DCDC_EN=1, then PWM_CTL changes to provide PWM waveform by 0 and open-drain
### Appendix B  STM32G081B-EVAL IO Assignment

#### Table 40. STM32G081B-EVAL IO Assignment

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>IO Assignment on mother board</th>
<th>IO Assignment on legacy daughterboard</th>
<th>IO Assignment on UCPD daughterboard</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PC11</td>
<td>VCP_USART_3_RX</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>PC12</td>
<td>GPIO_LCD / SD_MOSI_DIR</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>PC13</td>
<td>KEY_TAMP_IN1, RTC_TS, RTC_OUT1, WKUP2</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>PC14 - OSC32_IN</td>
<td>OSC32_IN</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>PC15 - OSC32_OUT</td>
<td>OSC32_OUT</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>PF3 - VBAT</td>
<td>VBAT</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>PF4 - VREF+</td>
<td>VREF+</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>8</td>
<td>VDD_1</td>
<td>VDD</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>VSS_1</td>
<td>VSS</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>10</td>
<td>PF0 - OSC_IN</td>
<td>OSC_IN</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>11</td>
<td>PF1 - OSC_OUT</td>
<td>OSC_OUT</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>12</td>
<td>PF2 - NRST</td>
<td>NRST, (WKUP8)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>13</td>
<td>PC0</td>
<td>GPIO_EXT_RST</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>14</td>
<td>PC1</td>
<td>MC_IO_(PFC_sync1)</td>
<td>-</td>
<td>GPIO_9V_EN_LPTIM1_OUT</td>
</tr>
<tr>
<td>15</td>
<td>PC2</td>
<td>GPIO_JOY_UP</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>16</td>
<td>PC3</td>
<td>GPIO_JOY_DOWN</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>17</td>
<td>PA0</td>
<td>JOY_SEL_TAMP_IN2, WKUP1</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>18</td>
<td>PA1</td>
<td>MC_AIN1_COMP_1_INP (Bus voltage)</td>
<td>LDR_OUT_COMP_1_INP_ADC_IN1</td>
<td>GPIO_DP1_DET</td>
</tr>
<tr>
<td>19</td>
<td>PA2</td>
<td>MC_AIN2(CurrentA)</td>
<td>SMART_2_TX</td>
<td>TYPE-C_1_FRSTX</td>
</tr>
<tr>
<td>20</td>
<td>PA3</td>
<td>MC_AIN3(Heatsink temp)</td>
<td>GPIO_SMART_1V8</td>
<td>TYPE-C_2_V_ADC_IN3</td>
</tr>
<tr>
<td>21</td>
<td>PA4</td>
<td>AUDIO_OUT_DAC1_OUT1</td>
<td>-</td>
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<tr>
<td>22</td>
<td>PA5</td>
<td>AUDIO_OUT_DAC1_OUT2</td>
<td>-</td>
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<tr>
<td>23</td>
<td>PA6</td>
<td>AUDIO_IN_ADC_IN6 / MC_AIN6(CurrentB)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Pin No.</td>
<td>Pin Name</td>
<td>IO Assignment on mother board</td>
<td>IO Assignment on legacy daughterboard</td>
<td>IO Assignment on UCPD daughterboard</td>
</tr>
<tr>
<td>---------</td>
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<td>----------------------------------</td>
</tr>
<tr>
<td>24</td>
<td>PA7</td>
<td>LCD/SD1_MOSI</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>25</td>
<td>PC4</td>
<td>USART_1_TX</td>
<td>-</td>
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<tr>
<td>26</td>
<td>PC5</td>
<td>USART_1_RX</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>27</td>
<td>PB0</td>
<td>MC_TIM_3_CH3(Encoder index)</td>
<td>GPIO_SMART_CMDVCC</td>
<td>TYPE-C_1_FRSTX</td>
</tr>
<tr>
<td>28</td>
<td>PB1</td>
<td>MC_TIM_3_CH4(PFC_PWM)</td>
<td>-</td>
<td>TYPE-C_1_V_ADC_IN9</td>
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<tr>
<td>29</td>
<td>PB2</td>
<td>POT_ADC_IN10</td>
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<tr>
<td>30</td>
<td>PB10</td>
<td>MC_ADC_IN11(CurrentC)</td>
<td>HDMI_CEC</td>
<td>TYPE-C_1_I_ADC_IN11</td>
</tr>
<tr>
<td>31</td>
<td>PB11</td>
<td>BOARD_DET_ADC_IN15</td>
<td>BOARD_DET_ADC_IN15</td>
<td>BOARD_DET_ADC_IN15</td>
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<tr>
<td>32</td>
<td>PB12</td>
<td>MC_TIM_1_BK(EmergencySTOP)</td>
<td>GPIO_SMART_OFF</td>
<td>TYPE-C_2_I_ADC_IN16</td>
</tr>
<tr>
<td>33</td>
<td>PB13</td>
<td>-</td>
<td>I2C2_SCL (HDMI_SINK)</td>
<td>GPIO_DISCHARGE_1</td>
</tr>
<tr>
<td>34</td>
<td>PB14</td>
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<td>I2C2_SDA (HDMI_SINK)</td>
<td>GPIO_DISCHARGE_2</td>
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<tr>
<td>35</td>
<td>PB15</td>
<td>MC_IO_(Dissipative brake)</td>
<td>GPIO_SMART_3/5V</td>
<td>TYPE-C_1_CC2</td>
</tr>
<tr>
<td>36</td>
<td>PA8</td>
<td>MC_TIM_1_CH1(UH)</td>
<td>-</td>
<td>TYPE-C_1_CC1</td>
</tr>
<tr>
<td>37</td>
<td>PA9</td>
<td>USART_BOOT_1_TX / MC_TIM_1_CH2(VH)</td>
<td>-</td>
<td>TYPE-C_1_DBCC1</td>
</tr>
<tr>
<td>38</td>
<td>PC6</td>
<td>MC_TIM_3_CH1 (EncoderA)</td>
<td>IR_IN_TIM3_CH1</td>
<td>GPIO_DP2_HPDP</td>
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<td>39</td>
<td>PC7</td>
<td>GPIO_JOY_RIGHT</td>
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<td>40</td>
<td>PD8</td>
<td>LED3</td>
<td>-</td>
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<td>41</td>
<td>PD9</td>
<td>LED4</td>
<td>-</td>
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</tr>
<tr>
<td>42</td>
<td>PA10</td>
<td>USART_BOOT_1_RX / MC_TIM_1_CH3(WH)</td>
<td>-</td>
<td>TYPE-C_1_DBCC2</td>
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<tr>
<td>43</td>
<td>PA11 [PA9]</td>
<td>USART_1_CTS</td>
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<td>PA12 [PA10]</td>
<td>USART_1_RTS_DE_CK</td>
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<td>45</td>
<td>PA13</td>
<td>SWDIO</td>
<td>-</td>
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<td>46</td>
<td>PA14 - BOOTO</td>
<td>SWCLK / BOOTO0</td>
<td>-</td>
<td>-</td>
</tr>
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<td>47</td>
<td>PA15</td>
<td>-</td>
<td>GPIO_SMART_RST</td>
<td>GPIO_USB3_DET</td>
</tr>
<tr>
<td>48</td>
<td>PC8</td>
<td>GPIO_JOY_LEFT</td>
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<tr>
<td>49</td>
<td>PC9</td>
<td>GPIO_SD_DETECT</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>50</td>
<td>PD0</td>
<td>MC_TIM_16_CH1(PFC_sync 2)</td>
<td>-</td>
<td>TYPE-C_2_CC1</td>
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Table 40. STM32G081B-EVAL IO Assignment (continued)

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<tr>
<th>Pin No.</th>
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<th>IO Assignment on mother board</th>
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Appendix C  Federal Communications Commission (FCC) and Industry Canada (IC) Compliance Statements

C.1  FCC Compliance Statement

C.1.1  Part 15.19
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

C.1.2  Part 15.105
This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

C.1.3  Part 15.21
Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

C.2  IC Compliance Statement

C.2.1  Compliance Statement
Industry Canada ICES-003 Compliance Label: CAN ICES-3 (A)/NMB-3(A).

C.3  Déclaration de conformité
Étiquette de conformité à la NMB-003 d'Industrie Canada: CAN ICES-3 (A)/NMB-3(A).
Appendix D  Mechanical dimensions

Figure 53. Mechanical dimensions

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<th>Symbol</th>
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Revision history

Table 42. Document revision history

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<th>Date</th>
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