EVAL-RHRICL1ATV1, EVAL-RHRICL1ALV1, EVAL-RHRICL1AFV1 evaluation boards for the RHRPMICL1A

Introduction

This user manual provides an overview of the EVAL-RHRICL1ATV1, EVAL-RHRICL1ALV1 and EVAL-RHRICL1AFV1 evaluation boards developed for the RHRPMICL1A, rad-hard integrated current limiter IC. One evaluation board for each of the three operative modes of the RHRPMICL1A is available. Each evaluation tool includes all external components, needed for a complete electrical evaluation of the device functionality in the selected configuration.

Table 1. Application tools

Type	Part number	Configuration	Marking
Evaluation tools	EVAL-RHRICL1ATV1	Re-triggerable	RHRPMICL1ATV1 – RE-TRIGGERABLE
Evaluation tools	EVAL-RHRICL1ALV1	Latched	RHRPMICL1ALV1 – LATCHED ON/OFF
Evaluation tools	EVAL-RHRICL1AFV1	Foldback	RHRPMICL1AFV1 – FOLDBACK

Figure 1. EVAL-RHRICL1ATV1 (re-triggerable evaluation board)

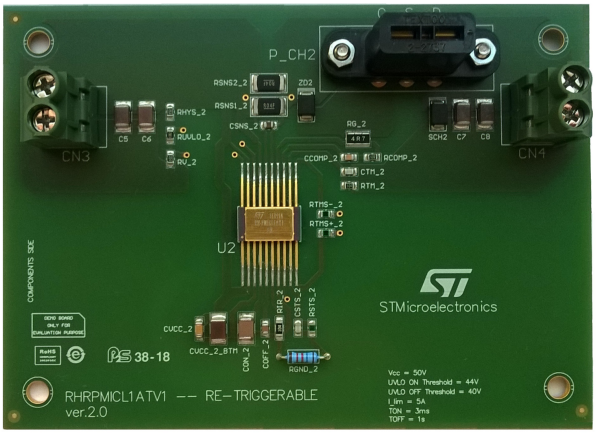


Figure 2. EVAL-RHRICL1ALV1 (latched evaluation board)

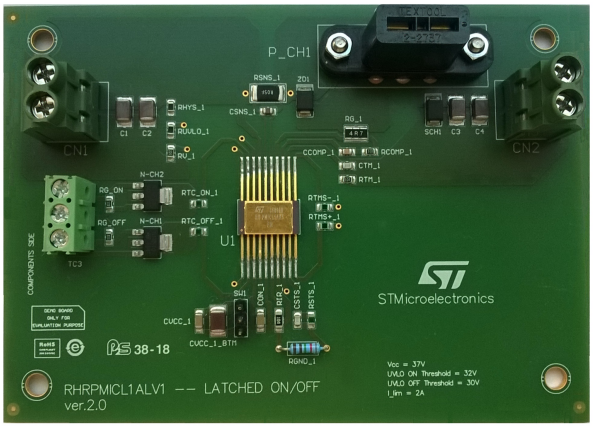
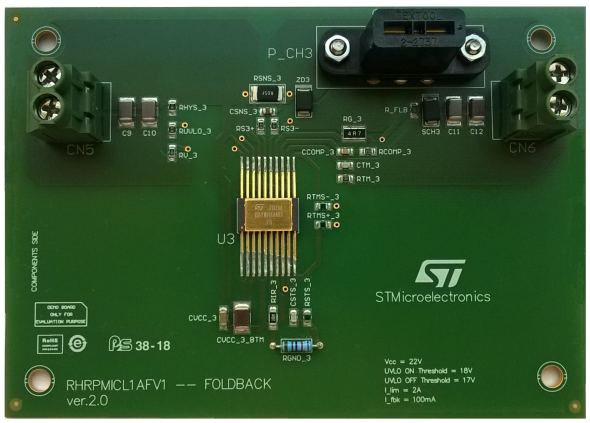


Figure 3. EVAL-RHRICL1AFV1 (foldback evaluation board)



1 Description

The RHRPMICL1A is an integrated current limiter designed to work as a high-side gate driver or intelligent power switch driver, with an external P-channel power MOSFET. It can be used as a universal solution to protect a power supply (from 8.5 V) from anomalous external current demand (for example, even in case of a short-circuit condition).

The device can operate with a supply voltage range from 8.5 V to 52 V. An undervoltage lockout circuitry has been implemented to guarantee the appropriate power supply integrity.

As the device can operate in floating ground configuration, in this user manual GND, the ground pin of the RHRPMICL1A device (pin 7), and MGND the ground of main bus are defined.

In case of overload, the device behavior changes according to its configured mode of operation:

- In **latched mode** the device provides current limitation capability for an external configurable time, called trip-off time, and if the overcurrent condition exceeds this time, the device switches OFF. In this case, the device may be switched ON again through the telecommand pin only or a UVLO deactivation/activation cycle
- In **re-triggerable mode**, after the trip-off time, that is externally configurable, the device switches OFF and remains in this state for a recovery time that is externally configurable. Once this time elapses, the device recovers its typical operation mode if the overload condition disappears, otherwise it switches cyclically ON and OFF again while the overload persists (hic-up mode)
- In **foldback mode**, in case of overload, the device provides current limitation with a value decreasing in tracking with the output voltage, reaching a fixed and safe value even if a short-circuit persists

The mode of operation can be selected by configuring the RHRPMICL1A pins according to the following configuration table, which is implemented in the evaluation boards:

Table 2. Applicable tools

Mode	SET_FLB	SET_STS	TC_ON	TC_OFF	TON	TOFF	Status at power-up
Latched OFF	0	0	Telecommand	Telecommand	C_{ON}	GND(1)	OFF
Latched ON	0	1	Telecommand	Telecommand	C_{ON}	GND(1)	ON
Re-triggerable	0	1	Vcc	Vcc	C_{ON}	C_{OFF}	ON
Foldback	1	1	Vcc	Vcc	GND(1)	GND(1)	ON

1. *GND refers to the RHRPMICL1A GND pin (pin 7), not to the main system ground (MGND).*

The characteristics and the main functionalities of each demonstration board are described in the following sections.

2 Common features and parameters

This section describes the features that are in common to the three boards, such as: UVLO, floating ground configuration, current limitation, analog and digital telemetries, and explains how to customize them by changing the external components on the board.

2.1 Undervoltage lockout and hysteresis settings

The UVLO and hysteresis can be programmed by a set of three resistors: the R_{HYS}, R_{UVLO} and R_V.

A 220 kΩ resistor is generally used for R_V, the other two resistors are obtained by the following equations:

$$R_{UVLO} = \frac{2.5 * R_V}{V_{TH\_ON} - 2.5} - K \quad (1)$$

$$R_{HYS} = \frac{2.5 * R_V}{V_{TH\_OFF} - 2.5} - R_{UVLO} \quad (2)$$

Where K=150 is a corrective fixed value to be added to Eq. (1) in order to take into account that during the rising phase of supply voltage, in the UVLO external resistor divider, R_{HYS} is shorted by a non-ideal switch embedded in the RHRPMICL1A.

2.2 Gate driving

The driver circuit is designed to drive an external P-channel power MOSFET (connected in high-side configuration) providing on the Vg pin a voltage signal in the range V_{CC} down to (V_{CC} - 12 V). All the evaluation boards are equipped with a through-hole socket where the power MOSFET can be easily housed.

When the device is ON and no current limitation is active, the Vg node is pulled down and the gate of the external MOSFET is internally clamped, about 12 V below the supply voltage V_{CC}. When the MOSFET has to be switched OFF, Vg is brought up to V_{CC}.

When the MOSFET is in current limitation mode, the Vg voltage is a value inside the range [V_{CC}-12 V, V_{CC}], defined by the limitation control loop.

2.3 Current sense and limitation function

The voltage drop on the external R_{SENSE} resistor is continuously monitored (by ISNS+ and ISNS- pins) and compared with a fixed 100 mV internally generated threshold.

The current limitation threshold can be externally set according to the application requirements by a suitable choice of the R_{SENSE} resistor.

In the re-triggerable and latched evaluation boards it is:

$$I_{LIM} = 100mV / R_{SENSE} \quad (3)$$

If the voltage drop on R_{SENSE} exceeds 100 mV means that the current demand is becoming excessive: an internal timer starts counting the trip-off time T_{ON} and the device enters the current limitation mode. In such a condition the limitation control loop is enabled in order to force Vg to the proper voltage level, limiting the current to the load.

Please refer Section 5.3.2 Bill of material of the EVAL-RHRICL1AFV1 board for the current limitation settings in the foldback mode evaluation board.

2.4 Floating ground configuration

The evaluation boards are equipped with the R_{GND} floating resistance mounted between the GND pin of the ICL (GND) and the system ground (MGND).

An embedded 14.8 V Zener diode chain allows the device to operate in floating ground configuration and protects the ICL device as its internal voltage supply is clamped at V_Z ~ 15 V (14.8 V typ).

According to the voltage value of the Bus supply and depending on the value of RGND, the device can work (or not) in floating ground condition, as follows:

1. **Vcc <14.8 V**

   The Zener diode chain is OFF and the R_{GND} is used to protect the system against a potential internal failure of the device. Since the typical current consumption of the ICL device is ~ 1.5 mA (the current contribution of the Zener diode chain is null in this case), in order to have a certain V_{GND}, the R_{GND} value is:

$$R_{GND} = \frac{V_{GND}}{1.5mA} \quad (4)$$

2. **Vcc > 14.8 V**

   In this case the Zener diode chain is enabled and the R_{GND} is also used to limit the maximum current consumption of the device, flowing through R_{GND} resistor from GND pin to the system ground MGND.

   This current consumption is given by the sum of two contributions:

   a. The net current consumption of the RHRPMICL1A (considering the internal Zener diode chain current as zero)

   b. The current consumption of the Zener diode chain in ON-state

For example, if we want to set the maximum current consumption of the RHRPMICL1A device to 2 mA, the value of R_{GND} is:

$$R_{GND} = \frac{V_{CC} - 14.8V}{2mA} \quad (5)$$

The RHRPMICL1A can be configured to work also with power Buses with voltage higher than 52 V, by adding the proper protection components to the application.

Guidelines on this feature are provided in the RHRPMICL1A datasheet, in the section 8.1.

2.5 Analog telemetry

The analog telemetry circuit gives information about the current flowing across the load. This circuit provides on the TM pin a source current whose value is instantly proportional to the current flowing from the bus supply line to the load. The voltage drop (V_{TM}) on the external resistor R_{TM} connected between the TM pin and MGND, is proportional to the load current (I_{SENSE}) flowing through R_{SENSE}, thus performing a current/voltage conversion:

$$R_{TM} = \frac{V_{TM}}{I_{RTM}} = \frac{V_{TM}}{I_{SENSE}} * \frac{R_{TMS}}{R_{SENSE}} \quad (6)$$

2.6 Digital telemetry (status telemetry)

The status telemetry circuit gives some information about the device status, which can be retrieved by monitoring the STS output pin, according to the following table.

Table 3. Signal on digital telemetry pin

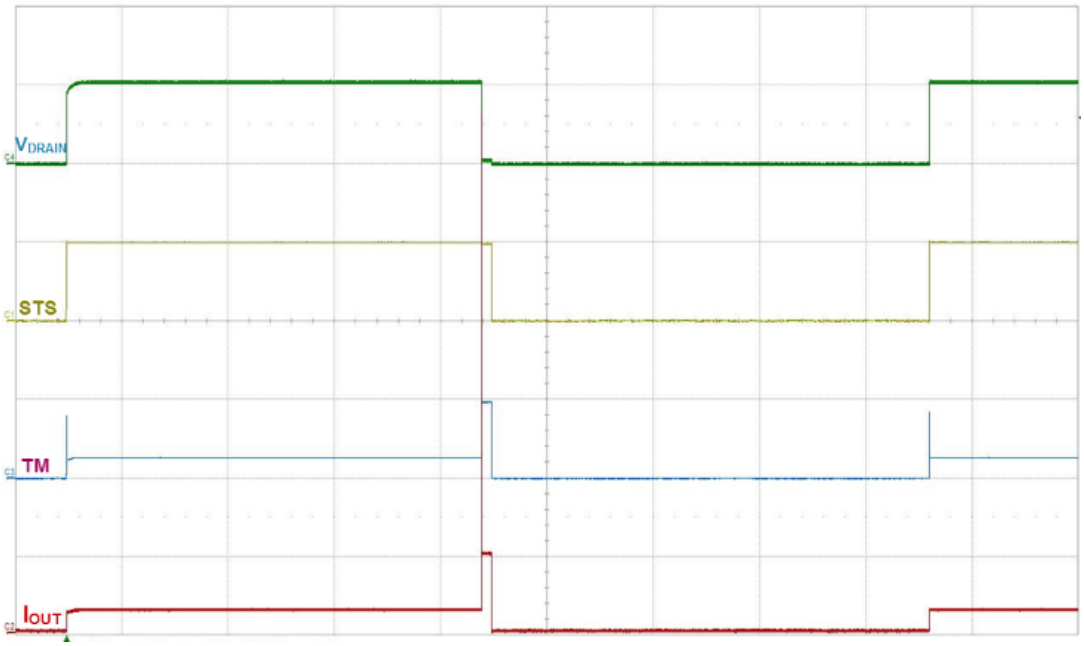
STS pin signal	RHRPMICL1A driver status
HIGH	ON
LOW	OFF

The STS is an open drain pin that can source a 100 µA fixed current; it is typically connected to MGND through an external resistor R_{STS}, setting the desired high logic level value V_{H_STS} as follows:

$$R_{STS} = \frac{V_{H\_STS}}{100\mu A} \quad (7)$$

The following picture shows the telemetry signals during the ICL operation.

Figure 4. **Telemetry signals**



3 Features: EVAL-RHRICL1ATV1, re-triggerable mode

3.1 Getting started

The EVAL-RHRICL1ATV1 evaluation board is customized to allow the test of re-triggerable operative mode of the RHRPMICL1A integrated current limiter (ICL).

In the re-triggerable mode, the ICL is able to restart automatically, recovering its normal operating mode if the current limitation cause is removed; besides, during any overload or output short-condition events, after the T_{OFF} recovery time elapses, the device tries to re-start for a dedicated T_{ON} slot time (trip-off time).

The configuration pins of the ICL in this mode are:

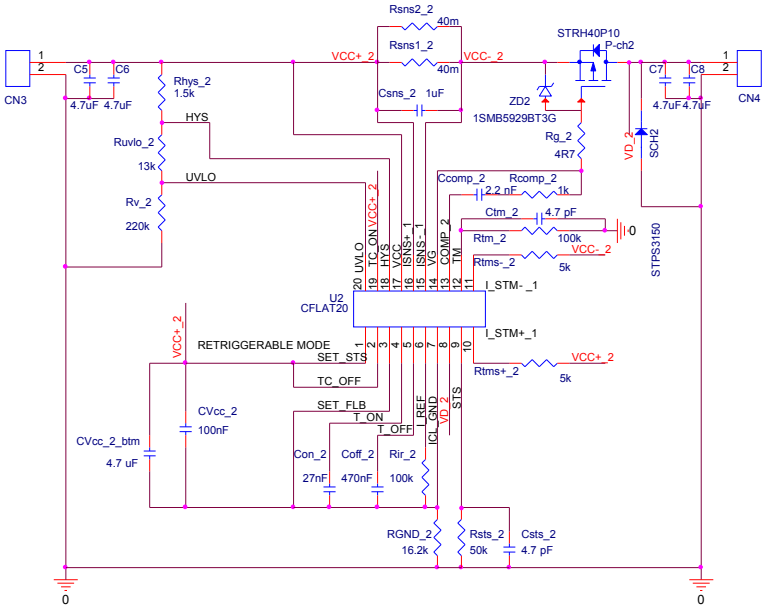
- Telecommand interface: disabled (TC_ON and TC_OFF both connected to V_{CC})
- SET_STS is connected to V_{CC}
- SET_FLB is connected to GND
- TON is connected to C_{ON}
- TOFF is connected to C_{OFF}

The external components of the board are pre-set to accomplish the following features:

- V_{CC} = 50 V with V_{TH_ON} = 44 V and V_{TH_OFF} = 40 V
- V_{HYS} = 4 V
- I_{LIM} = 5 A
- T_{ON} ~ 3 ms (typ 2.7 ms) with T_{OFF} ~ 1s (typ. 0.94 s)

The evaluation board schematic is shown below. Please note that the capacitor Csns_2, connected in parallel to the R_{SENSE}, affects the dynamic of the reaction time and therefore the decision whether to mount it or not is up to the application needs of the end user.

Figure 5. Re-triggerable evaluation board (schematic)

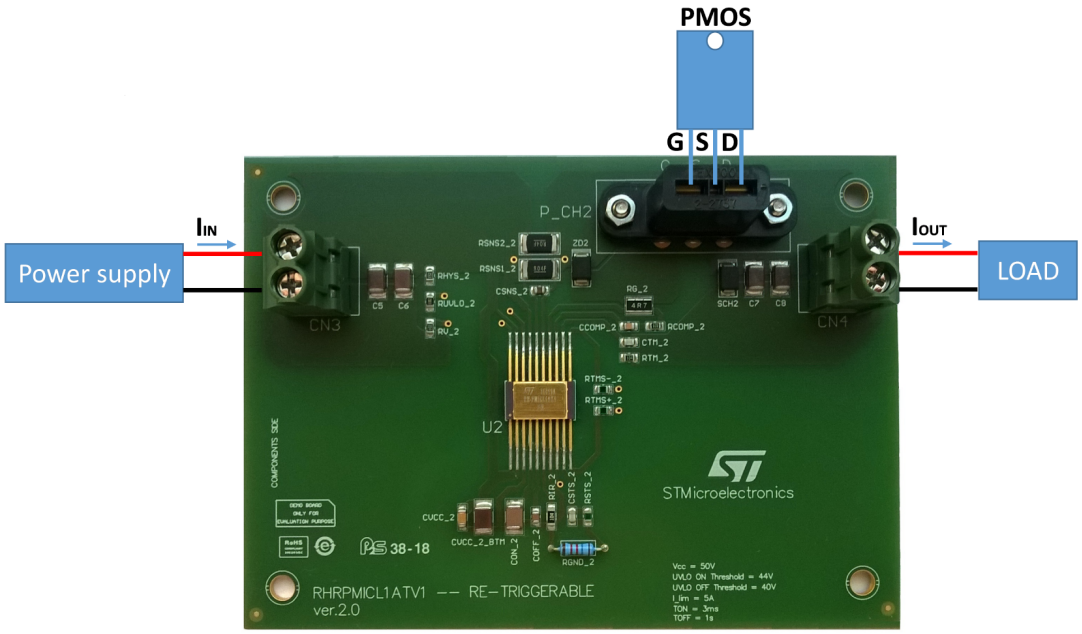


3.2 Operations

3.2.1 Power-on and testing environment

Connect a 50 V power supply to CN3, the load on CN4. The telecommand section is not activated in this evaluation board. The analog and digital telemetries are accessible on the R_{TM} and R_{STS} resistors respectively.

Figure 6. Testing environment



3.2.2 Trip-on and trip-off time programming

In re-triggerable mode, if the duration of the overcurrent is greater than the trip-off time T_{ON}, the external MOSFET is switched OFF after the T_{ON} time has elapsed and stays OFF for the recovery time T_{OFF}. When the T_{OFF} time elapses, the device restarts autonomously to its normal condition, turning ON again the MOSFET, if the current limitation cause is removed. Otherwise it switches cyclically ON and OFF again while the overload persists (hic-up mode).

The trip-off time T_{ON} is set by the C_{ON} capacitor connected between the pins TON and GND, and it is calculated by the following equation:

$$T_{ON} = R_{IR}{}^{*}C_{ON} \quad (8)$$

In the same way, the recovery time T_{OFF} is set through the external capacitor C_{OFF} connected between the pins T_{OFF} and GND. The C_{OFF} capacitor is charged with a constant current whose value is a fraction (typ. 1/20) of I_{REF} current (externally set by the resistor R_{IR} connected between the I_REF pin and GND). The charging phase of C_{OFF} capacitor starts as soon as the T_{ON} time has elapsed, therefore the T_{OFF} time is equal to the C_{OFF} charging time defined by:

$$T_{OFF} = 20{}^{*}R_{IR}{}^{*}C_{OFF} \quad (9)$$

In the equations above, unit for T_{ON} and T_{OFF} are in seconds, for resistance in Ohm and for capacitance in Farads.

The typical behavior of the device configured in re-triggerable mode is depicted below (timing is not in scale).

Figure 7. Overload shorter than T_{ON}+T_{OFF}

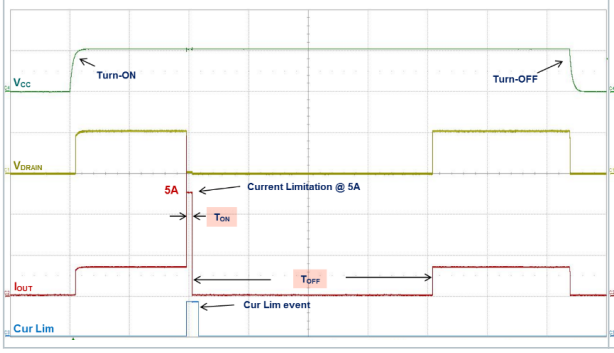


Figure 8. Overload longer than T_{ON}+T_{OFF}

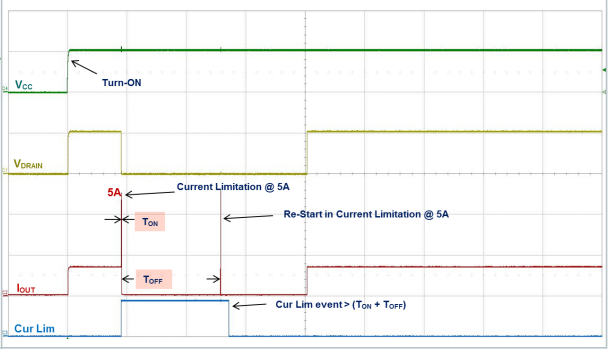
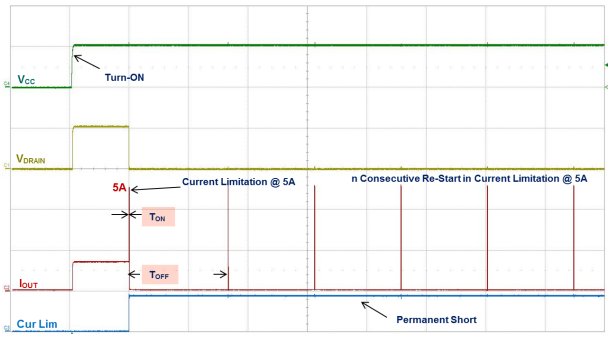


Figure 9. Continuous short-circuit



3.3 Evaluation board layout and BOM

3.3.1 Layout of the EVAL-RHRICL1ATV1 board

Figure 10. EVAL-RHRICL1ATV1 top layout

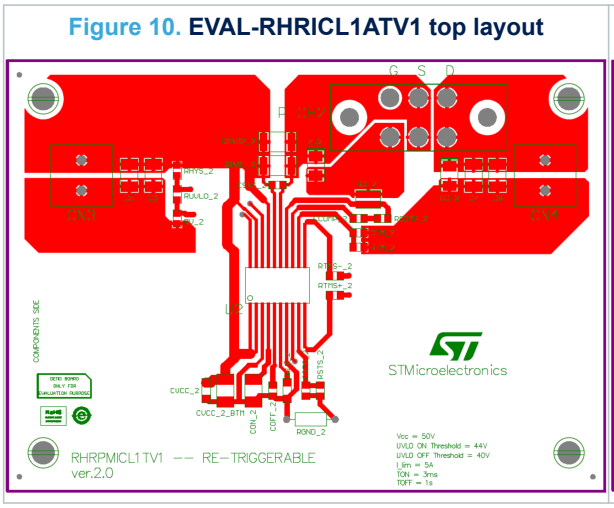
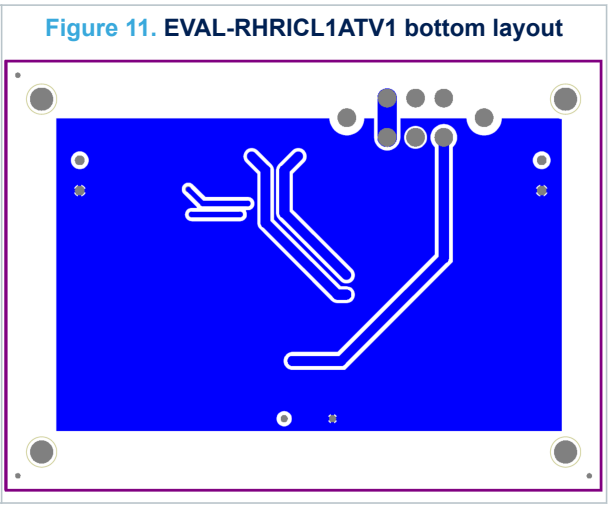


Figure 11. EVAL-RHRICL1ATV1 bottom layout



3.3.2 Bill of material of the EVAL-RHRICL1ATV1 board

Table 4. Bill of material

Item	Qty	Reference	Part / value	Voltage current	Manufacturer	Manufacturer code	More info	Footprint package
1	2	CN3, CN4	2PIN screw connector	Pitch 6.35 mm	Phoenix contact	1714955	INPUT (CN1) and OUTPUT (CN2) connectors	TH
2	4	C5,C6, C7,C8	4.7 µF capacitor	100 V	TDK	C4532X7S2A475M	X7S	1812
3	1	CVcc_2_btm	4.7 µF capacitor	100 V	TDK	C4532X7S2A475M	X7S	1812
4	1	CVcc_2	100 nF	100 V	MULTICOMP	MCCA000490	X7R	1206
5	1	Csns_2	1 µF	10 V	KEMET	C0805C105K8NACTU	X8L	0805
6	1	Coff_2	470 nF	50 V	KEMET	C0805C474K5RAC	X7R	0805
7	1	Ccomp_2	2.2 nF	50 V	AVX	08055C222JAT2A	X7R	0805
8	2	C_TM_2 C_STS_2	47 pF	50 V	KEMET	C0805C470J5GACTU	NPO	0805
9	1	Con_2	27 nF	50 V	KEMET	C1812C273J5GACTU	NPO	1812
10	1	Rv_2	220 kΩ 0.125 W	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA6AEB224V		0805
11	2	Rtms+_2, Rtms-_2	5 kΩ 0.200 W	100 V, 0.1%, 5 ppm/°C	Vishay thin film	PNM0805E5001BST5		0805
12	1	Rtm_2	100 kΩ 0.125 W	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA6AEB104V	I=20 µA	0805
13	1	Rsts_2	50 kΩ 0.200 W	100 V, 0.1%, 25 ppm/°C	Vishay	PNM0805E5002BST5	I=100 µA	0805
14	1	RGND_2 (R_floating)	16.2 kΩ 0.600 W	1%	Vishay	MBB02070C1622FCT00		TH
15	1	Rg_2	4.7 Ω 1 W	200 V, 1%	Panasonic	ERJB1BF4R7U		1020
16	2	Rsns1_2 Rsns2_2	40 mΩ 1 W	1%, 75 ppm/°C	VISHAY	WSL2512R0400FEA	I=0.5 A, 10 A	2512
17	1	Rhys_2	1.5 kΩ 0.125 W	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA6AEB152V		0805
18	1	Ruvlo_2	13 kΩ 0.125 W	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA6AEB133V		0805
19	1	Rcomp_2	1 kΩ 0.125 W	0.1%, 25 ppm/°C	Panasonic	ERA6AEB102V		0805

Item	Qty	Reference	Part / value	Voltage current	Manufacturer	Manufacturer code	More info	Footprint package
20	1	Rir_2	100 kΩ 0.250 W	150 V, 0.1%, 25 ppm/°C	Panasonic	ERA8AEB104V	I=10 µA	1206
21	1	ZD2	Zener	15 V, 3 W	ON Semiconductor	1SMB5929BT3G	Zener	SMB-CASE403A
22	1	SCH2	STPS3150	3 A, 150 V	ST	STPS3150U	Diode 100 V, 5 A	SMB
23	1	P_ch2 SOCKET	P-ch TO254AA socket (STRH40P10)	34 A, 100 V	3M TOUCH SYSTEMS	203-2737-55-1102	P-channel, B_{Vdss} 100 V, id 48 A, $R_{DS(on)}$ 60 mΩ, Qg 162 nC	TO-254 AA
24	1	U2	ICL001		ST			FLAT20

4 Features: EVAL-RHRICL1ALV1, latched mode

4.1 Getting started

The EVAL-RHRICL1ALV1 evaluation board is customized to allow the test of latched operative mode of the RHRPMICL1A integrated current limiter (ICL).

In the latched mode, if the duration of the overcurrent event is greater than the trip-off time T_{ON}, the device remains in current limitation for the T_{ON} interval, then the external MOSFET is latched OFF until a reset is given through either the telecommand interface or a UVLO activation/deactivation cycle. Depending on the SET_STS pin logic status the device can be programmed to start up in latched-ON or latched-off mode.

The configuration pins of the ICL in this mode of operation are the following:

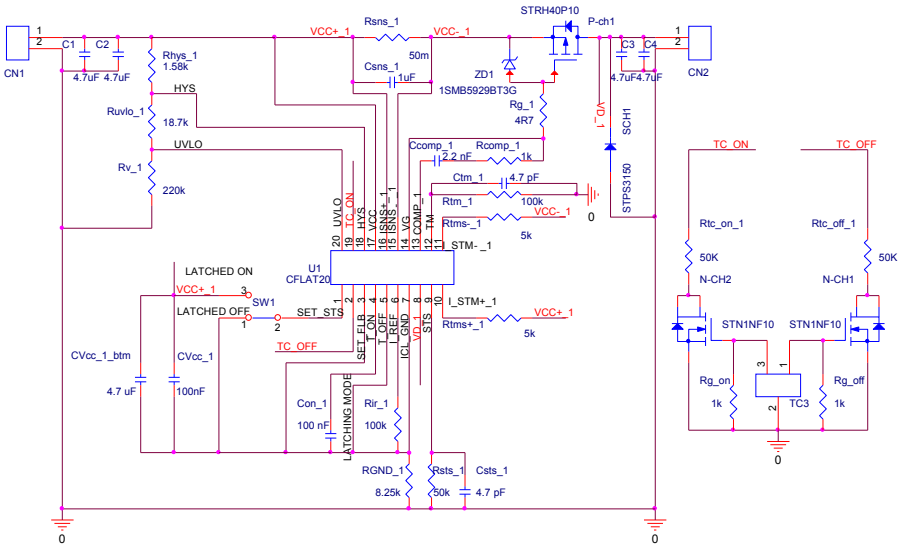
- Telecommand interface: enabled
- SET_STS is connected to V_{CC} (latched-ON) or GND (latched-OFF) through the switch *SW1*
- SET_FLB is connected to GND
- TON is connected to C_{ON}
- TOFF is connected to GND

The external components of the board are pre-set to accomplish the following features:

- V_{CC} = 37 V with V_{TH_ON} = 32 V and V_{TH_OFF} = 30 V
- V_{HYS} = 2 V
- I_{LIM} = 2 A
- T_{ON} ~ 10 ms
- TC_ON and TC_OFF are available on *TC3* connector
- SET_STS can be connected to V_{CC} or GND through the switch *SW1*

The evaluation board schematic is shown below. Please note that the capacitor Csns_1, connected in parallel to the R_{SENSE}, affects the dynamic of the reaction time and therefore the decision whether to mount it or not is up to the application needs of the end user.

Figure 12. Latched evaluation board schematic



4.2 Operations

4.2.1 Power-on and testing environment

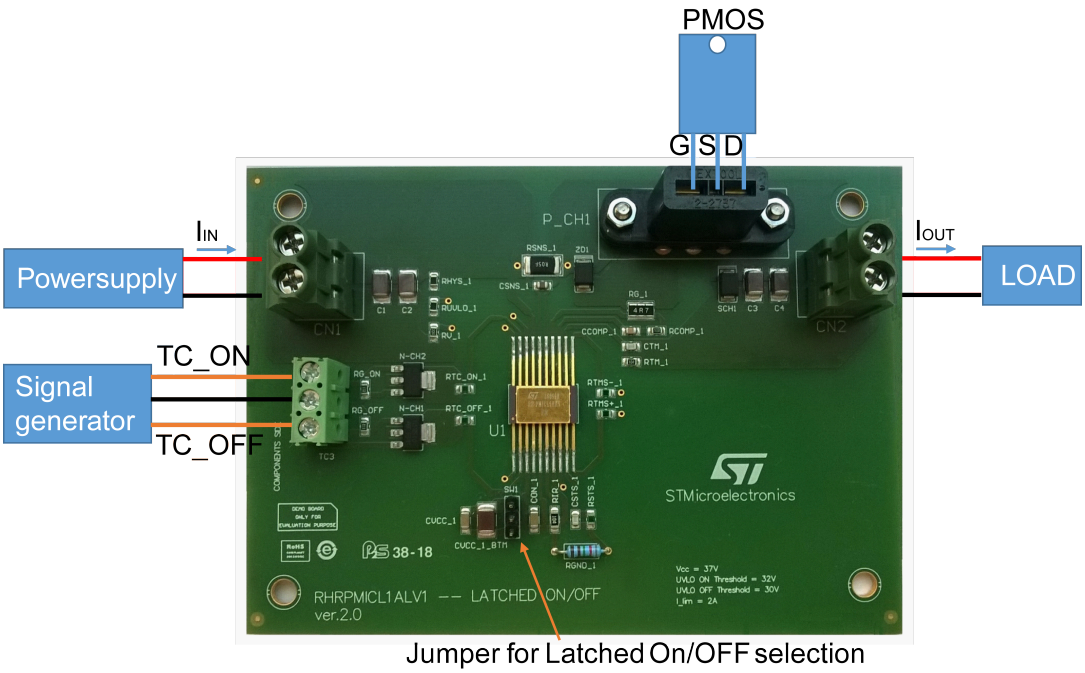
Connect a 37 V power supply to CN1, the load on CN2.

The telecommand section is available on the TC3 connector. Separated signals TC_ON and TC_OFF are applied to drive properly the telecommand interface.

Connect a jumper on SW1 in the position 1-2 to set the latched-OFF configuration, or in the position 2-3 for latched-ON one.

Analog and digital telemetries are accessible on the R_{TM} and R_{STS} resistors respectively.

Figure 13. Testing environment



4.2.2 Trip-off time programming

In latched mode, if the duration of the overcurrent is greater than the trip-off time T_{ON}, the device remains in current limitation for the T_{ON} interval, after the external MOSFET is switched OFF and stays OFF until the device is reset through the telecommand interface or UVLO activation/deactivation cycling. The trip-off time T_{ON} is set by the C_{ON} capacitor connected between the pins TON and GND, and it is calculated by the following formula:

$$T_{ON} = R_{IR} * C_{ON} \quad (10)$$

4.2.3 Telecommand interface

The telecommand interface is available through the TC_ON and TC_OFF pins of the ICL device. On the EVAL-RHRICL1ALV1 board the telecommand pins are driven by two additional MOSFET transistors (NCH_1 and NCH_2). The gates of these transistors are available by TC3 connector.

The device is switched ON by applying a positive pulse signal of the typical duration of 100 µs between terminal 3 and 2 of connector TC3 (Figure 12. Latched evaluation board schematic); or in alternative way, the device is switched ON by applying a negative pulse signal of the typical duration of 100µs directly to the pin TC_ON.

The device is switched OFF by applying a positive pulse signal of the typical duration of 100 µs between terminal 1 and 2 of connector TC3 (Figure 12. Latched evaluation board schematic); or in alternative way, the device is switched OFF by applying a negative pulse signal of the typical duration of 100 µs directly to the pin TC_OFF.

In order to have a more robust implementation, unwanted ON/OFF pulses having a short duration (< 10 µs) are ignored giving out a sort of noise immunity of the telecommand system. In case of contemporaneous application of ON and OFF commands, the OFF command has the priority; this means for example that, in case of a failure of the telecommand interface resulting in a permanent ON state, it is possible to switch OFF the device by sending an OFF command.

The typical behavior of the device configured in latched mode is depicted below (timing not in scale).

Figure 14. Latched-on at start-up diagram

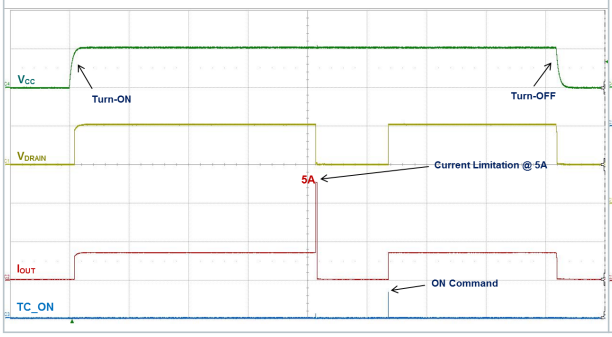
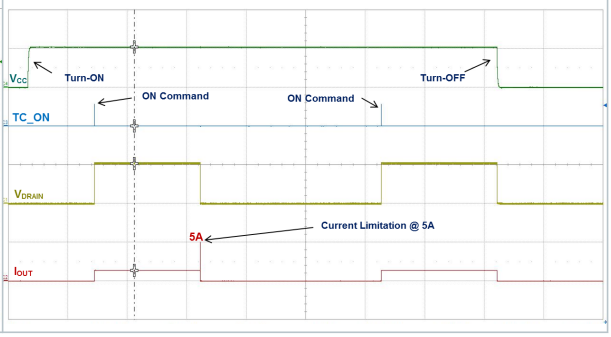


Figure 15. Latched-off at start-up diagram



4.3 Evaluation board layout and BOM

4.3.1 Layout of the EVAL-RHRICL1ALV1 board

Figure 16. EVAL-RHRICL1ALV1 top layout

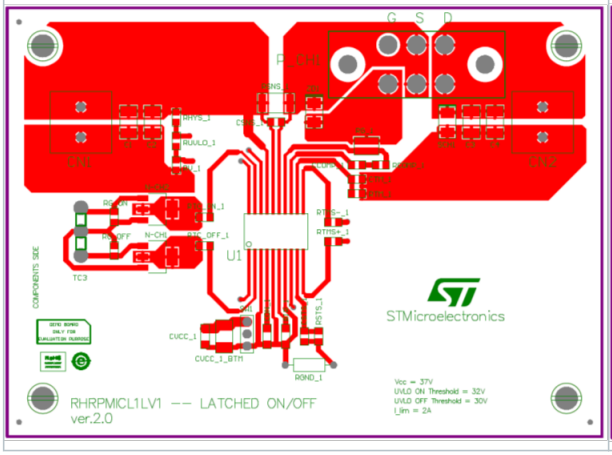
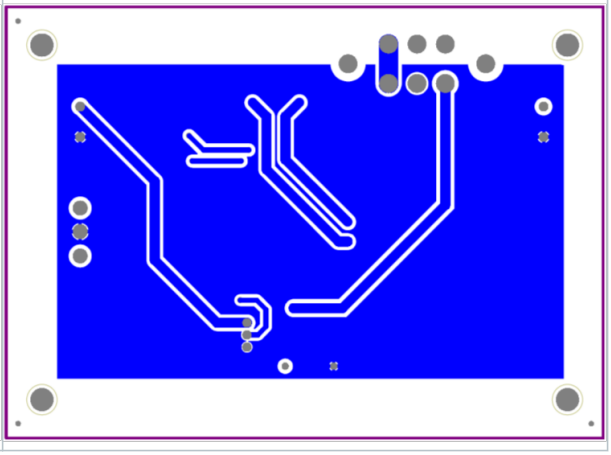


Figure 17. EVAL-RHRICL1ALV1 bottom layout



4.3.2 Bill of material of the EVAL-RHRICL1ALV1 board

Table 5. Bill of material

Item	Qty	Ref.	Part/ value	Voltage current	Manufacturer	Manufacturer code	More info	Footprint package
1	2	CN1, CN2	2-pin screw connector	Pitch-6.35 mm	Phoenix contact	1714955	INPUT (CN1) and OUTPUT (CN2) connectors	TH
2	4	C1, C2, C3, C4	4.7 µF capacitor	100 V	TDK	C4532X7S2A475M	X7S	1812
3	1	CVcc_1_btm	4.7 µF capacitor	100 V	TDK	C4532X7S2A475M	X7S	1812
4	1	CVcc_1	100 nF	100 V	MULTICOMP	MCCA000490	X7R	1206
5	1	Csns_1	1 µF	10 V	KEMET	C0805C105K8NACTU	X8L	0805
6	1	Ccomp_1	2.2 nF	50 V	AVX	08055C222JAT2A	X7R	0805
7	2	C_TM_1 C_STS_1	47 pF	50 V	KEMET	C0805C470J5GACTU	NPO	0805
8	1	Con_1	100 nF	50 V	AVX	12065C104KAT2A	X7R	1206
9	1	Rv_1	220 kΩ	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA6AEB224V	0.125 W	0805
10	2	Rtms+_1, Rtms-_1	5 kΩ	100 V, 0.1%, 25 ppm/°C	Vishay thin film	PNM0805E5001BST5	0.200 W	0805
11	1	Rtm_1	100 kΩ	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA6AEB104V	I=20 µA, 0.125 W	0805
12	1	Rsts_1	50 kΩ	100 V, 0.1%, 25 ppm/°C	Vishay	PNM0805E5002BST5	I=100 µA, 0.200 W	0805
13	1	RGND_1 (R_floating)	8.25 kΩ	1%	Vishay	MBB02070C8251FCT00	I=2 mA, 0.6 W	TH
14	1	Rg_1	4.7 Ω	200 V, 1%	Panasonic	ERJB1BF4R7U	1 W	1020
15	1	Rsns_1	50 mΩ	1 W, 1% ± 75 ppm/°C	Vishay DALE	WSL2512R0500FEA	1 W	2512
16	1	Rhys_1	1.58 kΩ	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA6AEB1581V	0.125 W	0805

Item	Qty	Ref.	Part/ value	Voltage current	Manufacturer	Manufacturer code	More info	Footprint package
17	1	Ruvlo_1	18.7 kΩ	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA6AEB1872V	0.125 W	0805
18	1	Rcomp_1	1 kΩ	0.1%, 25 ppm/°C	Panasonic	ERA6AEB102V	125 mW	0805
19	1	Rir_1	100 kΩ	150 V, 0.1%, 25 ppm/°C	Panasonic	ERA8AEB104V	I=10 µA, 0.250 W	1206
20	1	SW1	3-way switch					jumper 3vie
21	1	ZD1	Zener	15 V, 3 W	ON Semiconductor	1SMB5929BT3G	Zener	SMBCASE 403A
22	1	SCH1	STPS3150	3 A, 150 V	ST	STPS3150U	Diode 100 V-5 A	SMB
23	1	P_ch1 SOCKET	P-ch TO254AA socket (STRH40P10)	34 A, 100 V	3M TOUCH SYSTEMS	203-2737-55-1102	P-channel, B_{Vdss} 100 V, Id 48 A, $R_{DS(on)}$ 60 mΩ, Qg 162 nC	
24	1	U1	ICL001		ST			FLAT20
25	2	N-CH1, N-CH2	STN1NF101A, 100 V	V_{gsth} = 3 V	ST	STN1NF10	N-ch or NPN from 60 V, 100 V	SOT-223
26	2	Rg_on_1, Rg_off_1	1 kΩ	150 V, 1%	Vishay	CRCW08051K00FKEA	125 mW	0805
27	2	Rtcon_1, Rtcoff_1	50 kΩ 0.200 W	100 V, 0.1%, 25 ppm/°C	VISHAY thin film	PNM0805E5002BST5	To pull down	0805
28	1	TC3 CONN	3-way screw contact		PHOENIX contact	1935174	Telecomm. external connector	TH

5 Features: EVAL-RHRICL1AFV1, foldback mode

5.1 Getting started

The EVAL-RHRICL1AFV1 evaluation board is customized to allow the test of foldback operative mode of the RHRPMICL1A integrated current limiter (ICL).

In the foldback mode, when an overcurrent event is detected, the ICL device provides a current limitation profile whose value goes to tracking with the output voltage, reaching a small and safe value I_F (see Figure 20. Foldback current limiter characteristic even if a short-circuit on the load side occurs and persists.

This allows maintaining a safe power dissipation without shutting down the device, in case of failure.

The pin configuration of the ICL in this operation mode is:

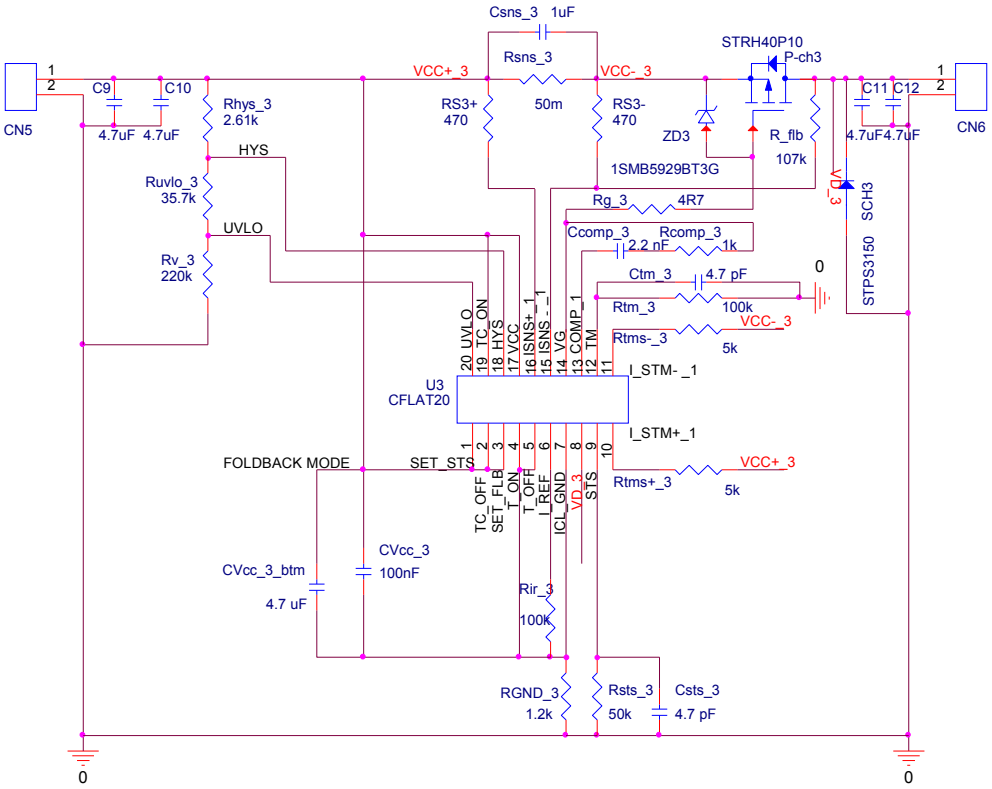
- Telecommand interface: disabled (TC_ON and TC_OFF both connected to V_{CC})
- SET_STS is connected to V_{CC} (ON at start-up)
- SET_FLB is connected to V_{CC} (foldback mode enabled)
- TON and TOFF are connected to GND

The external components of the board are pre-set to accomplish the following features:

- V_{CC} = 22 V with V_{TH_ON} = 18 V and V_{TH_OFF} = 17 V
- V_{HYS} = 1 V
- I_{LIM} = 2 A
- I_F = 100 mA

The evaluation board schematic is shown below. Please note that the capacitor Csns_3, connected in parallel to the R_{SENSE}, affects the dynamic of the reaction time and therefore the decision whether to mount it or not is up to the application needs of the end user.

Figure 18. **Foldback evaluation board (schematic)**



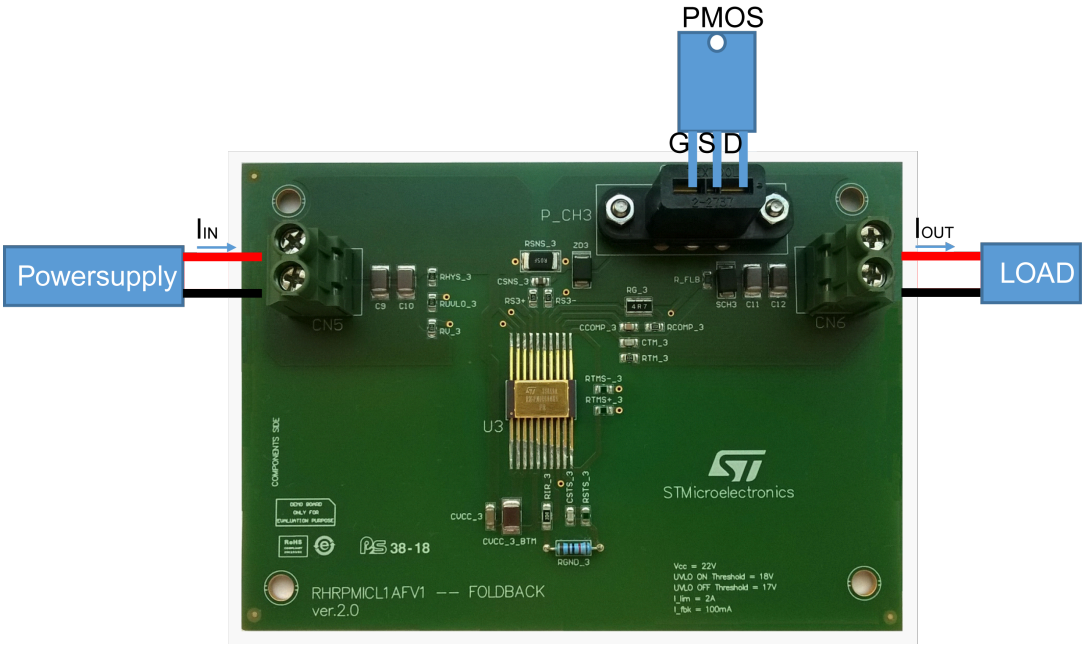
5.2 Operations

5.2.1 Power-on and testing environment

Connect a 22 V power supply to CN5, the load on CN6.

The telecommand section is not activated in this evaluation board. The analog and digital telemetries are accessible on the R_{TM} and R_{STS} resistors respectively.

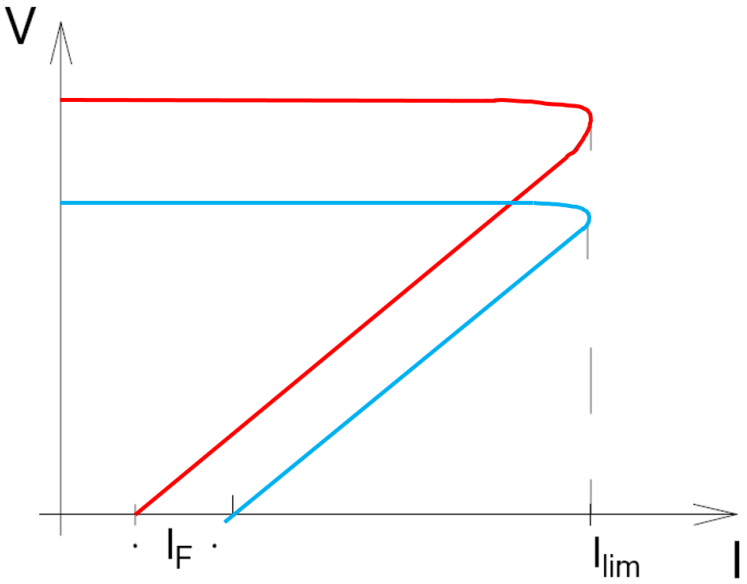
Figure 19. **Testing environment**



5.2.2 Current limit and foldback current programming

The V-I characteristic of a foldback current limiter developed with the EVAL-RHRICL1FV1A evaluation board is shown below (two curves are depicted, showing the foldback characteristics for two different values of I_F):

Figure 20. **Foldback current limiter characteristic**



This behavior is obtained by adding two sensing resistors RS3+ and RS3- between the R_{SENSE} terminals and ISNS+ and ISNS- pins of the RHRPMICL1A device. In addition, the foldback resistor R_{FLB} is connected between the power MOSFET drain and ISNS- pin.

Thanks to this sensing network, the output current in foldback mode, referring to Figure 20. Foldback current limiter characteristic, is given by:

$$I = \frac{(V_{CC} - V_F) - (R + R_{FLB})^{*}I_{FLB} - (R + R_{SENSE})^{*}I_{RS}}{R_{SENSE}} \quad (11)$$

where:

- V_F is the output voltage of V/I characteristic of Figure 20. Foldback current limiter characteristic (0 V in case of a short-circuit condition)
- "I_{RS}" is a design parameter referring to the input current of the current sense amplifier, having a typical value of 500 µA
- R=RS3+=RS3-
- I_{FLB} is the current flowing through the foldback resistor R_{FLB} and whose value is given by:

$$I_{FLB} = \frac{(VCC - V_F) - R^*I - 0.1}{R_{FLB}} \quad (12)$$

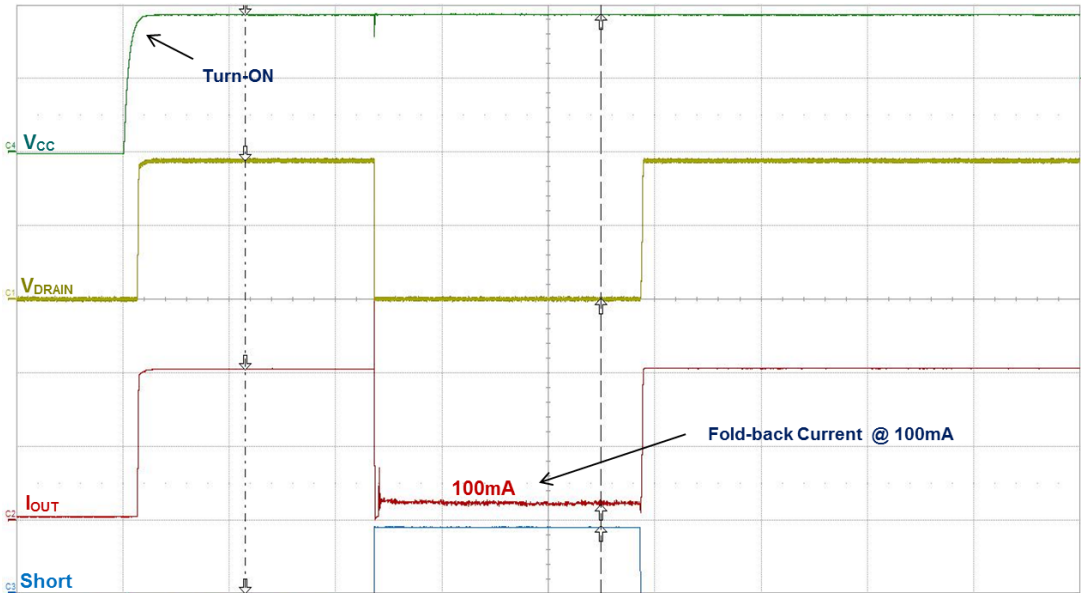
Of course, in case of output short-circuit condition, V_F = 0 V and I = I_F, i.e. the small and safe value (see Figure 20. Foldback current limiter characteristic) reached when a short-circuit on the load side occurs and persists.

The Eq. (11) and Eq. (12) are intended as a theoretical support to estimate the foldback current I (or IF) and do not take into account the variation due to external component accuracy and matching, as well as the standard process variations. Trimming on the final application is necessary.

In order to obtain the best results, it is recommended to use well-matched high precision resistors (0.1%) for RS3+ and RS3- and R_{FLB}.

The typical behavior of the device configured in latched mode is depicted below (timing is not in scale).

Figure 21. Foldback mode diagram



5.3 Evaluation board layout and BOM

5.3.1 Layout of the EVAL-RHRICL1AFV1 board

Figure 22. EVAL-RHRICL1AFV1 top layout

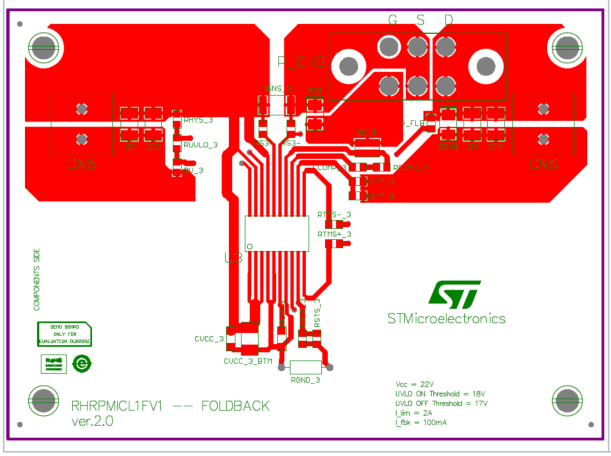
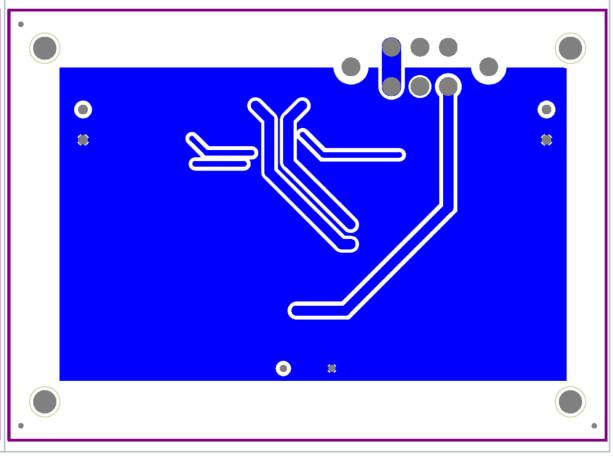


Figure 23. EVAL-RHRICL1AFV1 bottom layout



5.3.2 Bill of material of the EVAL-RHRICL1AFV1 board

Table 6. Bill of material

Item	Qty	Reference	Part / value	Voltage current	Manufacturer	Manufacturer code	More info	Footprint package
1	2	CN5, CN6	2-pin screw connector	Pitch 6.35 mm	Phoenix contact	1714955	Input (CN1) and ouput (CN2) connectors	TH
2	4	C9, C10, C11, C12	4.7 µF capacitor	100 V	TDK	C4532X7S2A475M	X7S	1812
3	1	CVcc_3_btm	4.7 µF capacitor	100 V	TDK	C4532X7S2A475M	X7S	1812
4	1	CVcc_3	100 nF	100 V	MULTICOMP	MCCA000490	X7R	1206
5	1	Csns_3	1 µF	10 V	KEMET	C0805C105K8NACTU	X8L	0805
6	1	Ccomp_3	2.2 nF	50 V	AVX	08055C222JAT2A	X7R	0805
7	2	C_TM_3 C_STS_3	47 pF	50 V	KEMET	C0805C470J5GACTU	NPO	0805
8	1	Rv_3	220 kΩ 0.125 W	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA6AEB224V		0805
9	2	Rtms+_3, Rtms-_3	5 kΩ 0.200 W	150 V, 0.1%, 5 ppm/°C	Vishay thin film	PNM0805E5001BST5		0805
10	1	Rtm_3	100 kΩ 0.125 W	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA6AEB104V	I=20 µA	0805
11	1	Rsts_3	50 kΩ 0.200 W	100 V, 0.1%, 25 ppm/°C	Vishay	PNM0805E5002BST5	I=100 µA	0805
12	1	RGND_3 (R_floating)	1.2 kΩ 0.600 W	1%	Vishay	MBB02070C1201FCT00	I=2 mA	TH
13	1	Rg_3	4.7 Ω 1 W	200 V, 1%	Panasonic	ERJB1BF4R7U		1020
14	1	R_flb	107 kΩ 0.100 W	0.1 W, 0.1% ± 25 ppm/°C	Multicomp	MCTC0525B1073T5E		0805
15	1	Rsns_3	50 mΩ 1 W	1W, 1% ± 75 ppm/°C	Vishay DALE	WSL2512R0500FEA		2512

Item	Qty	Reference	Part / value	Voltage current	Manufacturer	Manufacturer code	More info	Footprint package
16	2	RS3+ RS3-	470 Ω 0.125 W	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA6AEB471V		0805
17	1	Rhys_3	2.61 kΩ 0.100 W	100 V, 0.1%, 25 ppm/°C	TE CONNECTIVITY	RN73C2A2K61BTDF		0805
18	1	Ruvlo_3	35.7 kΩ 0.100 W	100 V, 0.1%, 25 ppm/°C	TE CONNECTIVITY	RN73C2A35K7BTDF		0805
19	1	Rcomp_3	1 kΩ 0.125 W	0.1%, 25 ppm/°C	Panasonic	ERA6AEB102V		0805
20	1	Rir_3	100 kΩ 0.250 W	100 V, 0.1%, 25 ppm/°C	Panasonic	ERA8AEB104V	I=10 µA	1206
21	1	ZD3	Zener	15 V, 3 W	ON Semiconductor	1SMB5929BT3G	Zener	SMB-CASE403A
22	1	SCH3	STPS3150	3 A, 150 V	ST	STPS3150U	Diode 100 V -5 A	SMB
23	1	P_ch3 SOCKET	P-ch TO254 AA socket (STRH40P10)	34 A 100 V	3M TOUCH SYSTEMS	203-2737-55-1102	P-channel, B_{Vdss} 100 V, Id 48 A, $R_{DS(on)}$ 60 mΩ, Qg 162 nC	TO-254 AA
24	1	U1	ICL001		ST			FLAT20

Revision history

Table 7. **Document revision history**

Date	Version	Changes
24-Jul-2019	1	Initial release.
16-Sep-2019	2	Minor text changes.

Contents

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