Nucleo144 H7 SMPS with STLINK V3

MB1363

H755ZIQ

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Legend

General comment such as function title, configuration, ...
Text to be added to silkscreen.
Warning text.
Notes to generate the board layout.

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SB should be placed close to the MCU to avoid stub on CLK lines.

Place capacitor close to MCU pad.
MCU PWR SUPPLIES

MCU DECAPS
Ceramic capacitor (Low ESR, ESR<1ohm)

SMPS MCU Supply Config

Supply Config 1 : LDO only (SMPS OFF, LDO ON)
Disconnect V3_SMPS_IN from V3_MCU
Connect V3_SMPS_IN to GND
Connect VDD_SMPS_IND_OUT to GND
Connect VDD_LDO to 3V3_MCU
2 x 2.2μF near VCAP pins/plans

Supply Config 2 : Internal SMPS only (SMPS ON, LDO OFF)
Default config
Connect VDD_SMPS_IND_OUT to VDD_MCU
Connect VDD_SMPS_IND_OUT to VCAP1/2/3
Connect VDD_LDO to 3V3_MCU
Connect 3V3_SMPS_IN to GND

Supply Config 3 : SMPS & LDO cascaded (SMPS & LDO ON)
Compared to config 2 :
Disconnect VDD_SMPS_IND_OUT from VCAP
Connect VDD_SMPS_IND_OUT to VDD_LDO
Add 2x100nF near VDDLDO pins/plans
Add 2x2.2μF near VCAP pins/plans (see config 1)

Supply Config 5 : external SMPS
Disconnect V2_MCU from VDD_SMPS_IND_OUT
Connect V2_MCU to V2_VOUTCORE (Connectors page)
**STLINK_V3E**

**Title:**

**Size:**

**Reference:**

**Sheet:** of A3

**Revision:**

**Project:** Nucleo144 H7 SMPS with STLINK V3

- MB1363D...to pin 1
- Connector must be on the border of the PCB
- Pin attributions on ESD can be swapped for layout optimisation

**STDC14 Receiver**

- PIX101 PIX102
- VDD
- PICN107
- PICN105
- PICN1010
- PICN106
- PICN102

**ST-LINK USB CONNECTOR**

- USB_Micro-B receptacle (must be same length and must be Shielded).
- Specific constraints for T_SWDIO and T_SWCLK (must be same length and must be Shielded).

**ST-LINK POWER**

- 33V_sts
- 3V3_STLK
- HSE CLK STLINK

- level shifter 1V8/3V3
- 47ohm resistors to Target MCU to avoid stub noises and from ST-LINK to 47ohm resistors and from

**3V3_STLK**

- Connector must be on the border of the PCB
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**USB_DEV_HS_P/PB15R15**

**USB_DEV_HS_N/PB14R14**

**STLK_SWDCLK/PA14A14**

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