Open Platform License Agreement

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The complete Open Platform License Agreement can be found on www.st.com/opla.
PSRAM

PSRAM Data, NWE & NOE shared with LCD

Impedance Constraint [Min = 40.00  Max = 60.00 ]
Matched Net Lengths [Tolerance = 5mm]

Place close to PSRAM
Optional PU and PD to set PB2 when use in BOOT1 alternate function

Exposed central pad should not be connected to any voltage on PCB

Matched Net Lengths [Tolerance = 5mm]
FRIDA LCD

Top side: layout of CN16

Capacitive Touch Panel

- LCD RST and CTP RST share the same PIO for RST. Active LOW
- SB41 open and SB42 closed: 5V HIGH. LCD in 16bit mode
- SB41 closed and SB42 opened: 3V LOW. LCD in 8bit mode

VDD_MCU operating voltage range: 3.0V to 3.6V

LCD Backlight

Common mode supply filter

Layout: Interfaces to ST D4D and grouped in same area with BL/GND as local ground plane
USB Full Speed operating range voltage: 3.0V>VDD_USB<3.6V

ESD PROTECTION SHOULD BE CLOSE TO THE CONNECTOR
Connect only one jumper to supply the DISCO from one of the external 5V. If the DK board is connected to an external 220V/5V USB Charger, use jumper on pin 7/8.

**5V PWR SELECTION FROM EXTERNAL SOURCES**

**5V PWR FROM ARDUINO (VIN < 11.5V)**

Output: 5V / Up to 800mA

From Arduino power pin

**3V3 PWR**

Output: 3V3 / Up to 800mA

Open solder bridge if Discovery is supplied from +3V3 of extension connector

**GND PROBE**