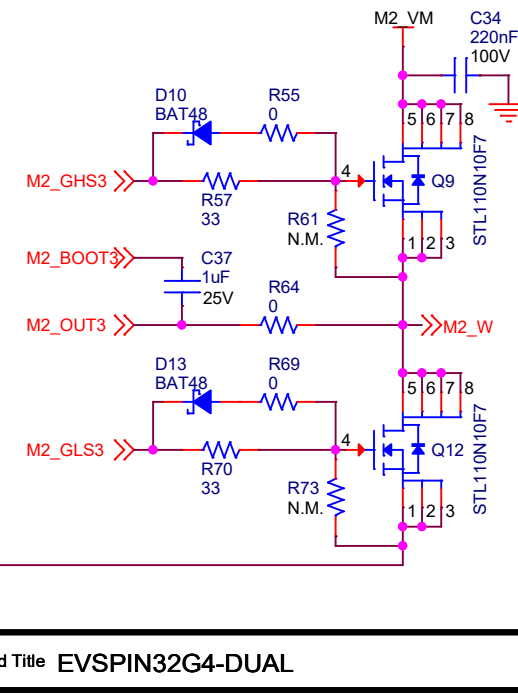
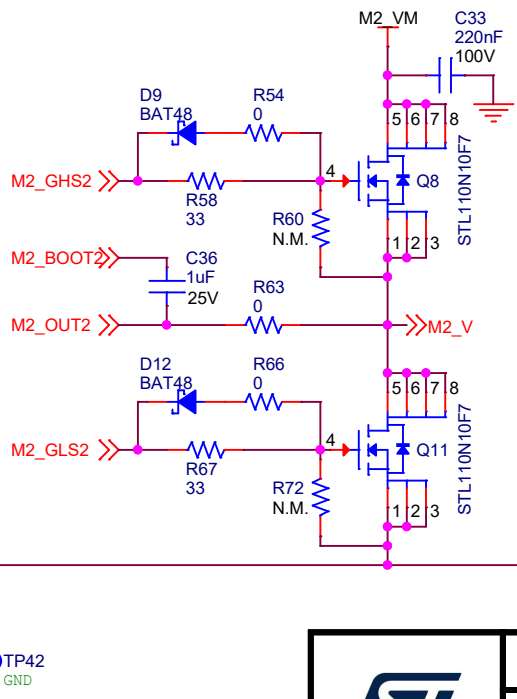
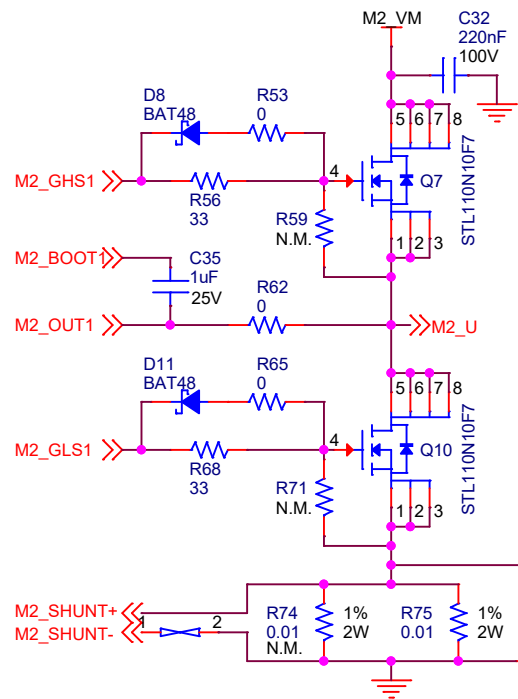
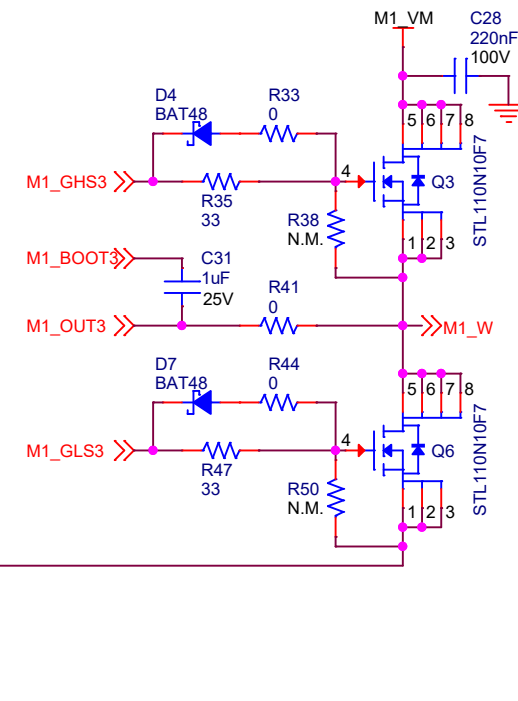
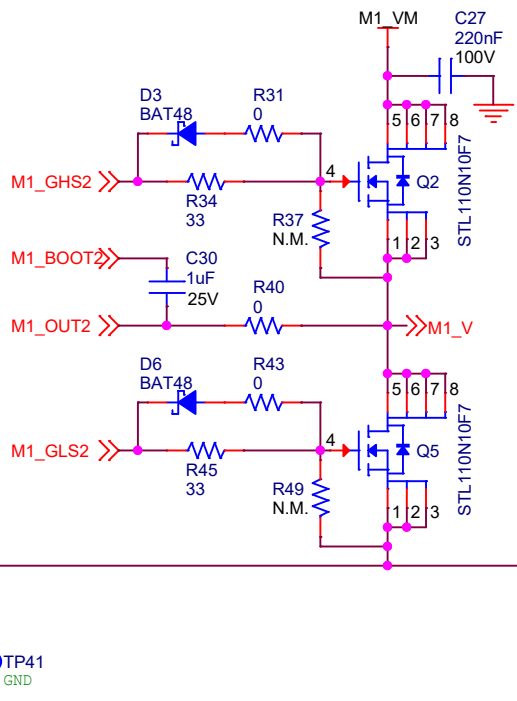
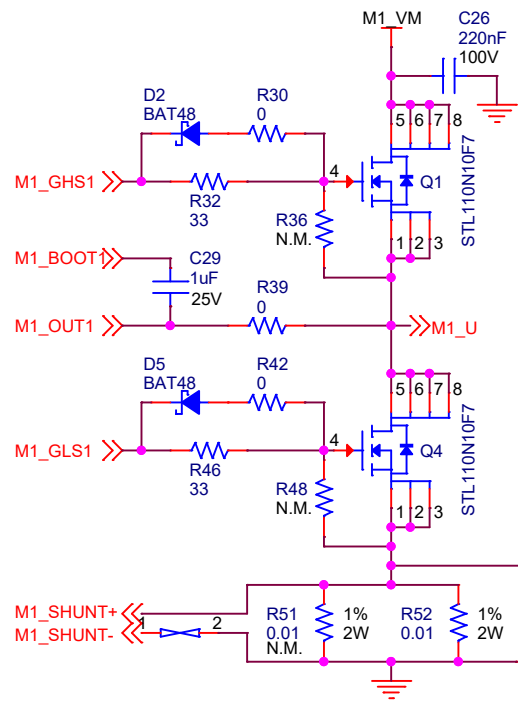

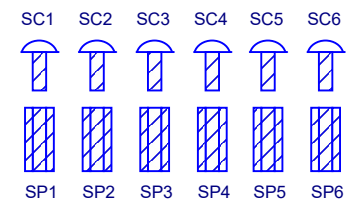
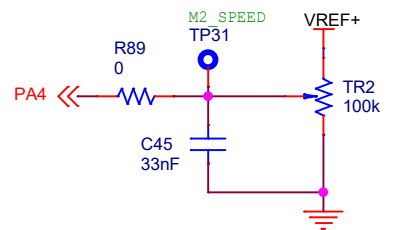
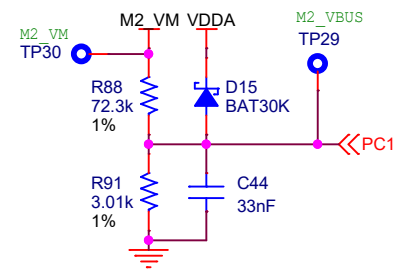
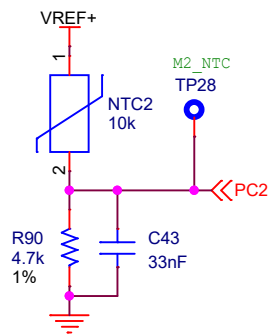
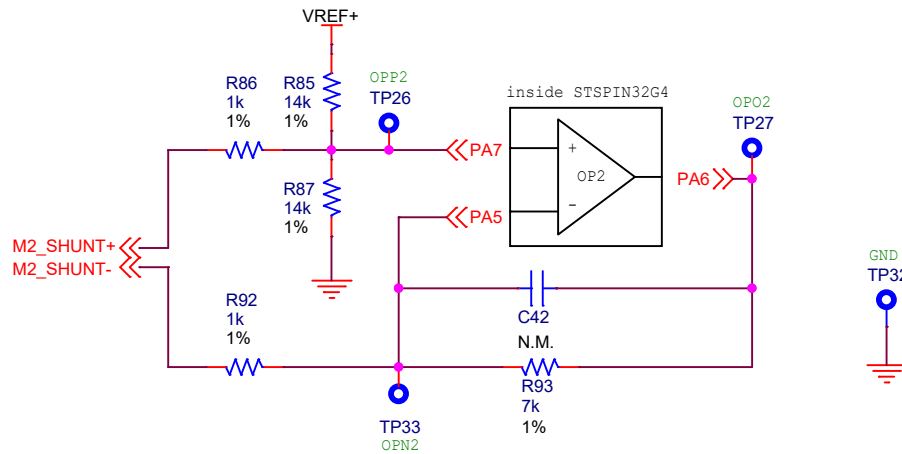
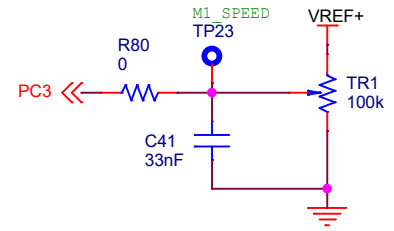
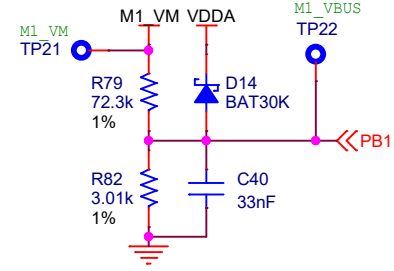
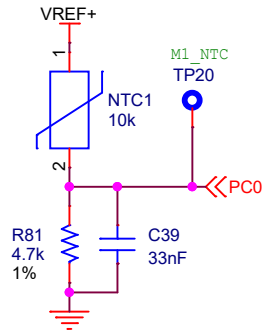
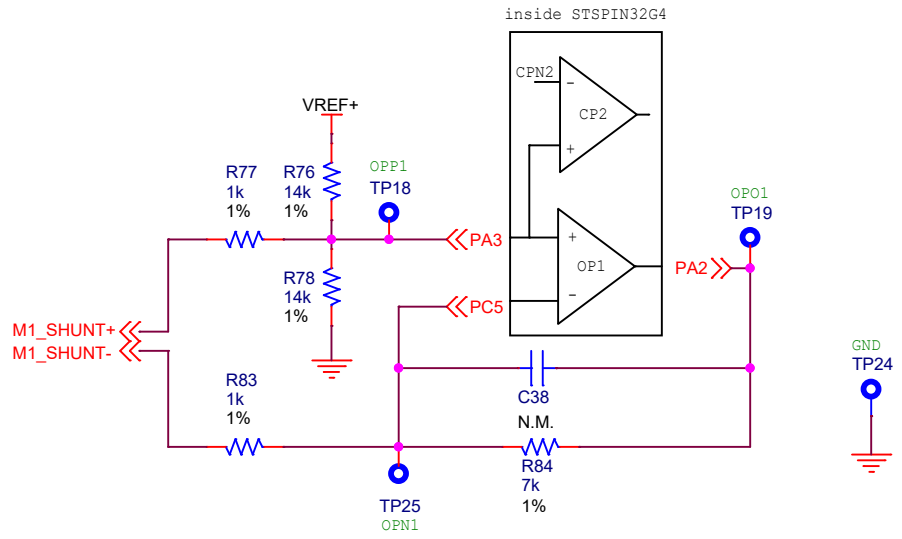

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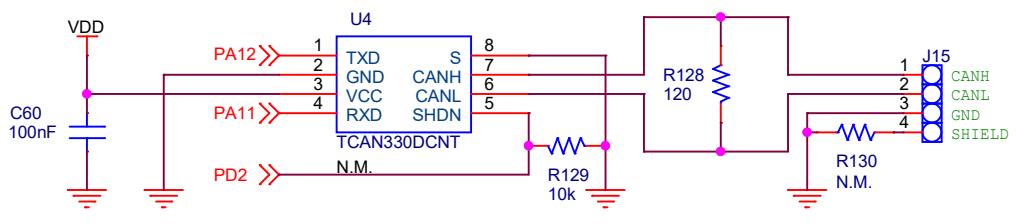
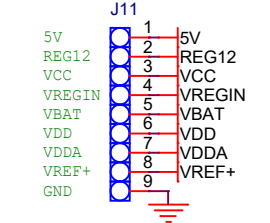
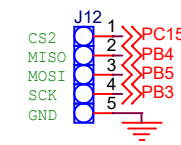
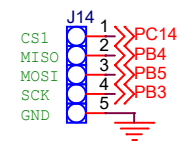
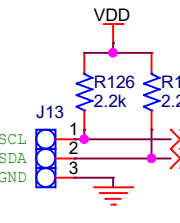
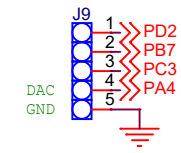
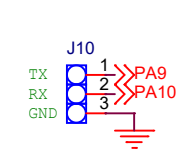
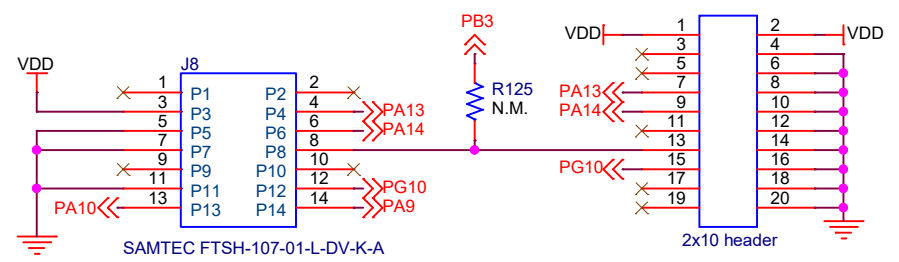
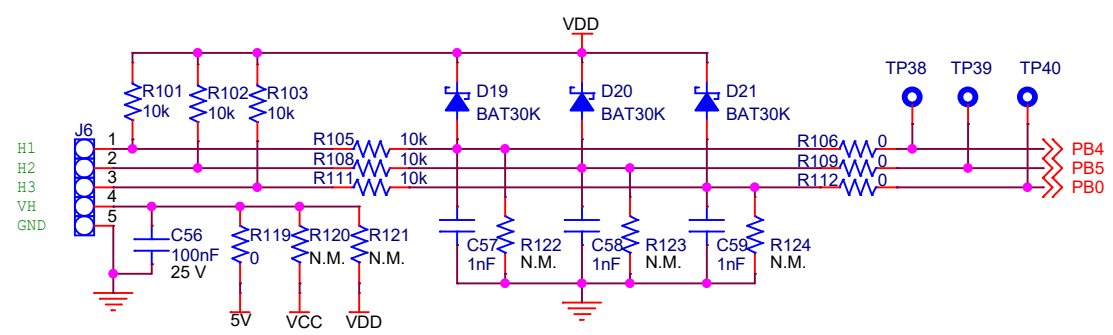
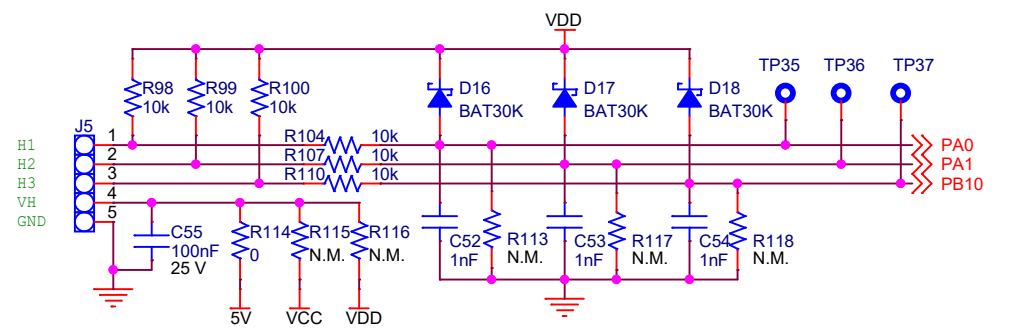
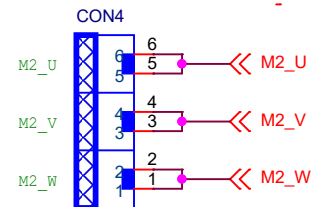
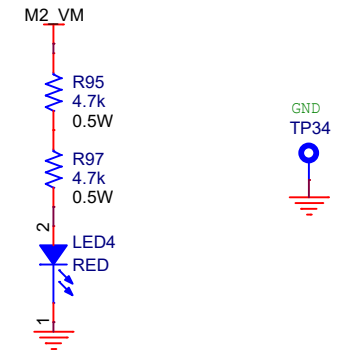
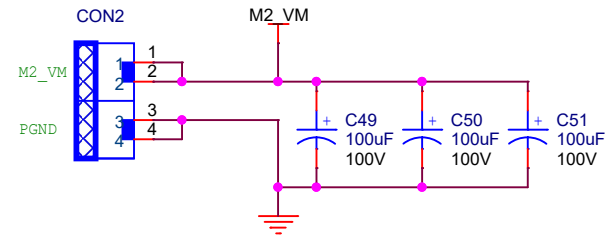
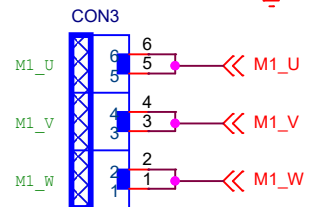
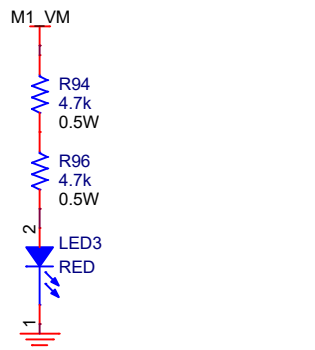
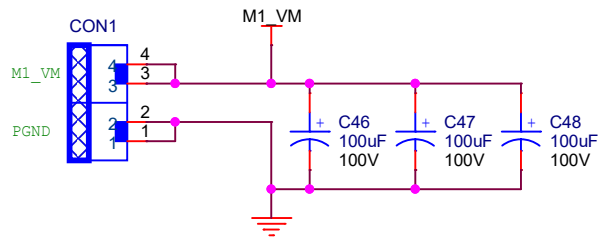
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	Sheet Title Analog				
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	Sheet Title Inputs Outputs			
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