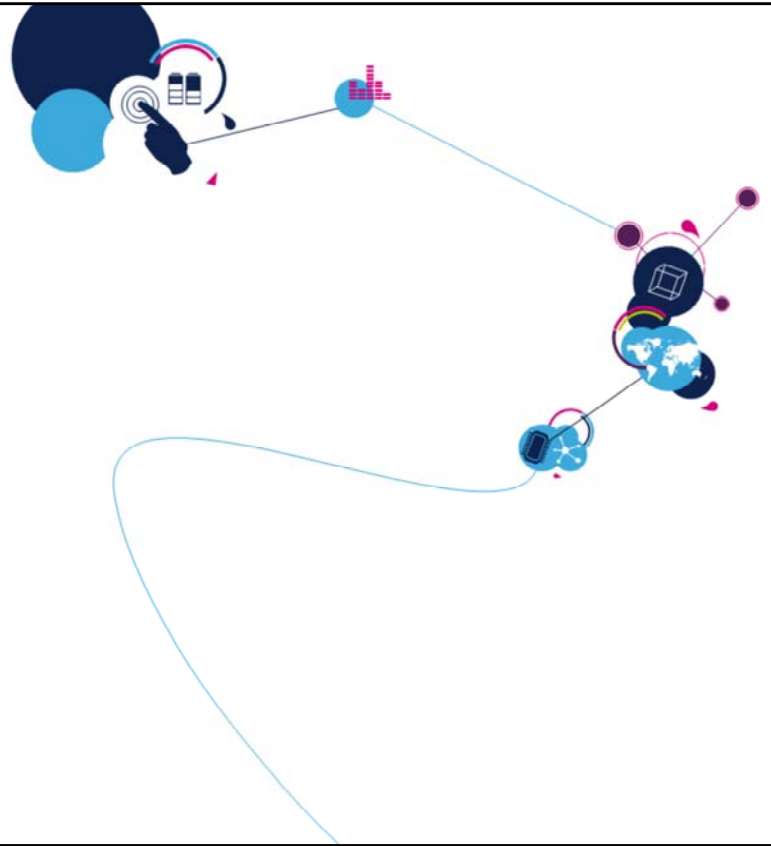


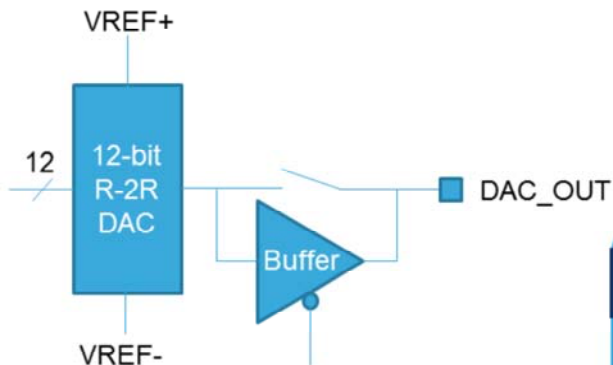
# STM32L4 - DAC

Digital-to-Analog Converter

Revision 3.1



Hello, and welcome to this presentation of the STM32L4 digital-to-analog converter. All the features of this analog block will be presented, which is used to convert digital signals to analog voltages which can interface with the external world.



- Provides digital data to analog output conversion
  - 8- or 12-bit modes
  - Two DAC modules (only 1 on STM32L45x/46x devices)
  - Low-power Sample & Hold mode

### Application benefits

On-chip DAC can control the external bias circuitry; replacing potentiometers. It can also serve as a voice and arbitrary signal generator.

The digital-to-analog converter on STM32L products ensures the conversion of 8- or 12-bit digital data to the analog voltage. Two DAC modules are embedded in the STM32L4 devices, except on STM32L45x/46x devices where only 1 DAC is implemented.

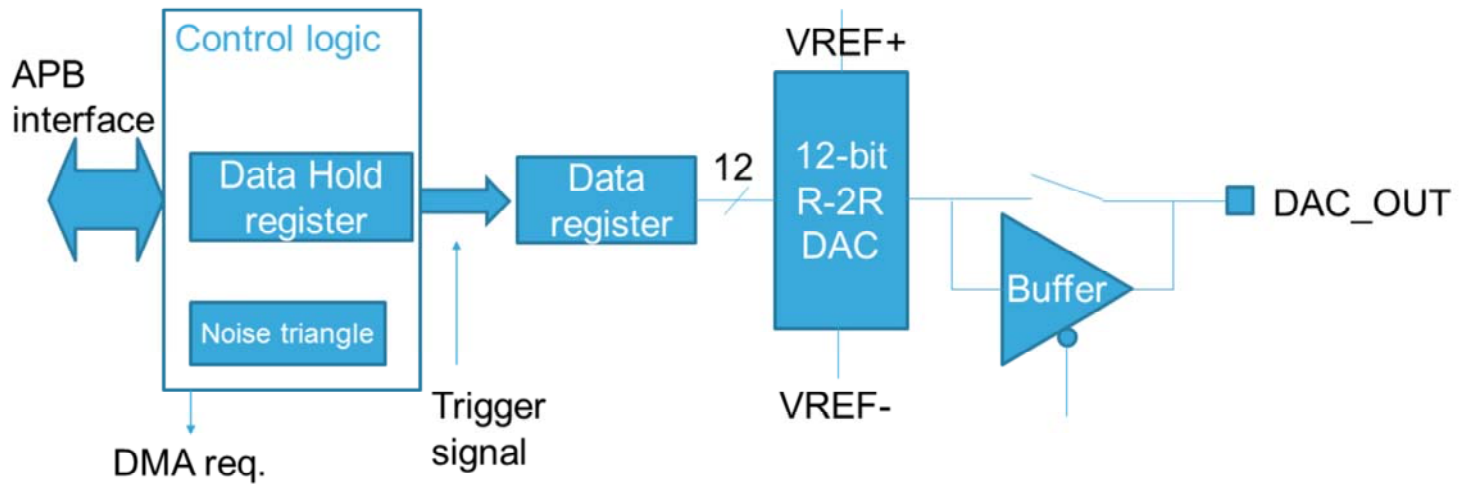
A low-power Sample and Hold mode is also integrated. The DAC can interface with external pots or bias circuitry. It can also create voice and arbitrary signals.

- 8- or 12-bit mode
  - 10-bit monotonicity guaranteed
- Buffered output
- Sample and Hold mode for low-power applications
- Synchronized update capability
- DMA capability
- Several trigger inputs
- Noise-wave, triangular-wave generation



The digital-to-analog converter inside STM32L4 products offers simple digital-to-analog conversion in an 8- or 12-bit mode; 10-bit monotonicity is guaranteed. The DAC output can have a low impedance buffer to drive external loads. Its Sample and Hold mode can reduce power consumption significantly. Two DACs can be synchronized with each other. The input data can be transferred by DMA which offloads the CPU. The DAC output data can be updated by a timer or an external trigger as well as a software trigger. It also integrates small logic to generate noise waves as well as triangle waves.

## Block diagram 4



X2 (except on STM32L45x/46x devices)

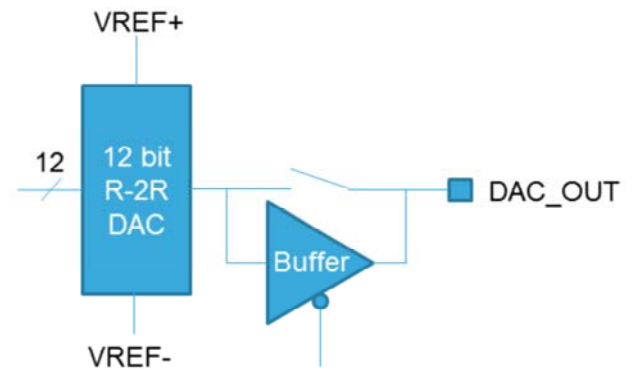
Here you can see the simplified block diagram of the digital-to-analog converter. The STM32L4 integrates 2 of them except on STM32L45x/46x devices where only 1 DAC is implemented.

# DAC with output buffer 5

## • Easy to interface with different configurations

### • Output

- Low impedance output using buffered mode
- Raw output from the R-2R type resistor ladder DAC
  - Output impedance is  $\sim 12\text{ k}\Omega$



The DAC output can be buffered for low impedance loads. When unbuffered, the output is directly connected to the R-2R resistor ladder network type of DAC.

## Flexible data input formats

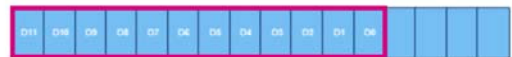
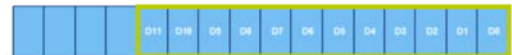
- 8-bit mode:

- Right-aligned data input (on 16-bit data register)
- 8-bit + 8-bit data input for Dual Channel mode



- 12-bit mode:

- Right-aligned data input (on 16-bit data register)
- Left-aligned data input (on 16-bit data register)



The DAC can support different input formats. In 8-bit mode, it's a right-aligned 8-bit data format. In Dual channel mode, it's an 8 bit plus 8 bit data format, in order to provide input data for two DAC simultaneously. In 12-bit mode, either a right- or left-aligned mode can be used for input data.

# DAC conversion triggers 7

## Several triggers for starting the DAC

- Automatically by writing to the Data Hold register
- By a triggered conversion:
  - 6 different timer outputs
  - External I/O trigger
  - Setting the software trigger bit



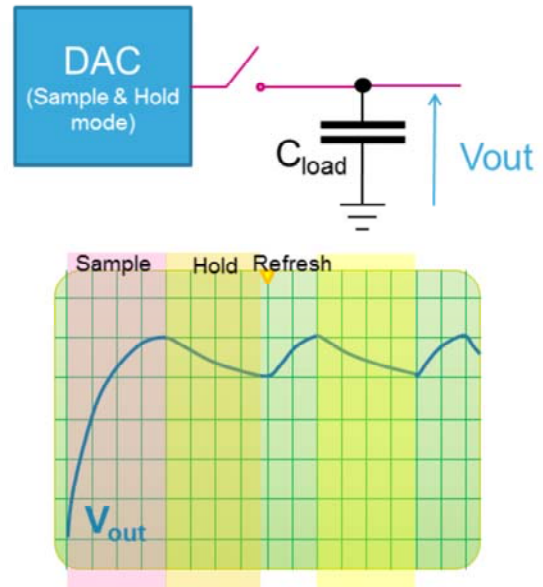
DAC output conversion is started by writing to the Data Hold register by software. 6 different timer outputs, an external I/O or software can trigger the DAC conversion.

# Sample and Hold feature

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## Low power mode

- “Sample & Hold” feature is available for extremely low power requirements.



The digital-to-analog converter has a Sample & Hold mode feature. The DAC can work intermittently, charge the external or internal capacitor, and be powered down while the output voltage is kept on the hold capacitor. After a certain period, the DAC is powered back on again and recharges the hold capacitor.

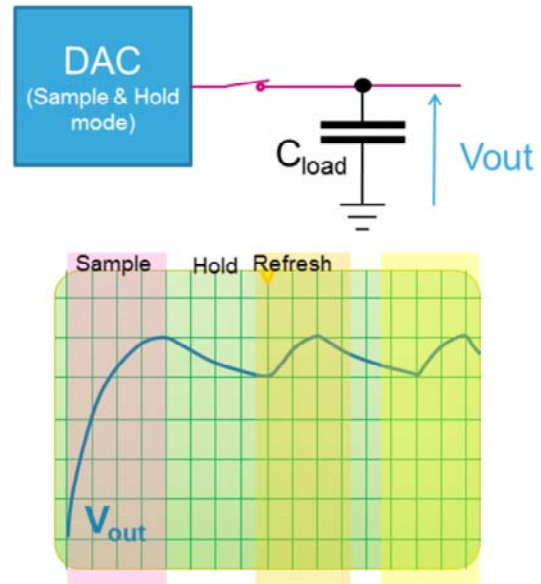


# Sample and Hold feature

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## Low power mode

- “Sample & Hold” feature is available for extremely low power requirements.
- When the DAC is configured in “Sample & Hold” mode, it is able to generate its converted output voltage, and active circuitry can be turned off.



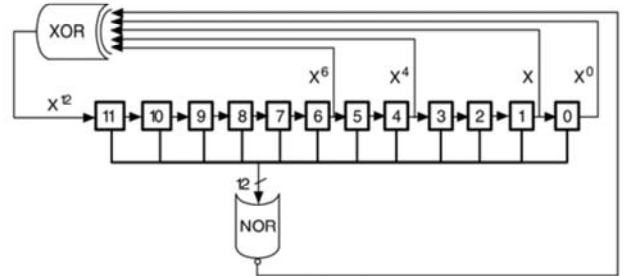
By doing so, the DAC is only active during very low duty cycles; resulting in very low power consumption. The duty cycle program is very flexible and autonomous.

# Noise and triangle wave generation 10

## Several wave generation

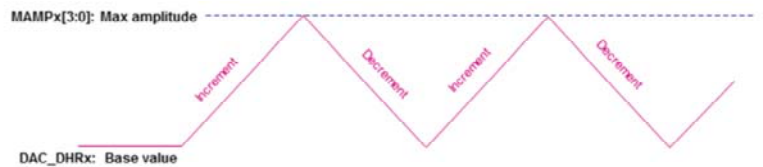
- Noise generation

- Based on the LFSR (linear feedback shift register)
  - Initial value = 0xAAA
  - Calculated noise value is added to the Data Hold register without overflow using an external trigger



- Triangle generation

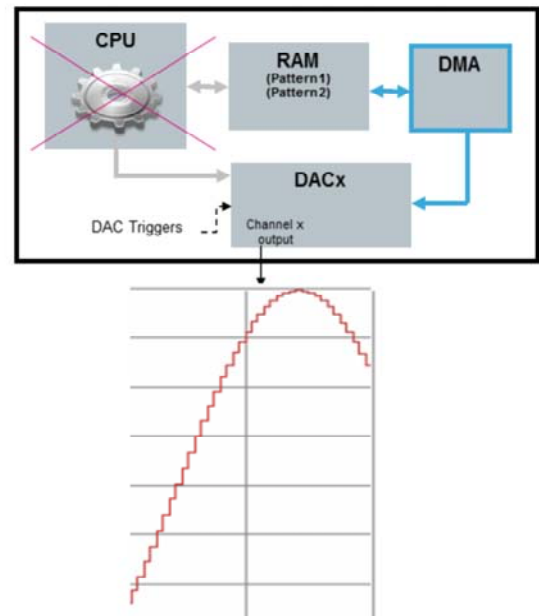
- Based on the up-down counter, a triangle waveform can be generated (each trigger increments a +/- 1 step)



The DAC digital interface integrates two special signal generators. The Linear Feedback Shift register can create the noise signal for the DAC input. Each trigger updates the DAC output data by an LFSR block. The up-down counter with a programmable count value can create triangle wave data which can update the DAC output data. The data can also be updated by a trigger signal.

## Offloads the CPU

- The DAC DMA request is generated when an external trigger occurs:
  - The Data Hold register value is then transferred to the Data Output register.
  - DMA underrun with interrupt capability
  - Can generate a stable sampling time based output (timer controlled)



The DAC can also create DMA requests from the trigger signal. Once a trigger is detected, the Data Hold register value is then transferred to the Data Output register. Then the DMA request is generated to obtain the new data for the Data Hold register. As the update of the Output Data register is initiated directly by the trigger signal, the DAC output signal will not have jitter, so that it can create a stable sampling time signal output, making it easy to filter out the sampling frequency.

# Interrupts and DMA 12

Interrupt event	Description
DMA underrun	When a DMA request is not processed by the next external trigger

DMA event	Description
DMA request	External trigger when the DMAENx bits are set

The DAC can generate a DMA underrun interrupt. To transfer data from memory, a DMA request can be generated.

# Low-power modes

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Mode	Description
Run	Active.
Sleep	Active.
Low-power Run	Active.
Low-power Sleep	Active.
Stop 0/Stop 1	Active.
Stop 2	Not available. Contents of peripheral registers are kept.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.
Shutdown	Powered-down. The peripheral must be reinitialized after exiting Shutdown mode.



The digital-to-analog converter is active in the following low-power modes: Run, Sleep, Low-power run, Low-power sleep, Stop 0 and Stop1.

In Stop2 mode, the DAC is not available, but the content of its registers is kept. In Standby or Shutdown modes, the DAC is powered-down and it must be reinitialized afterwards.

	Condition	Value (typical)	Unit
VDDA		1.8 ~ 3.6	V
Monotonicity		10	bits
DNL		+/- 2	LSB
INL		+/- 4	LSB
ENOB	1 kHz output	11.4	bits
	Differential	10.9	bits
Consumption	Buffer on	185	uA
	Buffer off	155	uA
Settling time	+/-1 LSB (Buffer on) R = 5 kohm, C = 50 pF	1.7	usec
Sampling rate		1.0	Msample/s



The following table shows some performance parameters for the digital-to-analog converter. The DAC can work between 1.8 and 3.6 volts. 10-bit monotonicity is guaranteed. Power consumption is 185  $\mu$ A when the buffer is enabled and 155  $\mu$ A when the buffer is disabled. By using Sample & Hold mode, the current consumption can be drastically reduced. Depending on the condition and the hold capacitor characteristics, less than 1  $\mu$ A current consumption is possible for this mode. The DAC buffered output has a settling time of 1.7  $\mu$ sec with 5 kohms and 50 pF load. The DAC can handle a sampling rate of 1 mega sample per second; when using external components, it can support up to 10 mega samples per second. This is described in detail in application note AN4566.

## Related peripherals 15

- Refer to these peripherals trainings linked to this peripheral, if any
  - DMA – direct memory access
  - Interrupts
  - GPIO – general purpose inputs and outputs
  - TIM – timers
  - ADC – analog to digital converter
  - COMP – comparators
  - Op Amp – operational amplifiers



This is a list of peripherals related to the DAC. Please refer to these peripheral trainings for more information if needed.

- For more details, please refer to following sources
  - AN3126: Audio and waveform generation using the DAC in STM32 microcontrollers
  - AN4566: Extending the DAC performance of STM32 microcontrollers

Application notes dedicated to DAC topics are also available.