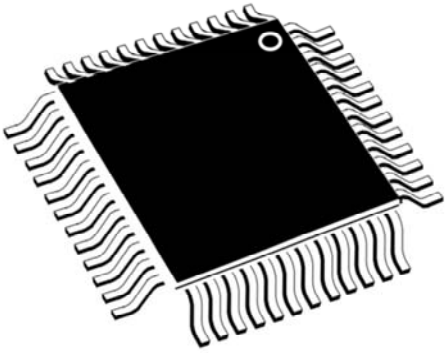
Hello, and welcome to this presentation of the STM32 general-purpose IO interface. It covers the general-purpose input and output interface and how it allows connectivity to the environment around the microcontroller.

Overview

- Provides interface for interaction with external environment
  - Fully configurable
  - With interrupt and wake-up capability
  - Direct connection to AHB2 bridge



Application benefits

- Direct Microcontroller wake-up
- Supports a wide range of supply voltages
- Direct connection to AHB2 allows fast toggle response

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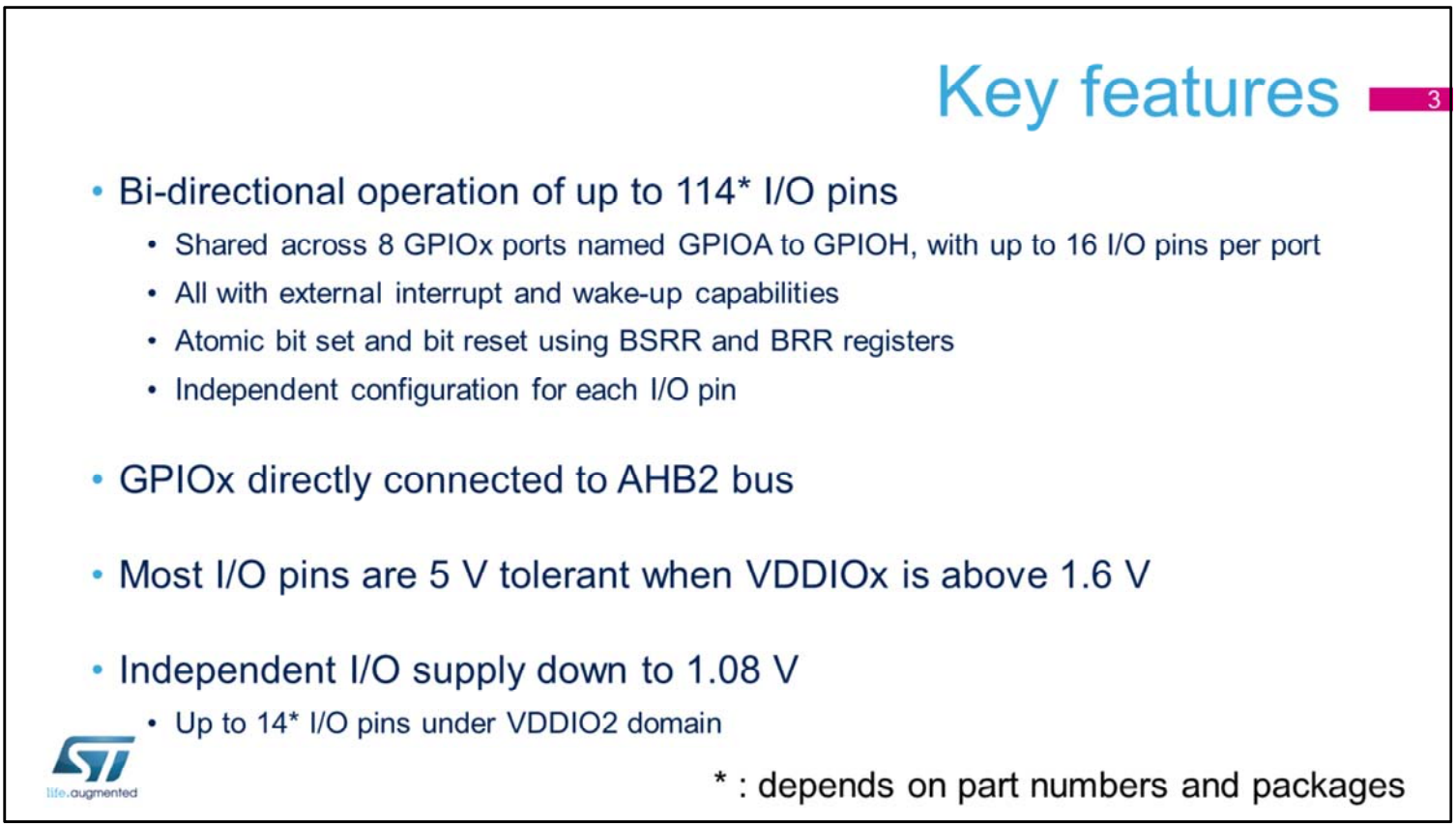
General-purpose IO pins of STM32 products provide an interface with the external environment. This configurable interface is used by the MCU and also all other embedded peripherals to interface with both digital and analog signals. Application benefits include a wide range of supported IO supply voltages, as well as the ability to externally wake up the MCU from low power modes.



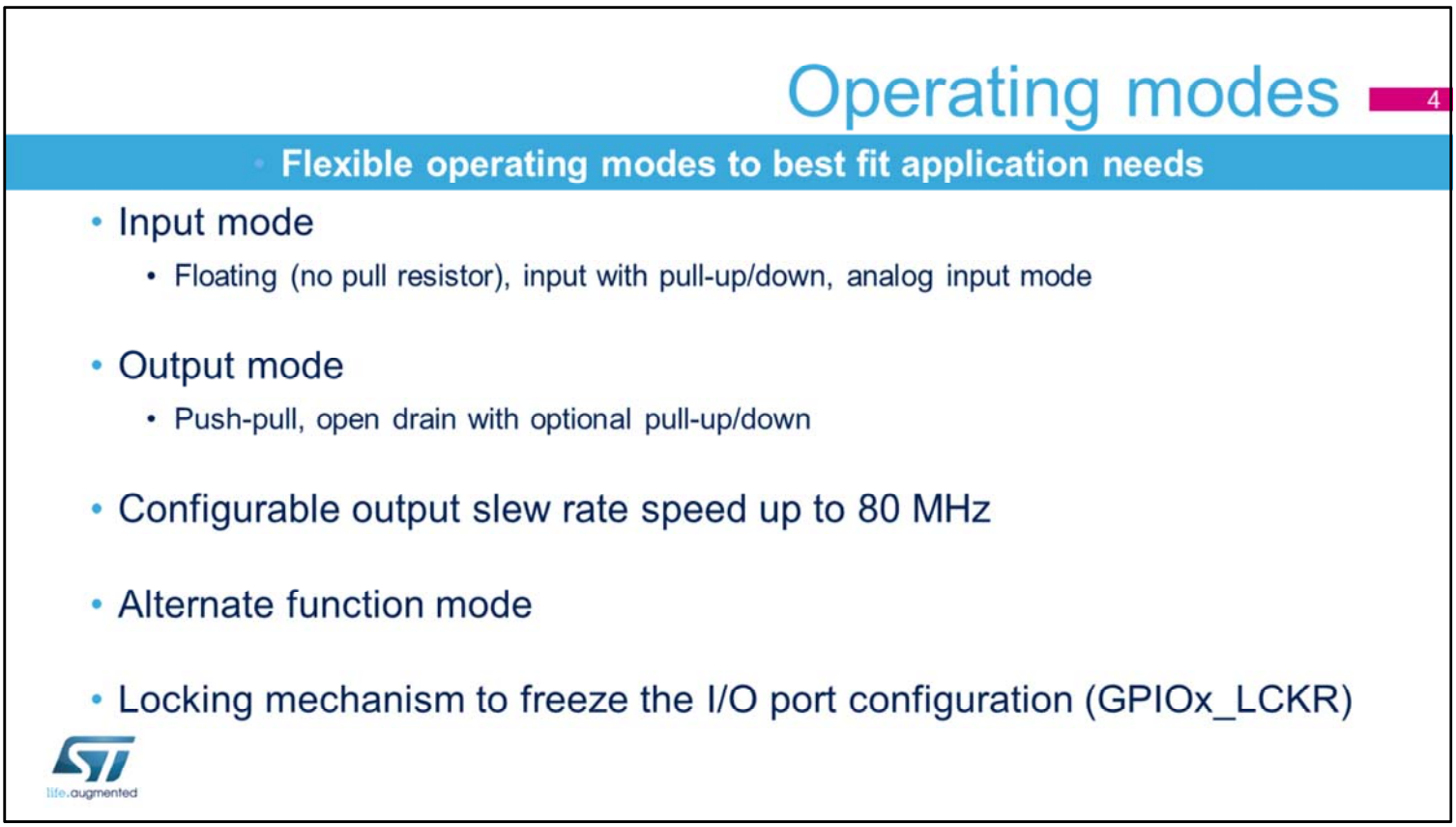
General-purpose I/O provides bidirectional operation – input and output – with independent configuration for each I/O pin. They are shared across up to 9 ports named GPIOA to GPIOI, each of them hosting up to 16 I/O pins. I/O ports support atomic bit set and reset operation through BSSRR and BRR registers and support the use of bit banding in the memory map.

I/O ports are directly connected to the AHB2 bus. This allows fast I/O pin operations, e.g. toggling of the pin every 2 clock cycles.

Most of the I/O pins are 5 V tolerant when supplied from VDDIOx above 1.6 V.

Up to 14 I/O pins are supplied by externally providing a voltage within the VDDIO2 supply domain. This supply is independent of the VDD provided to the part. This functionality allows users to adapt logic levels of the MCU's I/O pins to the levels required by external logic which may be supplied by different voltage domains without need for

external level shifters.

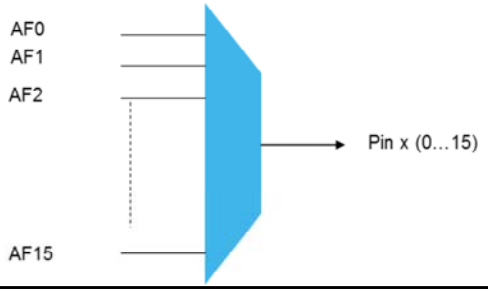


General-purpose I/O pins can be configured into several operating modes.
An I/O pin can be configured in an input mode with floating input, input mode with an internal pull-up or pull-down resistor or as an analog input.
An I/O pin could be also configured in an output mode with a push-pull output or an open-drain output with an internal pull-up or pull-down resistor.
For each I/O pin, the slew rate speed can be selected from 4 ranges to compromise between maximum speed and emissions from the I/O switching and adjust the application's EMI performance.
I/O pins are also used by other integrated peripherals to interface with the external environment. Alternate function registers are used to select the configuration for the peripherals in this case.
Configuration of the I/O ports can be locked to increase

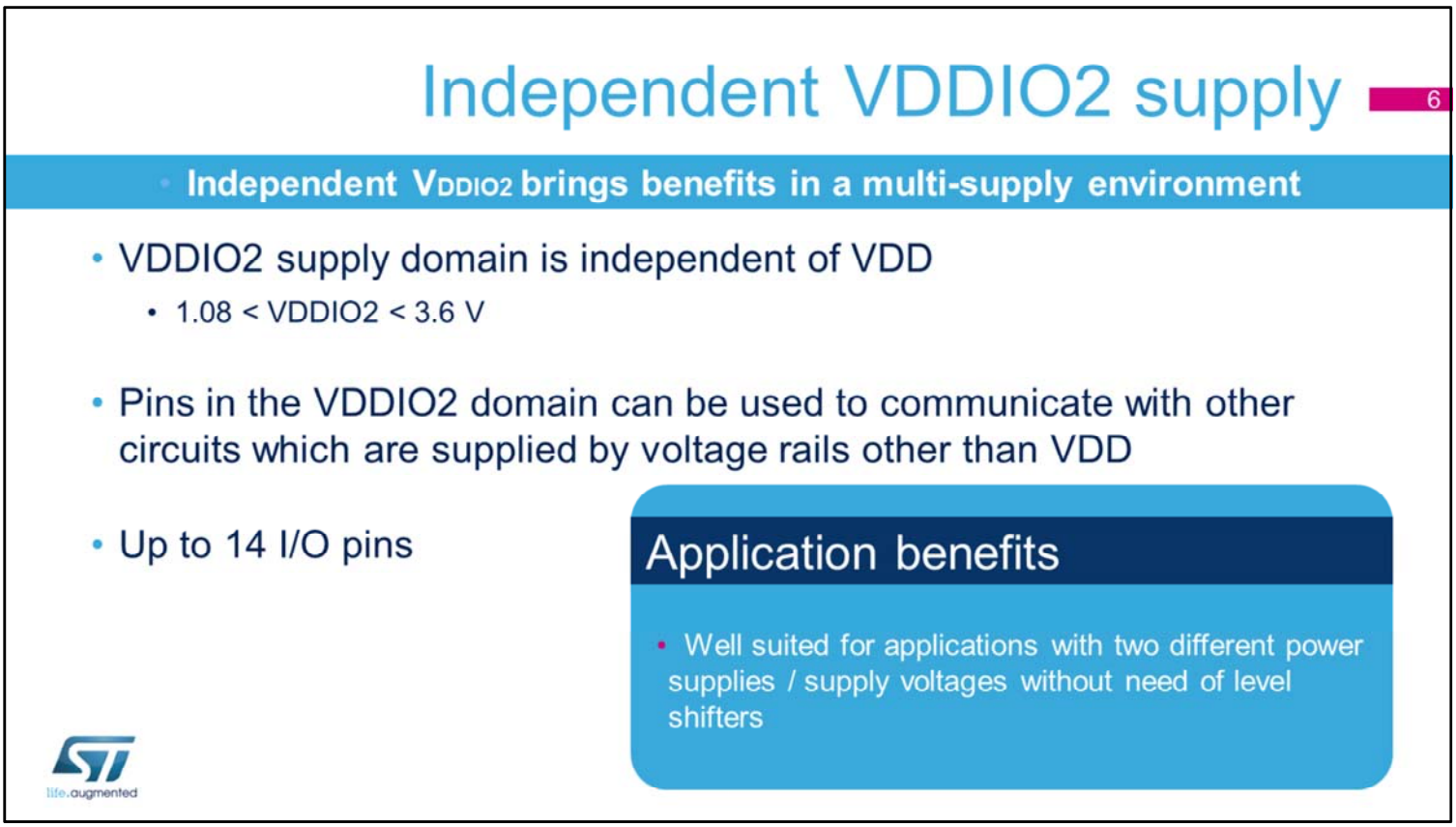
robustness of the application. Once the configuration is locked by applying the correct write sequence to the lock register, the I/O pin’s configuration cannot be modified until the next reset.

Alternate functions

- **Structure of I/O pins is used as interface by other embedded peripherals**
- Several integrated peripherals share the same I/O pins
  - Including USARTx_TX, TIMx_CHx, SPIx_MISO, EVENTOUT, ...
- Alternate function multiplexer selects the peripheral connected to the I/O pin
  - Only one alternate function is connected to a specific I/O pin at a single time
  - Configurable through the GPIOx_AFRL and GPIOx_AFRH registers



Several integrated peripherals such as the USART, timers, SPI and others share the same I/O pins in order to interface with the external environment.
Peripherals are configured through an alternate function multiplexer which ensures that only one peripheral is connected to the I/O pin at a single time. Of course, this selection can be changed during run time of the application through the GPIOx_AFRL and AFRH registers.



The Independent VDDIO2 supply domain allows operation in an environment with several different logic supply voltages. It allows the STM32 to communicate with logic supplied from 1.08 V, much lower than the VDD supply of the STM32, which can range up to 3.6 V.
Up to 14 I/O pins in this domain can be used to communicate with other logic circuits which are supplied by voltage rails other than VDD.
Independent voltage supplies may allow for the omission of external voltage shifters in the design.

Special considerations for I/O pins

Only debug pins remain in AF mode under reset

- During and after reset, the alternate functions (AF) are not active
  - I/O ports default to Analog mode
  - Saves current consumption during and after reset (Schmitt trigger is off)
- Only JTAG/SWD debug pins remain in AF pull-up/pull-down configuration
  - PA13: JTMS/SWDIO
  - PA14: JTCK/SWCLK
  - PA15: JTDI
  - PB3: JTDO
  - PB4: NJTRST

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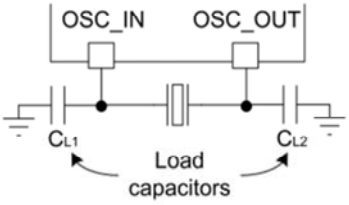
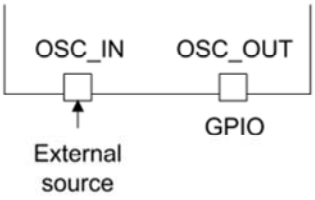
During and after reset, the alternate functions (AF) are not active, only debug pins remain in AF mode.
JTAG/SWD debug pins remaining in AF configuration mode are listed in this slide.

Special considerations for HSE/LSI pins

Oscillator pins can be used as standard I/O pins

- When the oscillator is switched OFF, related pins behave as I/O pins
  - Valid for both HSE / LSE
  - This state is the default one after reset
- When user external clock mode is used, the second pin behaves as an I/O pin
  - Only OSC_IN or OSC32_IN is used as clock source
  - OSC_OUT and OSC32_OUT are standard I/O pins





When the external oscillator is switched off, pins related to this oscillator can be used as standard I/O pins. This is the default state after device reset.
When the external clock source is used instead of a crystal oscillator, only related OSC_IN or OSC32_IN pins are used for the clock and OSC_OUT or OSC32_OUT pins can be used as standard I/O pins.

Analog switch control register

- **Special GPIOx_ASCR register present on STM32L47x/48x devices only**
- New GPIOx_ASCR control register is present on STM32L47x/48x devices
  - Used to enable an analog connection between an I/O pin and ADC input
  - Connection must be enabled before starting ADC conversions
  - Register will be removed on other devices and replaced by an automatic routing configuration

New GPIOx_ASCR control register has been introduced on STM32L47x/48x devices to control analog interconnection between an I/O pin and ADC input. This register has to be configured before the ADC conversions are started to correctly bring the signal to the ADC input.
This register is removed on other Categories of STM32L4 devices and the analog interconnection will be enabled automatically when an ADC channel is selected.

Multi-supply I/O pins

- **Some I/O pins can be supplied from different sources**
- New I/O pin supply scheme brings new I/O pin structures and names
  - TT and FT definition is extended by new abbreviation suffix
  - Maximum VIN is defined by lowest supply voltage connected to the structure of given I/O pin
  - For example, formula VIN < min (VDD, VDDA) + 4.0 V applies for FT_a pin

Abbreviation suffix	Description	Example
_f	I/O with Fm+ capability, supplied by V_{DD}	FT_f, FT_fa
_l	I/O with LCD function, supplied by V_{LCD}	FT_l
_a	I/O with analog function, supplied by V_{DDA}	FT_a, TT_a
_u	I/O with USB function, supplied by V_{DDUSB}	FT_u
_s	I/O with independent supply, supplied by V_{DDIO2}	FT_s, FT_fs

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A new multi-supply scheme of I/O pins brings new I/O pin structures. Previously-used naming – FT, TT – has been extended by abbreviation suffixes to highlight alternate supply sources for each FT and TT I/O pin.
Previously-used name FTf for Fm+ capable pins has been transformed to FT_f, the new _l suffix has been added to mark pins supplied through LCD supply, suffix _a marks pins supplied by analog supply, suffix _u is used for pins supplied from USB supply and suffix _s now clearly identifies pins within the independent VDDIO2 supply domain.
The absolute maximum rating for each I/O pin is defined by the lowest voltage of the supplies listed for each I/O pin.

Low-power modes

Mode	I/O Description
Run	Active.
Sleep	Active.
Low-power run	Active.
Low-power sleep	Active.
Stop0/Stop 1	Active.
Stop 2	Active.
Standby	Only as input with internal pull-up, pull-down or floating.
Shutdown	Only as input with internal pull-up, pull-down or floating. Configuration lost when exiting.
Reset	Forced to analog input mode when the MCU is under reset.

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I/O pins remain active in all modes except Standby and Shutdown, where the only available configuration is input with internal pull-up, pull-down resistor or floating input. When exiting Shutdown mode, the I/O configuration is lost. When the MCU is under reset, I/O pins are forced into an analog input mode.

Differences with STM32L47x/48x devices

- For STM32L43x/44x/45x/46x devices, the maximum number of GPIO is up to 83.
- For STM32L41x/42x/43x/44x/45x/46x/49x/4Ax devices, the GPIOx_ASCR register used to enable the analog switches connected to the ADC, is not present.
- No GPIOs can be connected to the independent VDDIO2 power supply for STM32L41x/42x/43x/44x/45x/46x devices.

This slide presents the key differences between baseline STM32L47x/48x devices and other devices.

Compared to STM32L47x/48x devices, STM32L43x/44x/45x/46x devices have up to 83 GPIOs and STM32L41x/42x devices have up to 52 GPIOs. They no longer have GPIOs connected to an independent power supply (VDDIO2), and the GPIOx_ASCR register, enabling an analog switch connected to the ADC inputs, is no longer present.