Hello, and welcome to this presentation of the STM32 Low-power timer (LPTIM). It covers the features of this peripheral, which offers a set of timing features and can generate waveforms even in low-power modes.

Overview

- The LPTIM is a 16-bit timer. Thanks to its diversity of clock sources, the LPTIM is able to keep running in most of the available low-power modes of the STM32L4 microcontroller.

Features summary

- Asynchronous running capability
- Ultra-low power consumption
- Timeout function for wakeup from low-power modes

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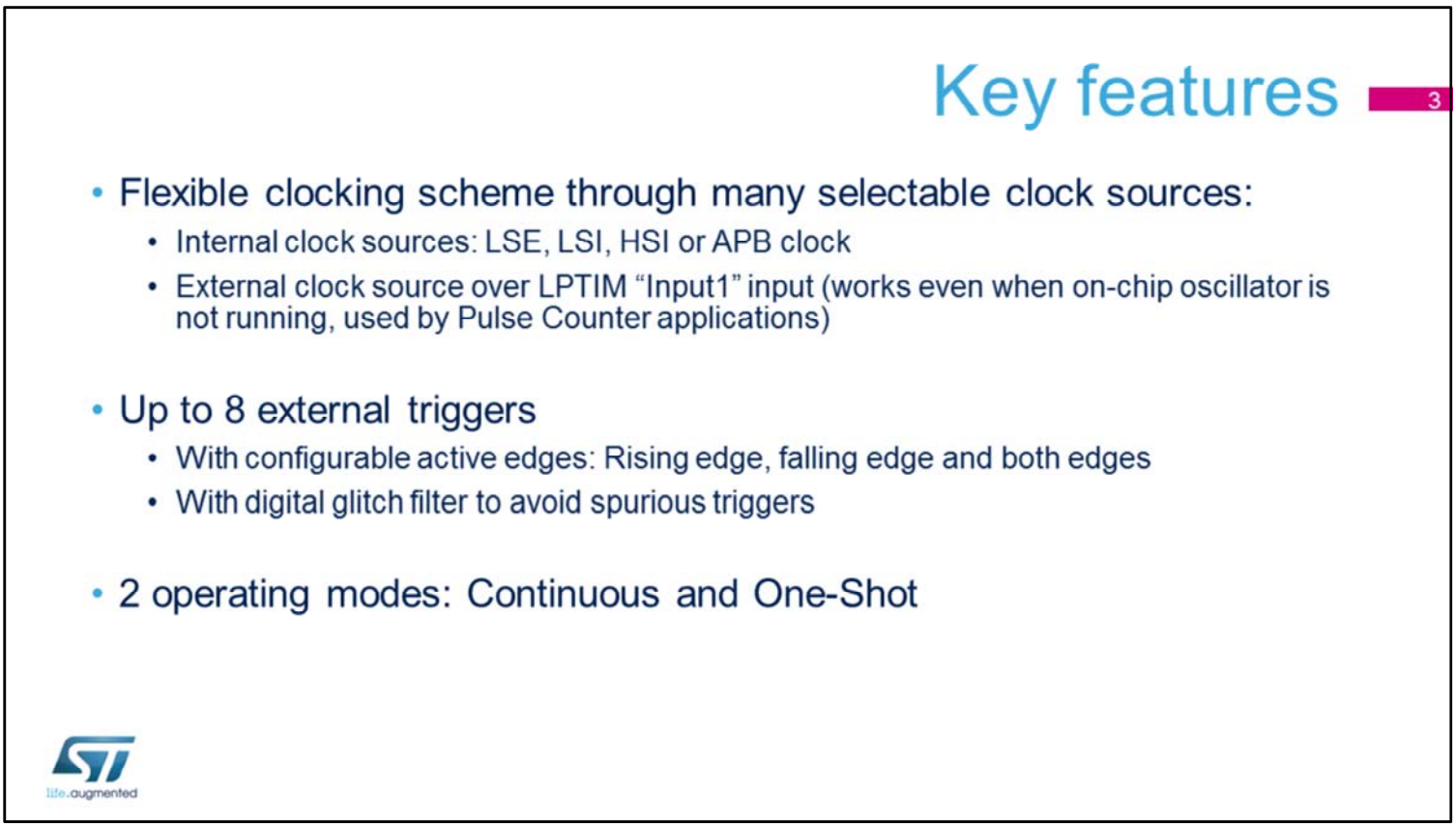
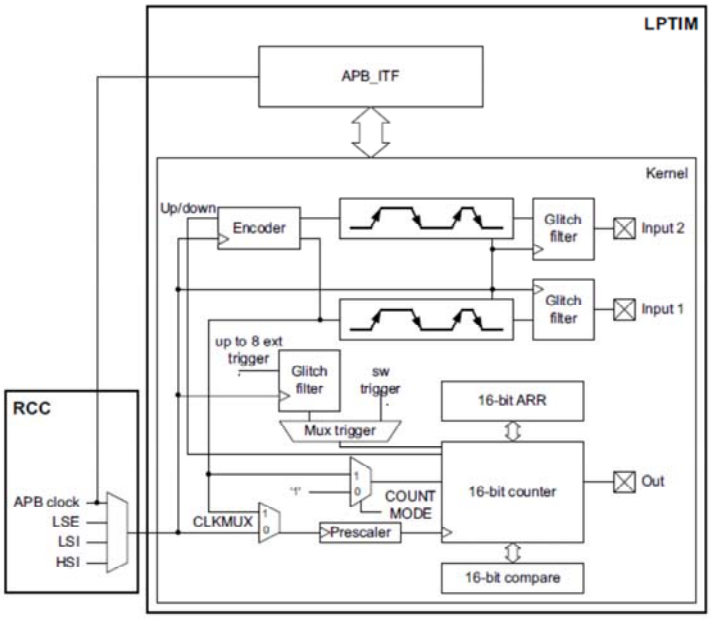
The low-power timer peripheral embedded in the STM32L4 microcontroller provides a 16-bits timer that is able to run even in Stop 0, Stop 1 and Stop 2 low-power modes. This is made possible thanks to a flexible clocking scheme. The low-power timer peripheral provides basic general-purpose timer functions with very low power consumption compared to other timers. One major function of the low-power timer is its capability to keep running even when no internal clock source is active when configured in asynchronous counting mode.



The low-power timer's main feature is its ability to keep running even in low-power modes when almost all clock sources are turned off. The low-power timer has a very flexible clocking scheme. It can be clocked from on-chip clock sources: LSE, LSI, HSI or APB clock. Or it can be clocked from an external clock source over the low-power timer's "Input1" input. This latter feature is used for building "Pulse Counter" applications and is a key function for metering applications like gas-meters, etc.
The low-power timer features up to 8 external trigger sources with configurable polarity. External trigger inputs feature digital filters to cancel-out faulty triggers that could be raised in noisy operating environments.
The low-power timer can be configured to run either in Continuous or One-shot mode. One-shot mode is used for generating pulse waveforms while Continuous mode is used to generate PWM waveforms.

Block diagram



The low-power timer is a peripheral with two clock domains. The APB clock domain contains the peripheral's APB interface. The kernel clock domain contains the low-power timer peripheral's core functions. The kernel clock domain can be clocked by the APB clock source or by other internal clock sources including the LSE, LSI and HSI sources. Also the kernel clock domain can be clocked from an external clock source through the timer's "Input1" input.

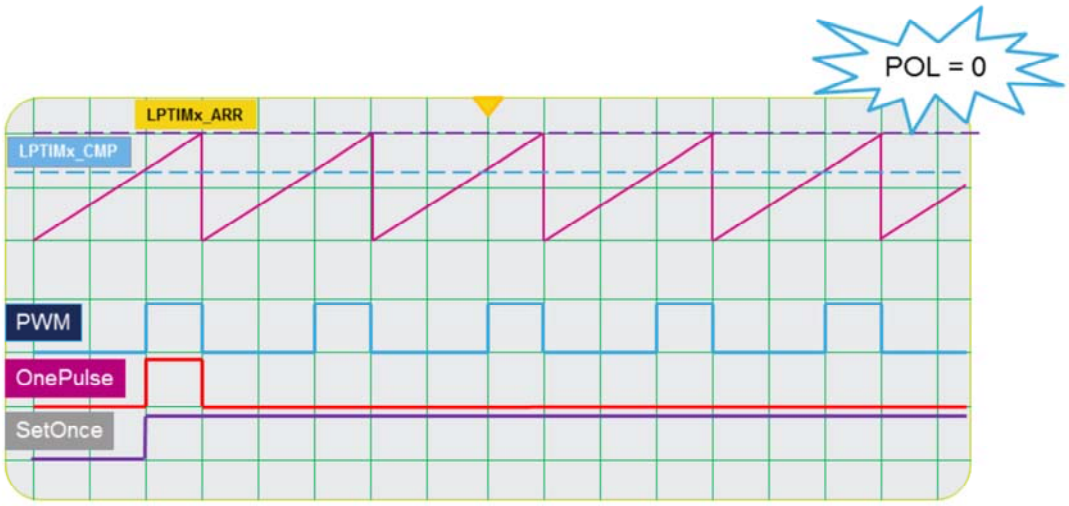
The low-power timer peripheral embeds a 16-bit counter that is fed through a power-of-two prescaler. The low-power timer peripheral features a 16-bit Auto-reload register and a 16-bit Compare register that are used to set the period and duty-cycle, respectively, for a PWM waveform signal output on the timer's "Out" output.

The low-power timer features an Encoder mode function that can be used to interface with incremental quadrature

encoder sensors using the peripheral’s “Input1” and “Input2” inputs. Both inputs feature glitch-filtering circuitry.

Up to 3 configurable waveforms

- PWM, One Pulse and Set Once waveforms



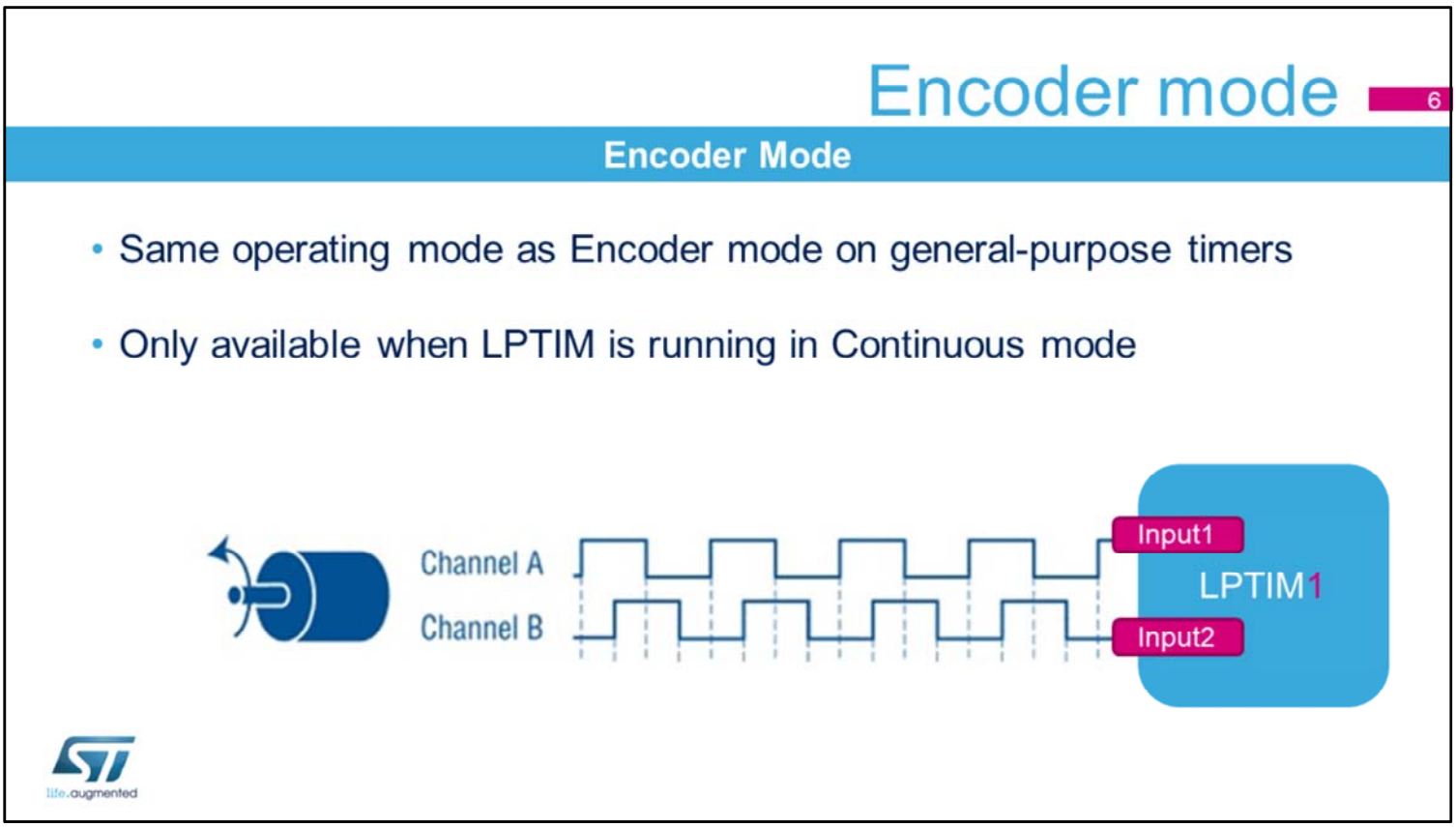
The low-power timer can be used to output various kinds of waveforms even when the microcontroller is in Stop 0, Stop 1 and Stop 2 low-power modes where almost all internal clock sources are turned off. The LPTIMx_CMP and LPTIMx_ARR registers in conjunction with the bit-fields ‘WAVE’ from the LPTIMx_CFGR register and ‘SNGSTRT’ from the LPTIMx_CR register are used to control the output waveform.

The output waveform is either a typical PWM signal with its period and duty-cycle controlled by the LPTIMx_ARR and LPTIMx_CMP registers, respectively. Or it is a single pulse with the last output state defined by the configured waveform.

If the last output state is the same as the one at the waveform’s beginning, then One-pulse mode is configured.

If not, then SetOnce mode is configured.

The low-power timer’s output polarity is controlled through the ‘WAVPOL’ bit-field in the LPTIMx_CFGR register.



The low-power timer features an Encoder mode function that can interface with the incremental quadrature encoder sensors using the peripheral's "Input1" and "Input2" inputs. Both inputs feature glitch-filtering circuitry.
The Encoder function is similar to the one embedded by the general-purpose timers.
In order to use the Encoder mode function, the low-power timer must be running in Continuous mode.
One important thing to note is that only the low-power timer 1 peripheral embeds the Encoder mode function. The low-power timer 2 peripheral doesn't embed an Encoder mode function.

Interrupts

Interrupt event	Description
Compare match	Interrupt flag is raised when the Counter register's (LPTIMx_CNT) content matches the Compare register's (LPTIMx_CMP) content.
Auto-reload match	Interrupt flag is raised when the Counter register's (LPTIMx_CNT) content matches the Auto-reload register's (LPTIMx_ARR) content.
External trigger event	Interrupt flag is raised when an external trigger is detected.
Auto-reload register write completed	Interrupt flag is raised when the write action into the LPTIMx_ARR register is completed.
Compare register write completed	Interrupt flag is raised when the write action into the LPTIMx_CMP register is completed
Direction change	Used for Encoder mode, two interrupt flags are embedded to highlight direction change: Up flag to highlight up-counting direction change and Down flag to highlight down-counting direction change.

The low-power timer peripheral features 7 interrupt sources.

- The “Compare match” interrupt is raised once the content of Counter register LPTIMx_CNT matches or is greater than the Compare register LPTIMx_CMP content.
- The “Auto-reload match” interrupt is raised when the Counter register’s content matches the Auto-reload register’s content.
- The “External trigger event” interrupt is raised when a valid external trigger is detected.
- The “Auto-reload register write completed” and the “Compare register write completed” interrupts are raised when the transfer of the content of the LPTIMx_ARR register and LPTIMx_CMP register, respectively, is completed from the peripheral’s APB interface logic into the peripheral’s core logic which are contained by two

different clock domains. This two interrupts are useful in mitigating the overhead of polling on the status of writing to these two registers when peripheral core clock is too slow compared to the APB interface clock.
- The “Up and Down Direction change” interrupts are raised when the Encoder mode function is enabled and the counting direction is changed from up to down or vice-versa. The counting direction of the low-power timer’s counter reflects the rotation direction of the quadrature sensor.

Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Low-power run	Active.
Low-power sleep	Active. Peripheral interrupts cause the device to exit Low-power sleep mode.
Stop 0/Stop 1	Active. Peripheral registers content is kept. Peripheral may make the device exit Stop 0/Stop 1 mode
Stop 2	Active. Peripheral registers content is kept. Peripheral may make the device exit Stop 2 mode
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.
Shutdown	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

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The low-power timer peripheral is active in the following low-power modes: Run, Sleep, Low-power run, Low-power sleep, Stop 0, Stop 1 and Stop 2.
The low-power timer is able to wake up the microcontroller from either Sleep, Low-power sleep, Stop 0, Stop 1 or Stop 2 modes.