Hello, and welcome to this presentation of the STM32L4 power controller. The STM32L4’s power management functions and all power modes will also be covered in this presentation.
Please note that this presentation has been written for STM32L47x/48x devices.
Key differences with other devices are indicated at the end of the presentation unless otherwise specified.
STM32L4 devices feature FlexPowerControl, which increases flexibility in power mode management and further reduces the overall application consumption. Run mode can support a system clock running at up to 80 MHz, with only 120 µA/MHz. At 26 MHz, the consumption is even lower: 100 µA/MHz.

STM32L4 devices support 8 main low-power modes: Low-power run, Sleep, Low-power sleep, Stop 0, Stop 1, Stop 2, Standby and Shutdown modes. Each mode can be configured in many ways, providing several additional sub-modes.

In addition, STM32L4 devices support a battery backup domain, called VBAT.

The high flexibility in power management provides both high performance with a CoreMark score equal to 273, together with outstanding power efficiency, demonstrated by the ULPBench score equal to 150.

### Power Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Current Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Run (Range 1) at 80 MHz</td>
<td>120 µA / MHz**</td>
</tr>
<tr>
<td>Run (Range 2) at 26 MHz</td>
<td>100 µA / MHz**</td>
</tr>
<tr>
<td>LPRUN at 2 MHz</td>
<td>112 µA / MHz**</td>
</tr>
<tr>
<td>SLEEP at 26 MHz</td>
<td>35 µA / MHz</td>
</tr>
<tr>
<td>LPSLEEP at 2 MHz</td>
<td>48 µA / MHz</td>
</tr>
<tr>
<td>STOP 0 (full retention)</td>
<td>110 µA</td>
</tr>
<tr>
<td>STOP 1 (full retention)</td>
<td>6.6 µA / 6.9 µA*</td>
</tr>
<tr>
<td>STOP 2 (full retention)</td>
<td>1.1 µA / 1.4 µA*</td>
</tr>
<tr>
<td>STANDBY + 32 KB RAM</td>
<td>350 nA / 650 nA*</td>
</tr>
<tr>
<td>STANDBY</td>
<td>115 nA / 415 nA*</td>
</tr>
<tr>
<td>SHUTDOWN</td>
<td>30 nA / 330 nA*</td>
</tr>
<tr>
<td>VBAT</td>
<td>4 nA / 300 nA*</td>
</tr>
</tbody>
</table>

*Typ @ VDD = 1.0 V @ 25 °C

*: with RTC

**: from SHAM1
The STM32L4 has several key features related to power management:
Several low-power modes, down to 30nA while it is still possible to wake up the MCU with an event on an I/O. For only 350 nA, 32 kilobytes of SRAM can be retained. A large number of peripherals can wake up from the various low-power modes. Dynamic consumption is down to 100 µA/MHz, executing from Flash memory. A battery backup domain, called VBAT, including the RTC and certain backup registers. Several power supplies are independent, allowing to reduce MCU power consumption while some peripherals are supplied at higher voltages.

Thanks to the large number of power modes, STM32L4 devices offer high flexibility to minimize the power consumption and adjust it depending on active peripherals,
required performance and needed wake-up sources.
STM32L4 devices have several independent power supplies, which can be set at different voltages or tied together. The main power supply is VDD, supplying almost all I/Os except for 14 I/Os of Port G. VDD also supplies the reset block, temperature sensor and all internal clock sources. In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog. VDD supplies voltage regulators which provide the VCORE supply. VCORE supplies most of the digital peripherals, SRAMs and Flash. STM32L4 MCUs feature several independent supplies for peripherals: VDDA for the analog peripherals, VDDUSB for the USB transceiver and VDDIO2 which supplies the 14 I/Os on Port G. The VLCD pin provides the LCD common and segments reference voltage. The VREF+ pin provides the reference voltage to the analog-to-digital and to digital-to-analog converters and can be used as an external buffer reference for the application. A backup battery can be connected to VBAT pin to supply
the backup domain.
The main power supply VDD ensures full feature operation in all power modes from 1.71 up to 3.6 V, allowing to be supplied by an external 1.8 V regulator. Device functionality is guaranteed down to 1.6 V, the minimum voltage after which a brown-out reset is generated. Other independent supplies are provided to allow peripherals to operate at a different voltage. The analog power supply VDDA can be connected to any voltage other than VDD. When the analog-to-digital converters or comparators are used, the VDDA voltage must be greater than 1.62 V. When the digital-to-analog converters or operational amplifiers are used, VDDA must be greater than 1.8 V. When the voltage reference buffer is used, VDDA must be greater than 2.4 V. The USB power supply VDDUSB can be connected to any voltage other than VDD. When the USB is used, VDDUSB must be greater than 3 V.

14 I/Os of Port G, from PG15 to PG2, are supplied by
VDDIO2 independently from VDD. When these I/Os are used, VDDIO2 can be as low as 1.08 V. Several functions are available on these I/Os: I2C, SPI, serial audio interface, USARTs and Timers. The number of available I/O’s depends on the package.

A backup domain is supplied by VBAT, which must be greater than 1.55 V. The backup domain contains the RTC, the 32.768-kHz LSE external oscillator and the 128-byte backup registers.
The LCD reference voltage can be provided either by an external supply voltage or by the embedded voltage step-up converter. This reference is independent from the VDD voltage, ensuring the same LCD contrast regardless of the VDD value. VLCD is multiplexed with the PC3 pin which can be used as a GPIO when the LCD is not used.

- **VLCD from 2.5 to 3.6 V**: reference voltage for LCD:
  - It can be provided either by an external supply voltage or by the embedded voltage step-up converter, independently of the VDD voltage.
  - VLCD is multiplexed with PC3 which can be used as a GPIO when the LCD is not used.

- **VREF+**: reference voltage for ADCs and DACs
  - It can be provided either by an external reference voltage or by the internal voltage reference buffer.
  - VREF+ pin, and thus the internal voltage reference, is not available on low pin count packages. On those packages, this pin is double-bonded with VDDA which can be connected to an external reference. The internal voltage reference buffer is not available and must be kept disabled.

The LCD reference voltage can be provided either by an external supply voltage or by the embedded voltage step-up converter. This reference is independent from the VDD voltage, ensuring the same LCD contrast regardless of the VDD value. VLCD is multiplexed with the PC3 pin which can be used as a GPIO when the LCD is not used.

The ADC and DAC voltage references can be provided either by an external supply voltage or by the internal reference buffer. This allows us to improve converters performance by providing an isolated and independent reference voltage. The VREF+ pin and thus the internal voltage reference, is not available on low pin count packages. In those packages, the VREF+ is double-bonded with VDDA and the internal voltage buffer must be kept disabled. The voltage reference can be provided through the VDDA pin in those packages.
As a general requirement, the VDD power supply has to be provided first and released last.

More precisely, during the power-on phase, the following power sequence requirements must be respected:
- When VDD is below 1 Volt, other power supplies (VDDA, VDDIO2, VDDUSB and VLCD) must remain below VDD +300 millivolts.
- When VDD is above 1 Volt, all power supplies become independent.

During the power-down phase, VDD has to be switched off at the same time or after other power supplies. But VDD can temporarily become lower than other supplies provided that the energy absorbed by the MCU during this transient phase remains below 1 mJ.
Refer to the application note AN4555 for more details on the power supplies sequencing.
The STM32L4 MCU embeds four Peripheral Voltage Monitors to detect if the independent supply is present or not. These comparators have wake-up from Stop mode capability. The PVM1 compares the VDDUSB voltage with the 1.22 V threshold. The PVM2 compares the VDDIO2 voltage with the 0.96 V threshold. The PVM3 compares the VDDA voltage with the 1.65 V threshold, intended for the comparators and analog-to-digital converters. The PVM4 compares the VDDA voltage with the 1.82 V threshold, intended for the operational amplifiers and digital-to-analog converters.

To guarantee any of the supply sequences on the application, power isolation has been implemented and is active by default. It is the role of software to enable the needed supplies by removing the power isolation.
The power supply supervisor guarantees a safe and ultra-low power reset management. STM32L4 devices embed an ultra-low-power brown-out reset which is always enabled in all power modes except Shutdown mode. The BOR ensures reset generation as soon as the MCU drops below the selected threshold, regardless of the VDD slope. Five thresholds from 1.7 to 2.95 V are selected by option byte BOR_LEV[2:0], from VBOR0 = 1.7 V to VBOR1 = 2.95 V.

A power voltage detector can generate an interrupt when VDD crosses the selected threshold. The PVD can be enabled in all modes except Standby and Shutdown modes. 7 thresholds can be selected by software. In addition, comparisons can be done with an external pin. The BOR consumption with the 1.7 V threshold is included in the datasheet.
Two embedded linear voltage regulators supply all the digital circuitries except for the Standby circuitry and the Backup domain. The regulator output voltage (VCORE) can be programmed by software to two different values depending on the performance and the power consumption requirements. This is called Dynamic Voltage Scaling.

Depending on the application mode, VCORE is provided either by the Main voltage regulator for Run, Sleep and Stop0 modes, or by the Low-power regulator for Low-power run, Low-power sleep, Stop 0, Stop 1 and Stop 2 modes. The regulators are OFF in Standby and Shutdown mode. When SRAM2 content is preserved in Standby mode, the Low-power regulator remains ON and provides the SRAM2 supply.
In run mode, the voltage scaling Range 1 is the high performance range, allowing a system clock up to 80 MHz.
All peripherals can be activated, all clocks can be enabled.
The Run mode range 1 consumption is 131 µA/MHz at 80 MHz, from Flash memory with the ART accelerator enabled.
In Run mode, the voltage scaling Range 2 is the medium performance range, allowing a system clock up to 26 MHz. When executing from SRAM, the Flash consumption can be saved by configuring the Flash in Power-down mode and by gating its clock off. All peripherals can be activated except the USB OTG and Random Number Generator. All clocks can be enabled.

The Run mode range 2 consumption is 110 µA/MHz at 26 MHz from SRAM.
In Low-power run mode, the main regulator is OFF and the low-power regulator supplies the logic allowing a system clock up to 2 MHz. When executing from SRAM, the Flash consumption can be reduced by configuring the Flash memory in Power-down mode and by gating its clock off.

All peripherals can be activated except the USB OTG and Random Number Generator. All clocks can be enabled. At 2 MHz, there is no limitation regarding the number of peripherals that can be activated.

The Low-power run mode consumption is 135 µA/MHz at 2 MHz when executing from Flash memory with the ART accelerator enabled. It is 112 µA/MHz at 2 MHz when executing from SRAM1. The I2C, USART, LPUART and SWPMI clocks can be based on the internal high-speed oscillator at 16 MHz.
The Run mode, thanks to voltage scaling, and the Low-power run modes offer flexibility between required performance and consumption. In Run mode range 1, the system clock is limited to 80 MHz and the internal and external oscillators and the PLL can be used. In Run mode range 2, the system clock is limited to 26 MHz and the internal and external oscillators as well as the PLL can be used, but must be limited to 26 MHz. In Low-power run mode, the system clock must be limited to 2 MHz.
Run and Low-power run modes

- Each peripheral clock can be configured to be ON or OFF
  - After reset, all peripheral clocks are OFF, except Flash interface clock
  - SRAM1 and SRAM2 clocks are always ON in Run mode

- When running from SRAM1 or SRAM2 (in Run or Low-power run):
  - Flash can be put in Power-down mode
  - Flash clock can be switched off
  - Interrupt vectors must also be re-mapped to SRAM!

Each peripheral clock can be configured to be ON or OFF in Run and Low-power run modes. By default all peripherals clocks are OFF, except the Flash interface clock. The SRAM1 and SRAM2 clocks are always ON in Run mode.

When running from SRAM1 or SRAM2 (in Run or Low-power run modes), the Flash memory can be put in Power-down mode thanks to software, and the Flash clock can be switched off. The Flash memory must not be accessed when it is switched off, consequently interrupts must be mapped in SRAM, using the Cortex-M4 Vector Table Offset Register.
The current consumption in Run or Low-power run modes depends on several parameters: first the executed binary code, that means the program itself plus the compiler impact. Then it depends on the program location in the memory, the device software configuration, the I/O pin loading and switching rate, the temperature and so on...

The consumption also depends on if the code is executed from Flash memory or from SRAM. When code is executed from Flash, the Energy efficiency is better when the Flash accelerator is enable. When code is executed from SRAM, the Energy efficiency is better when executing from SRAM2.
The consumption in Run mode can be optimized down to low frequency, thanks to Low-power run mode. Enabling the ART accelerator increases performance but also reduces the dynamic consumption. Best consumption is most often reached when the Instruction Cache is ON, Data Cache is ON and Prefetch buffer is OFF, as this configuration reduces the number of Flash memory accesses.

The small Flash dynamic consumption allows a small consumption each time the firmware needs to access the Flash memory.

Consumptions from SRAM1 and SRAM2 are quite similar, but SRAM2 is much more power efficient than SRAM1, when not remapped at address 0, thanks to its 0 wait-state access.
Sleep and Low-power sleep modes allows all peripherals to be used and features the fastest wakeup time. In these modes, the CPU is stopped and each peripheral clock can be configured by software to be gated ON or OFF during the Sleep and Low-power sleep modes. These modes are entered by executing the assembler instruction Wait for Interrupt or Wait for Event. When executed in Low-power run mode, the device enters Low-power sleep mode.

Depending on the SLEEPONEXIT bit configuration in the CortexM4 System Control Register, the MCU enters Sleep mode as soon as the instruction is executed, or as soon as it exits the lowest priority Interrupt Sub Routine. This last configuration allows to save time and consumption by saving the need to pop and push the stack.
Batch Acquisition Mode is an optimized mode for transferring data. Only the needed communication peripheral + 1 DMA + 1 SRAM are configured with clock enabled in Sleep mode. Flash memory is put in Power-down mode and Flash clock is gated off during Sleep mode. Enter either Sleep or Low-power sleep mode. Note that the I2C clock can be at 16 MHz even in Low-power sleep mode, allowing support for 1-MHz Fast-mode Plus support. USART/LPUART clock can also be HSI16. Then it can enter either Sleep or Low-power sleep mode. Typical applications are sensor hubs.
In Sleep mode, the CPU clocks are OFF. In Range 1, the system clock is up to 80 MHz, in Range 2 it is up to 26 MHz. By default, the SRAM1 and SRAM2 clocks are enabled. They can be gated off during Sleep mode by software.

All peripherals can be activated in Range 1. In Range 2, all peripherals can be activated except the USB OTG and Random Number Generator.

The Sleep mode consumption is 37 µA/MHz in Range 1 at 80 MHz with the Flash memory ON.
In Low-power sleep mode, the CPU clocks are OFF and the logic is supplied by the low-power regulator. The system clock is up to 2 MHz. Flash memory can be configured in Power down and can be gated off; SRAM1 and SRAM2 can be gated off. All peripherals can be activated except the USB OTG and Random Number Generator. The Low-power sleep mode consumption is 40 µA/MHz at 2 MHz with Flash memory and SRAM OFF.
STM32L4 devices features three Stop modes: Stop 0, 1 and 2, which are the lowest power modes with full retention and only a 0.7-μs wakeup time to Run mode at 48 MHz. The contents of SRAM1, SRAM2 and all peripherals registers are preserved in Stop modes. All high speed clocks are stopped. The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled. Several peripherals can be active and wake up from Stop mode. System clock on wake-up can be the internal high-speed and multi-speed oscillators up to 48 MHz with only a 0.7μs wakeup time from RAM or 5μs from FLASH. Stop 2 consumption is lower than Stop 1, but Stop 0 and 1 supports more active peripherals.
In Stop 0 mode, the system clock is frozen and all high-speed clocks are powered down. The RTC, clocked by the internal or external low-speed oscillator, can be activated.

The brown-out reset is always enabled. Most of the peripheral clocks are gated off. Several peripherals can be functional in Stop 0 mode: Power voltage detector, peripherals voltage monitor, LCD controller, digital to analog converters, operational amplifiers, comparators, independent watchdog, low power timers, I2C, UART and low-power UART.

The events from all I/Os can wake up from Stop 0 mode, plus the interrupt generated by the active peripherals. In addition, SWPMI and USB can wake up from Stop 0 mode. The I2C and UART or LPUART can switch the HSI16 ON during the Stop mode in order to recognize their wakeup condition.
The Stop 0 mode consumption is 110 μA typical at 3V. The wakeup time is 0.7 μs when the system clock at wake up is MSI at 48 MHz, and the code is executed from SRAM.
Stop 1 mode is very similar to Stop 0 except that the power figures are much lower as the main regulator is stopped and replaced by the low Power Regulator.

The Stop 1 mode consumption without RTC is 6.6 µA typical at 3V. The wakeup time is 4 µs when the system clock at wakeup is MSI at 48 MHz, and the code is executed from SRAM.
In Stop 2 mode, the system clock is frozen and all high-speed clocks are powered down. The RTC, clocked by the internal or external low-speed oscillator, can be activated.

The brown-out reset is always enabled. Most of the peripheral clocks are gated off. Several peripherals can be functional in Stop 2 mode: power voltage detector, peripheral voltage monitors, LCD controller, comparators, independent watchdog, low power timer 1, I2C3, and the low-power UART.

The events from all I/Os can wake up from Stop 2 mode, plus the interrupt generated by the active peripherals. The I2C3 and LPUART can switch the HSI16 ON during Stop mode in order to recognize their wakeup condition.

The consumption in Stop 2 mode without the RTC is 1.2 µA typical at 3 V. The wakeup time is 5 µs when the system clock at wakeup is MSI at 48 MHz, and the code
is executed from SRAM.
When comparing Stop modes:

Stop 1 mode consumption is higher than Stop 2 mode consumption, but the wakeup time is shorter and the number of active peripherals is higher.

Stop 0 mode keep the Main regulator enabled, allowing a very short wake-up time lower than 1µs when restarting from the RAM to the expense of a higher consumption than Stop 1.

It is possible to wake up from Stop 0 or 1 mode with the USB Resume from Suspend event or with Attach Detection, but it is not supported in Stop 2 mode. A SWPMI Resume from Suspend event can also wake up the MCU from Stop 0 or 1 mode, but not from Stop 2.

The I2C address recognition is functional in both Stop modes, and can generate a wakeup event in case of an address match. Only 1 I2C is supported in Stop 2 versus 3 I2Cs in other Stop.

The UART byte reception is functional in both Stop modes and can generate a wakeup event in case of Start detection or Byte reception or Address match event. Only the low-power UART is
supported in Stop 2 mode. In other Stop modes, all 5 UARTs and the low-power UART can generate a wakeup event. When clocked by the internal or external low-speed oscillator, or when clocked by an external pin, the low-power timer can wake up the MCU with all its events. In Stop 0 or 1 mode, both low-power timers are supported whereas only LPTIM1 is supported in Stop 2 mode.
The Standby mode is the lowest power mode in which 32 Kbytes of SRAM2 can be retained, the automatic switch from VDD to VBAT is supported and the I/Os level can be configured by independent pull-up and pull-down circuitry.

By default, the voltage regulators are in Power down mode and the SRAMs and the peripherals registers are lost. The 128-byte backup registers are always retained. Thanks to software, it is possible to retain 32 Kbytes of SRAM2.

The ultra-low-power brown-out reset is always ON to ensure a safe reset regardless of the VDD slope.

Each I/O can be configured with or without a pull-up or pull-down, which is applied and released thanks to the APC control bit. This allows you to control the inputs state of external components even during Standby mode.
5 wakeup pins are available to wake up the device from Standby mode. The polarity of each of the 5 wakeup pins is configurable. The wakeup clock is MSI with a frequency configurable from 1 to 8 MHz.
In Standby mode with SRAM2, the main regulator is powered down and the low power regulator supplies the SRAM2 to preserve its content. The RTC, clocked by the internal or external low-speed oscillator, can be activated.

The brown-out reset is always enabled. The independent watchdog can also be enabled in Standby mode. Reset, brown-out reset, RTC and tamper detection, independent watchdog and any event on the 5 wakeup pins can exit the MCU from Standby mode.

The Standby with SRAM2 consumption without the RTC is around 390 nA typical at 3 V. The wakeup time is approximately 14 µs.
In Standby mode without SRAM2, the main regulator and the low-power regulator are powered down. The RTC, clocked by the internal or external low-speed oscillator, can be activated.

The brown-out reset is always enabled. The independent watchdog can also be enabled in Standby mode.

The wakeup events are the same as those described in Standby mode with SRAM2.

The Standby consumption without RTC is 150 nA typical at 3 V. The wakeup time is approximately 14 µs.
The shutdown mode is the lowest power mode of the STM32L4, with only 30 nA at 1.8 V. This mode is similar to Standby mode but without any power monitoring: the brown-out reset is disabled and the switch to VBAT is not supported in Shutdown mode. Hence the product state is not guaranteed in case the power supply is lowered below 1.6V. The LSI is not available, and consequently the independent watchdog is also not available. A brown-out reset is generated when the device exits Shutdown mode: all registers are reset except those in the backup domain, and a reset signal is generated on the pad. The 128-byte backup registers are retained in Shutdown mode. The wakeup sources are the 5 wakeup pins and the RTC. When exiting Shutdown mode, the wakeup clock is MSI
at 4 MHz.
In Shutdown mode, the main regulator and the low-power regulator are powered down. The RTC, clocked by the external low-speed oscillator, can be activated. The brown-out reset is deactivated. Only the external low-speed clock can be enabled.

The wakeup events are the RTC and tamper events, the reset and the 5 wakeup pins.

The Shutdown consumption without RTC is around 60 nA typical at 3 V. The wakeup time is approximately 250 µs.
Here you can see the summary of all the STM32L4 power modes.
From Run mode, it is possible to access all low-power modes except Low-power sleep mode. In order to go into Low-power sleep mode, it is required to move first to Low-power run mode and execute a Wait for Interrupt or Wait for Event instruction while the regulator is the low-power regulator. On the other hand, when exiting Low-power sleep mode, the STM32L4 is in Low-power run mode.

When the device is in Low-power run mode, it is possible to go into all low-power modes except Sleep, Stop 0 and Stop 2 modes. Sleep, Stop 0 or Stop 2 modes can only be entered from Run mode. If the device enters Stop 1 mode from Low-power run mode, it will exit in Low-power run mode. If the device enters Standby or Shutdown from Low-power run mode, it will exit in Run mode.
The backup domain allows to keep the RTC functional and to preserve the backup registers in case the VDD supply is down, thanks to a backup battery connected to the VBAT pin. The backup domain contains the RTC clocked by the low-speed external oscillator at 32.768 kHz. 3 tamper pins are functional in VBAT mode, and will erase the 128-byte backup registers also included in the VBAT domain, in case of intrusion detection.

The backup domain also contains the RTC clock control logic.

In case VDD drops below a certain threshold, the backup domain power supply automatically switches to VBAT. When VDD is back to normal, the backup domain power supply automatically switches back to VDD.

The VBAT voltage is internally connected to an ADC input channel in order to monitor the backup battery.
level.
When VDD is present, the battery connected to VBAT can be charged from the VDD supply.
The battery charging feature allows to charge a super-cap connected to VBAT pin through internal resistor when VDD is present. The charging is enabled by software and is done either through a 5kΩ or 1.5kΩ resistor depending on software. Battery charging is automatically disabled in VBAT mode.
In VBAT mode, the entire MCU is in Power-down mode except the backup domain, including the 128-byte backup registers, RTC and external low-speed clock. The consumption from VBAT pin is approximately 6 nA without the RTC at 3 V, and 500 nA with the RTC.
3 bits are available in the Flash option bytes to prohibit a given low-power mode. When cleared, an option bit configures reset generation when entering Shutdown mode. Another bit configures reset generation when entering Standby mode and the last bit configures reset generation when entering Stop modes.
3 bits are available in the Debug Control Register, in order to allow debugging in Sleep, Stop, Standby and Shutdown modes. When the related bit is set, the regulator is kept ON in Standby and Shutdown modes, and the HCLK and FCLK clocks remain ON to keep the debugger active. This maintains the connection with the debugger during the low-power modes, and continues debugging after wakeup. Remember to clear these bits when the MCU is not under debug, because the consumption is higher in all low-power modes when these bits are set, due to the fact they force the clocks and the regulators to remain enabled.
In addition to this training, you can refer to the Reset and Clock Control, Interrupts trainings as well as those for all the peripherals with wakeup from Stop capability.
For more details, please refer to following sources

- AN4621: STM32L4xx ultra-low-power features overview
- AN4746: Optimizing power and performances with STM32L4 series microcontrollers

For more details, please refer to application note
*STM32L4 ultra-low-power features overview.*
This slide presents the key consumption differences between STM32L4 devices.
This slide presents the key differences in ULP Bench scores between STM32L4 devices.

The ULP Bench score is also impacted by the difference in consumption (VDD = 3 V):

<table>
<thead>
<tr>
<th></th>
<th>L49x/4Ax</th>
<th>L47x/48x</th>
<th>L45x/40x</th>
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<td><strong>ULP Bench score</strong></td>
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