

ST7 MICROCONTROLLER TRAINING

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ST-REALIZER

Introduction

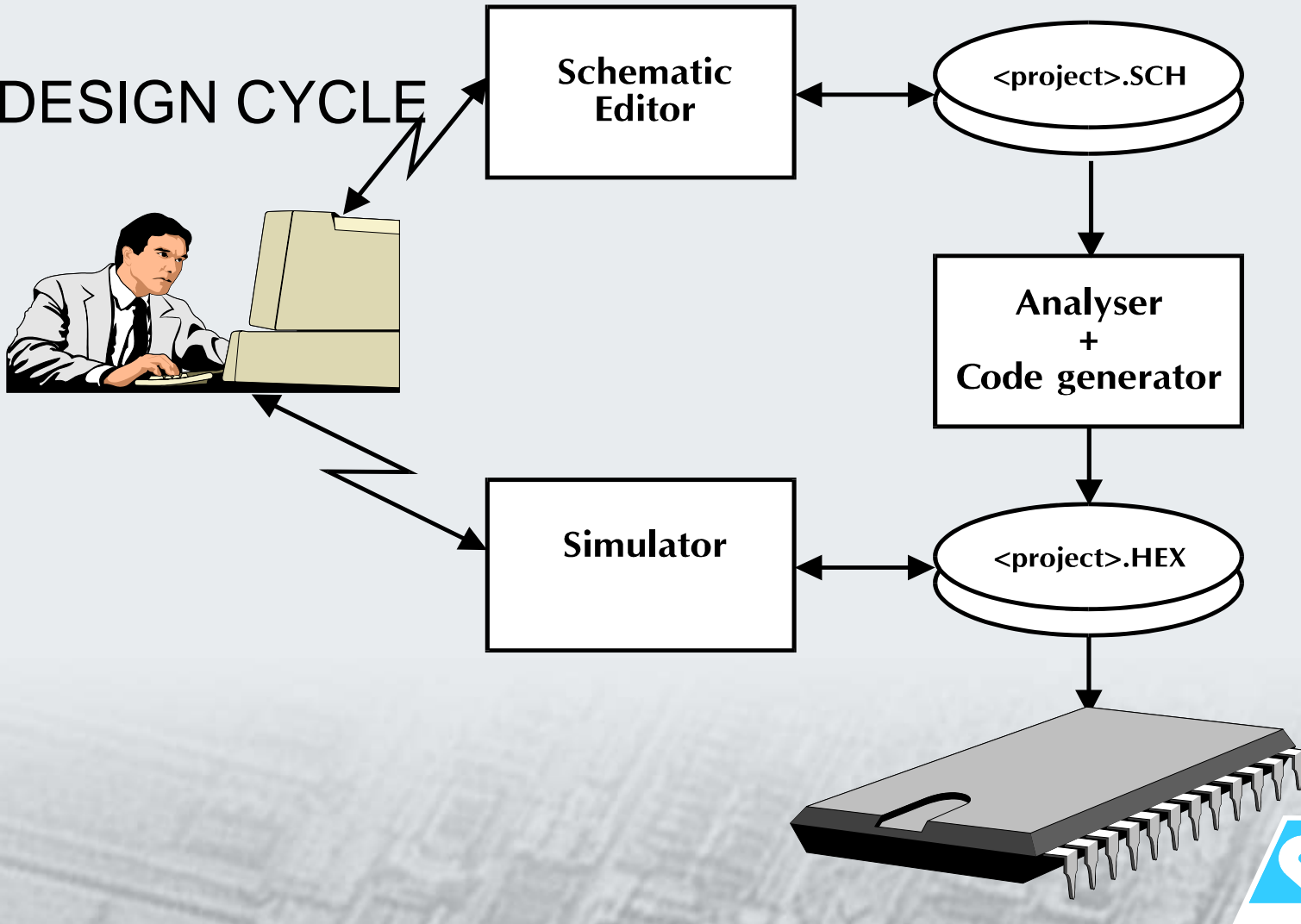
- Software developed by ACTUM Solutions for ST micros (ST6 and ST7) from their REALIZER product
- ST-REALIZER is a graphical oriented tool
- The application is described as a schematic using symbols
- Symbols are coming from libraries
- From the schematic, ST-REALIZER generates the executable code that will be programmed into the chip.



ST-REALIZER

Introduction (2)

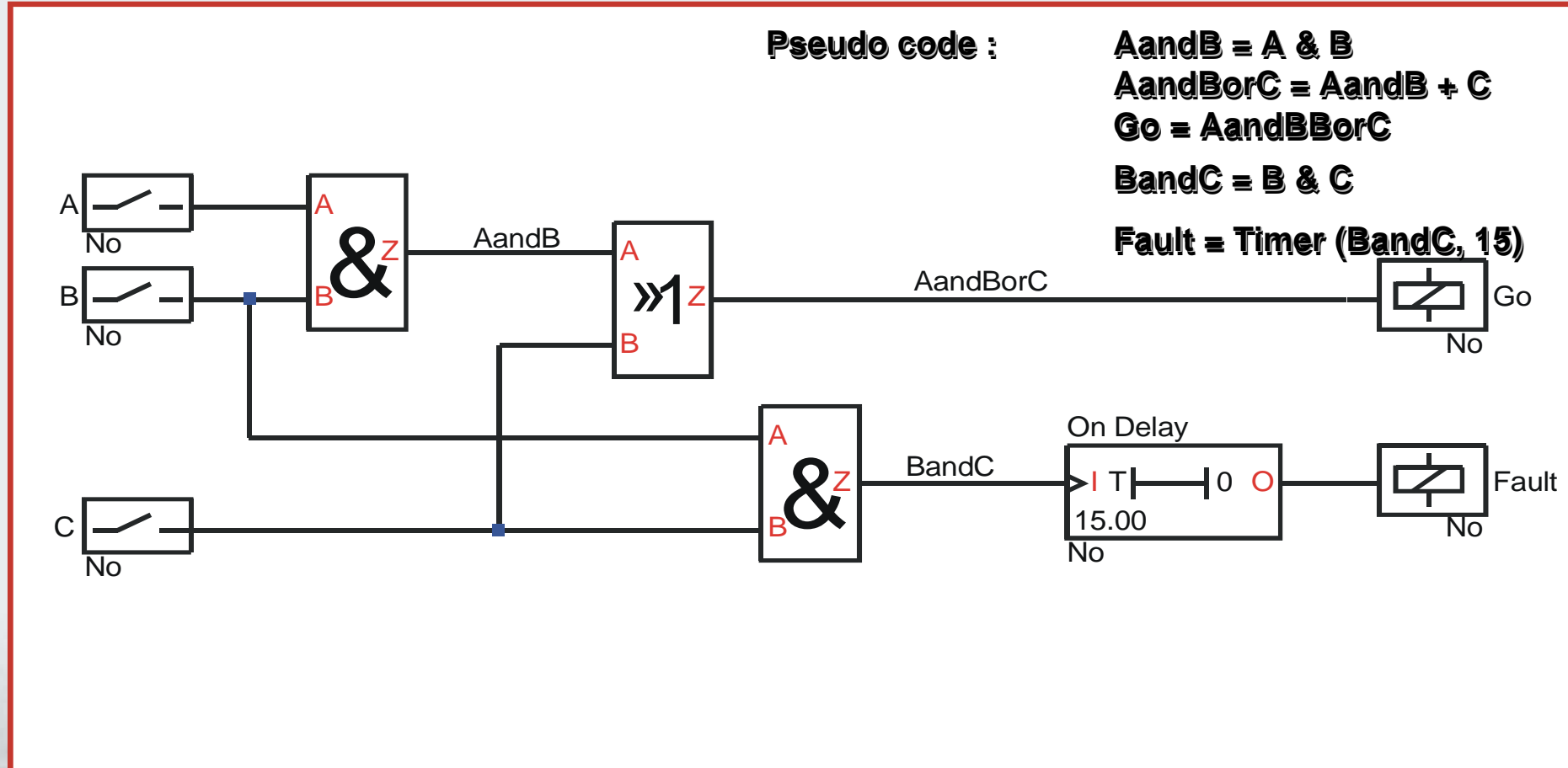
- DESIGN CYCLE



ST-REALIZER

Basic concepts

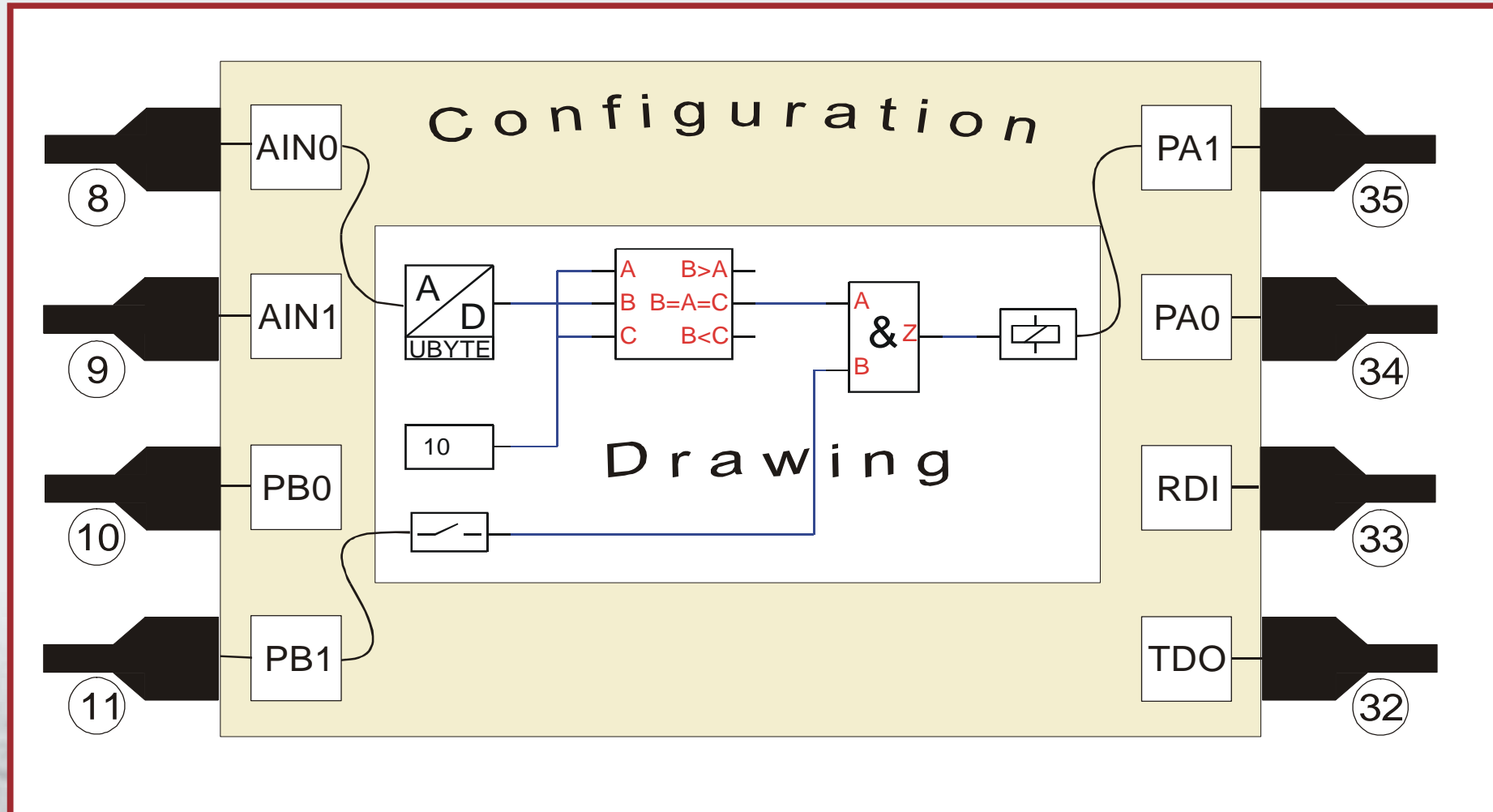
- EXAMPLE SCHEMATIC



ST-REALIZER

Basic concepts

- CONNECTING I/Os



ST-REALIZER

Basic concepts

- REAL CODE

```

C095 1581
C097 038105
C09A 018102
C09D 1481
C09F 058110
C0A2 06810A
C0A5 A6DB
C0A7 B783
C0A9 A605
C0AB B782
C0AD 1F82
C0AF 0F8207
C0B2 1881
C0B4 048102
C0B7 1981
C0B9
C0B9 088105
C0BC 1308
C0BE CCC0C3
C0C1 1208
C0C3 1D81
C0C5 0B8105
C0C8 038102
C0CB 1C81
C0CD 1E81
C0CF 0C8105
C0D2 008102
C0D5 1F81

.RINPEND: bres v0n4,#{2}
          btjf v0n7,#{1},ELOC4
          btjf v0n6,#{0},ELOC4
          bset v0n4,#{2}
ELOC4:   btjf v0n4,#{2},SLOC5
          btjt pv0n4,#{3},ChkLOC5
          ld A,{low {1499}}
          ld {T00006+1},A
          ld A,{low {{1499} shr 8}}
          ld T00006,A
          bres T00006,#{7}
ChkLOC5: btjf T00006,#{7},ELOC5
SLOC5:   bset v0n3,#{4}
          btjt v0n4,#{2},ELOC7
          bres v0n3,#{4}

ELOC7:
ELOC5:   btjt v0n3,#{4},SLOC8
          bres PBDR,#{1}
          jp ELOC8
SLOC8:   bset PBDR,#{1}
ELOC8:   bres v0n1,#{6}
          btjf v0n0,#{5},ELOC9
          btjf v0n7,#{1},ELOC9
          bset v0n1,#{6}
ELOC9:   bset v0n2,#{7}
          btjt v0n1,#{6},ELOCa
          btjt v0n6,#{0},ELOCa
          bres v0n2,#{7}

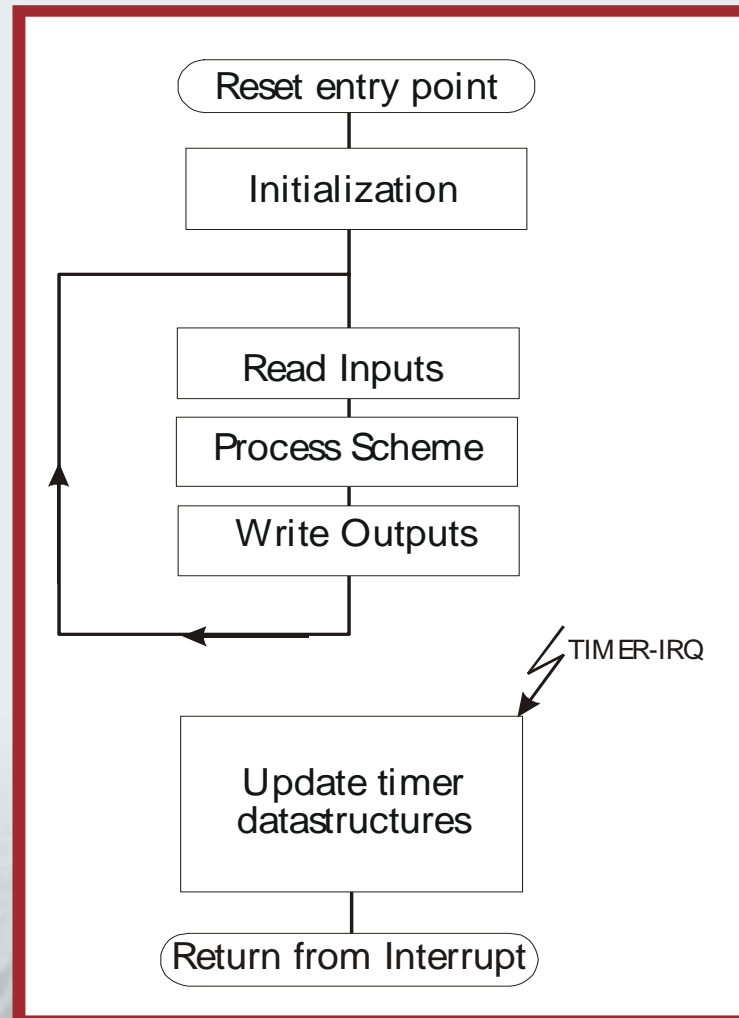
```



ST-REALIZER

Basic concepts

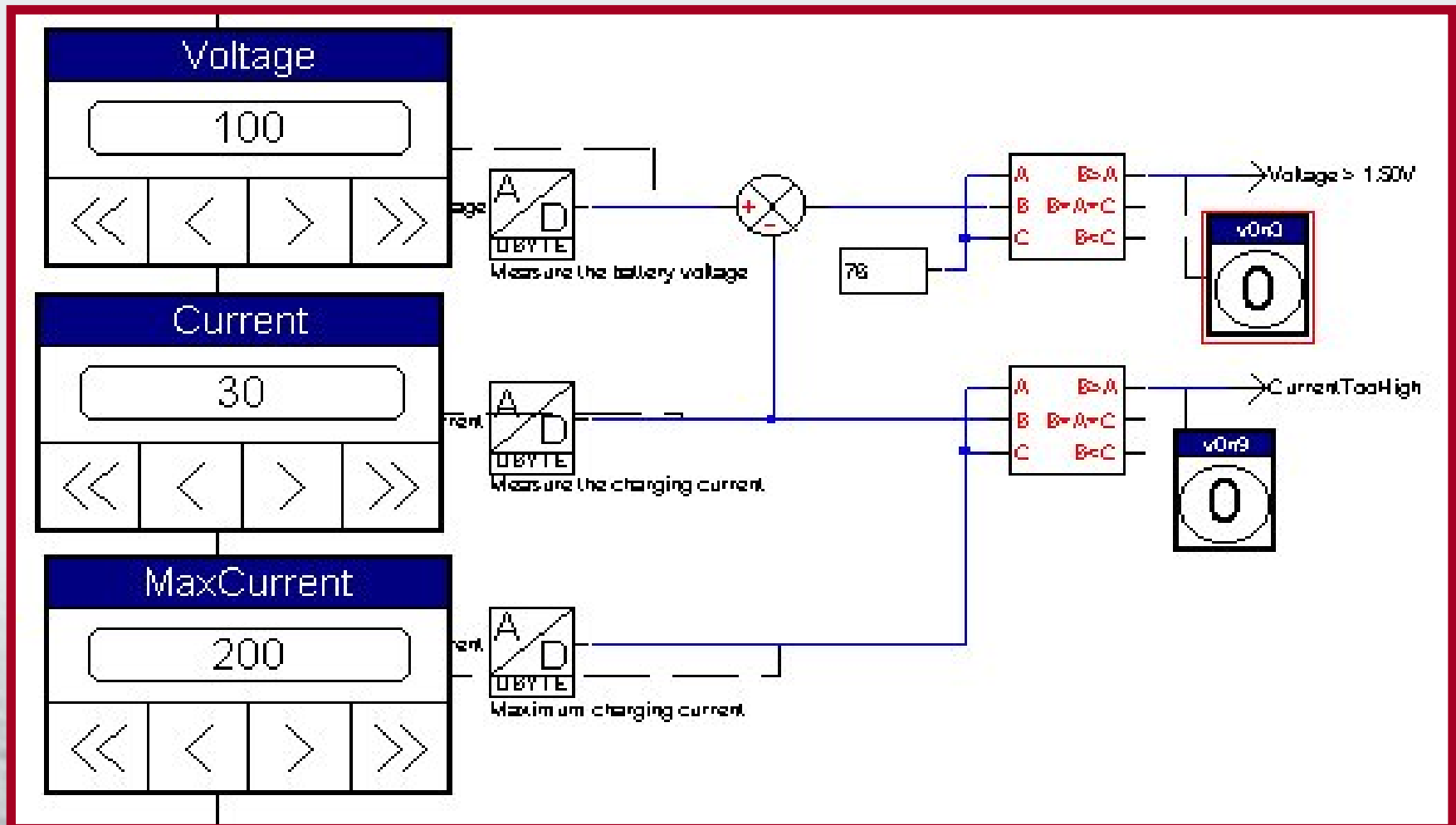
- STRUCTURE OF THE CODE



ST-REALIZER

Basic concepts

- SIMULATION



ST-REALIZER

- ADDITIONNAL FEATURES
 - Hierarchical design : subschemes
 - User-defined symbols
- RESULT
 - Clear design structure
 - Top down approach
 - Re-use of existing part
 - Flexibility
 - No assembly to write



ST-REALIZER

Advantages

- COMFORTABLE USER INTERFACE
- SELF DOCUMENTED DESIGN
- SHORT DESIGN CYCLE
 - Concept, design, development, test
- COMPLETE ERROR-FREE CODE
- DEVICE INDEPENDENT
 - Type, family, vendor
- POWERFUL INTERACTIVE & FUNCTIONAL SIMULATION
- NO NEED TO LEARN ASSEMBLY
- NO NEED TO LEARN HOW THE MICRO IS WORKING



ST-REALIZER II

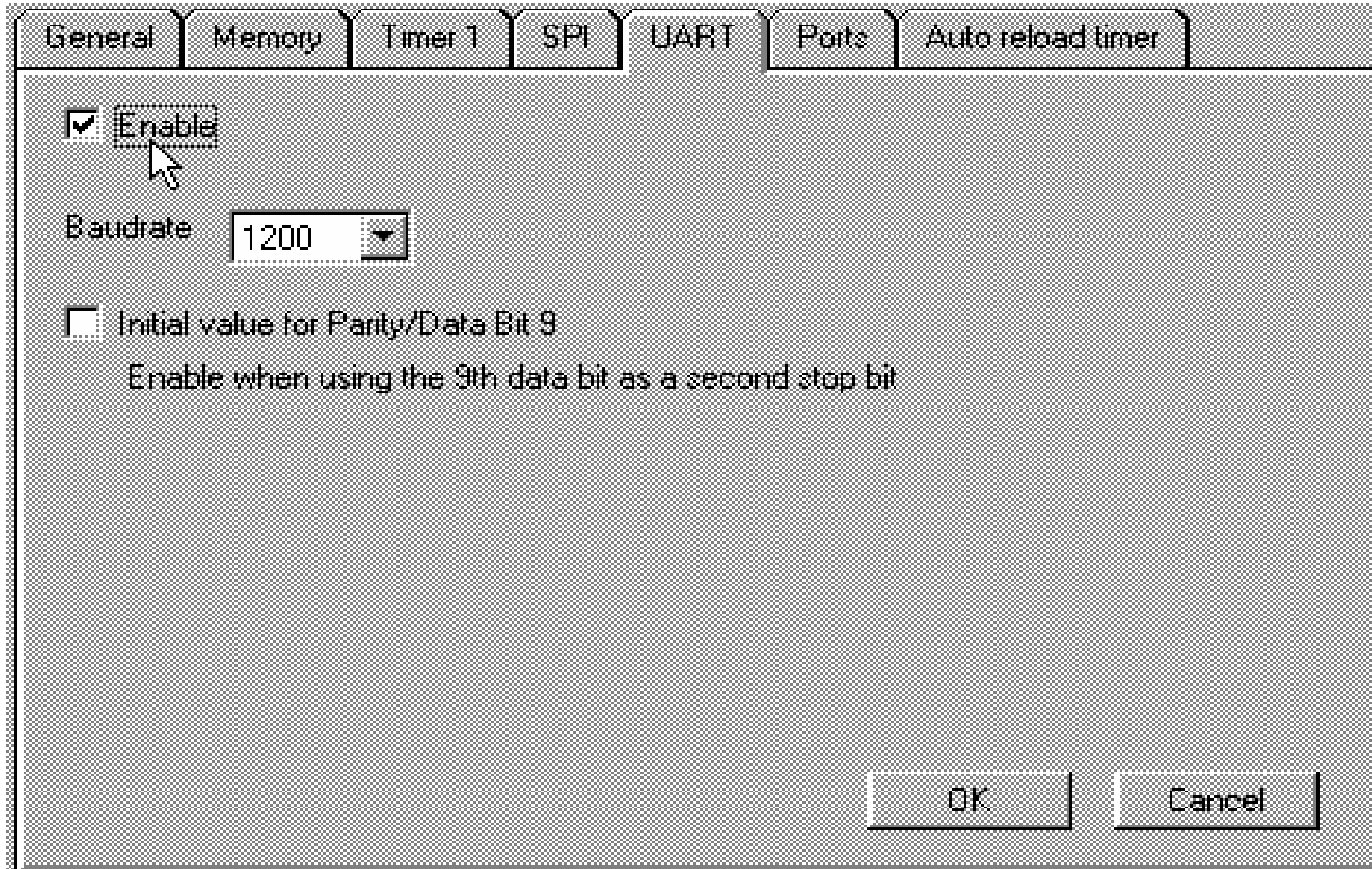
New features

- IMPROVED USER INTERFACE
- SUPPORT FOR INTERRUPTS
- SUPPORT FOR WAIT AND STOP MODE
- LOW LEVEL PERIPHERALS
- NEW SYMBOLS
- CONDITIONAL EXECUTION FOR SUBSCHEMES
- PIN LEVEL SIMULATION



ST-REALIZER II

Low level peripherals



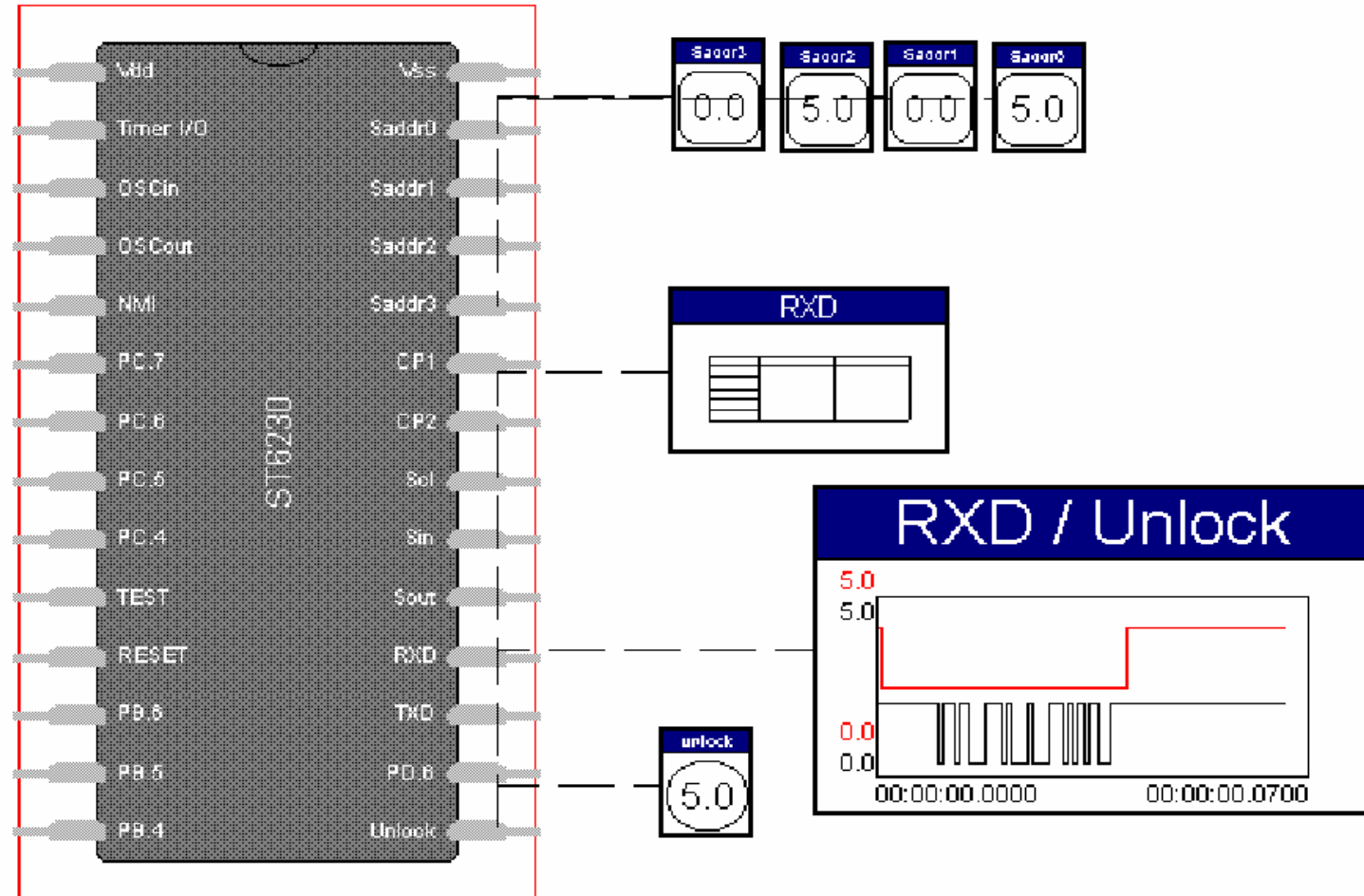
The image shows a configuration dialog box for the UART peripheral in the ST-Realizer II software. The dialog has a tabbed interface with the following tabs: General, Memory, Timer 1, SPI, UART, Ports, and Auto reload timer. The 'UART' tab is currently selected. Inside the dialog, there are three main settings:

- An **Enable** checkbox, which is checked. A mouse cursor is pointing at the checkbox.
- A **Baudrate** field with a dropdown menu, currently set to **1200**.
- An **Initial value for Parity/Data Bit 9** checkbox, which is unchecked. Below this checkbox is the text: "Enable when using the 9th data bit as a second stop bit".

At the bottom right of the dialog, there are two buttons: **OK** and **Cancel**.

ST-REALIZER II

Pin level simulation



REALIZER PRODUCTS

- ACTUM PRODUCTS

- Gold
- Silver
- Bronze

One target module, extendable with others

Available from ACTUM : www.actum.com



- ST-REALIZER II

- ST6 and ST7 Target micros
- Comparable to Silver

Available from ST

