Hello and welcome to this presentation of the STM32 independent watchdog. It covers the main features of this timer able to reset the microcontroller on expiry of a programmed period of time, unless the program refreshes the content of the downcounter before its value becomes equal to 0.
The independent watchdog is used to detect and resolve malfunctions due to software failures.

It triggers a reset sequence when it is not refreshed within the expected time-window. Since its clock is an independent 32-kHz low-speed internal RC oscillator (LSI), it remains active even if the main clock fails. Once enabled, it forces the activation of the low-speed internal oscillator, and it can only be disabled by a reset.

One of the main benefits for applications is its ability to run independently from the main clock.

Since the IWDG belongs to the VDD power domain, it remains active when the microcontroller enters the STANDBY and SHUTDOWN power states in which the
Vcore power supply is switched off.
The independent watchdog offers a wide range of timeout values: from 125 microseconds to 32 seconds. It is clocked by a 32-kHz RC oscillator which cannot be disabled when the independent watchdog is enabled. It generates a reset when the programmed timeout value elapses, or when a watchdog refresh occurs outside a programmed time-window.

It is possible to automatically enable the independent watchdog after a system reset thanks to the device option bits. It is possible to define the behavior of the independent watchdog in Debug mode.

Once running, the IWDG cannot be stopped. It remains active in Stop and Standby modes.
The independent watchdog registers are located in the CORE voltage domain while its functions are in the VDD voltage domain.

Two clocks are needed:
- The APB clock is required in order to access registers
- The LSI clock is required for the functional part of the watchdog

This architecture allows the independent watchdog to remain active even in Stop, Standby and Shutdown modes.

A programmable 8-bit prescaler is used to divide the LSI oscillator frequency.

The 12-bit downcounter defines the timeout value.
This diagram illustrates how the independent watchdog operates. When the downcounter reaches zero, the watchdog reset is activated. This happens when the application software did not refresh the window watchdog on time.

If the software refreshes the watchdog while the downcounter is greater than the value stored in the Window register, then a reset is generated as well. To prevent a watchdog reset, the refresh must occur when the downcounter value is other than zero, and lower than the time-window value.
The independent watchdog hardware is enabled by the device’s option bytes. If the hardware mode is enabled, after every system reset, the watchdog automatically loads the down-count with 0xFFF, and starts to count down. To prevent any reset, the Key register must be refreshed at regular intervals before the counter reaches 0 and within the time window, if this option has been selected.
The independent watchdog software start is configured in only a few steps.

- The first step is to write the Key register with value 0x0000_CCCC which starts the watchdog.
- Then remove the independent watchdog register protection by writing 0x0000_5555 to unlock the key.
- Set the independent watchdog prescaler in the IWDG_PR register by selecting the prescaler divider feeding the counter clock.
- Write the reload register (IWDG_RLR) to define the value to be loaded in the watchdog counter.

After accessing the previous registers, it is necessary to wait for the IWDG_SR bits to be reset in order to confirm that the registers have been updated.
Two options are now available: enable or disable the independent watchdog window option.

- To enable the window option, write the window value in the IWDG_WINR register.
- Otherwise, refresh the counter by writing 0x0000_AAAA in the Key register to disable the window option.
The IWDG time base is prescaled from the LSI clock at 32 kHz. The IWDG_PR prescaler register can divide the LSI clock frequency by 4 up to 256. The watchdog counter reload value is a 12-bit value written in the IWDG_RLR register.

A formula can be used to determine the independent watchdog timeout. The independent watchdog time is based on the LSI period and its prescaler, as well as the selected watchdog counter reload value.

Note that the Reset and Clock Controller (RCC) unit provides registers indicating the source of the reset. In that way the boot program can check if the reset was caused by the independent watchdog.
Low-power modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Run</td>
<td>Active*</td>
</tr>
<tr>
<td>Sleep</td>
<td>Active*</td>
</tr>
<tr>
<td>Stop 0</td>
<td>Active*</td>
</tr>
<tr>
<td>Stop 1</td>
<td>Active</td>
</tr>
<tr>
<td>Standby</td>
<td>Active</td>
</tr>
<tr>
<td>Shutdown</td>
<td>Active</td>
</tr>
</tbody>
</table>

* If IWDG enabled

The IWDG can be active in all modes. So when low-power modes are implemented, periodic wakeups are required to service the watchdog if the microcontroller state has to be preserved.