

# STM32MP1 – Arm® MPU Core

Arm® Cortex® -A7  
Revision 2.0

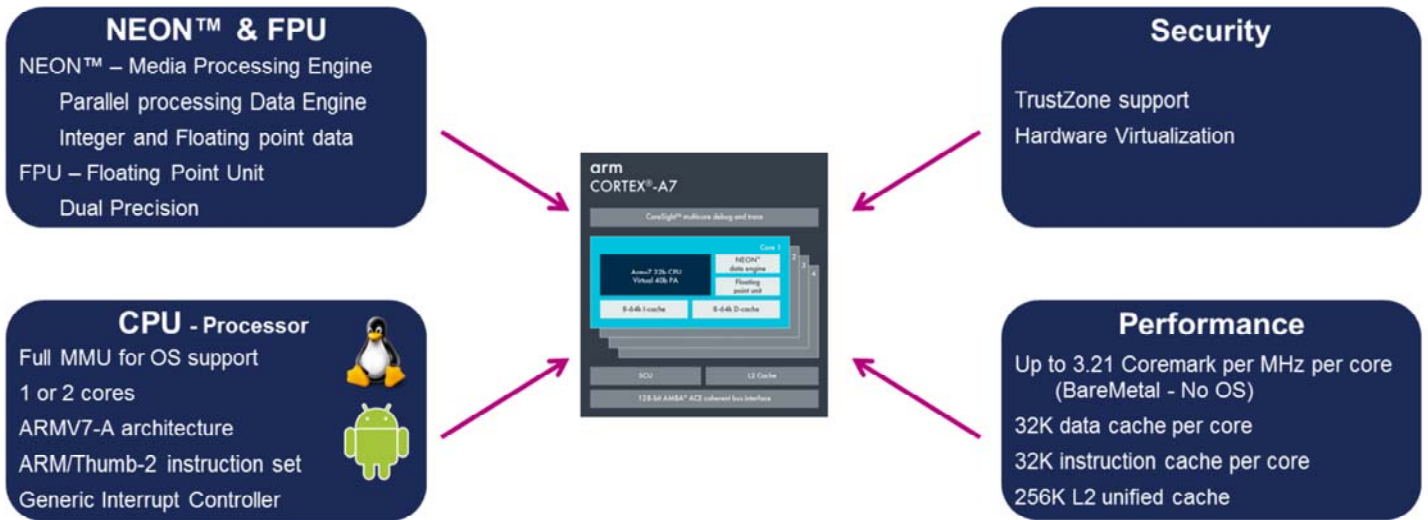


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Hello, and welcome to this presentation of the STM32MP1  
Arm® MPU Core.

# Arm<sup>®</sup> Cortex-A7<sup>®</sup> Core

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STM32MP1 series integrates a Cortex-A7<sup>®</sup> core from Arm in order to support a range of full Operating Systems including Linux, Android with high level of performance and a low power consumption.

Cortex-A7 core includes one or two 32-bit cores with complete SMP support with full HW coherence. Cortex-A7 core also supports Trustzone security with separated secure and non-secure execution modes.

Each core includes a 32 Kbytes data and 32 Kbytes instruction caches and a common unified level-two cache of 256 Kbytes, all having zero wait states and running at processor speed.

NEON<sup>®</sup> is an advanced Simple Instruction Multiple Data (SIMD) instruction set for further acceleration of media and signal processing functions. An single and double-precision FPU is also present.

A generic interrupt controller supports up to 224 interrupt lines with security and multicore routing.

- For more details, please refer to Arm<sup>®</sup> website at the following link:
  - <https://www.arm.com/products/processors/cortex-a/cortex-a7.php>



For more details, please refer to Arm<sup>®</sup> website in which you will find all information about the Cortex-A7 core.