Hello, and welcome to this introduction to the STM32WB Series training session. It describes the feature sets of the various lines available in the STM32WB microcontroller series.
The block diagram for STMWB devices is provided here for reference. The STM32WB proposes a variety of communication assets, a practical crystal-less USB2.0 FS interface, audio support, an LCD driver, up to 72 GPIOs, an integrated SMPS for power consumption optimization, and multiple low-power modes to maximize battery life. The independent radio frequency module with an integrated balun also offers high-performance wireless connectivity, running BLE/OpenThread protocols concurrently. On top of wireless and ultra-low-power aspects, a particular focus was placed on embedding security hardware functions such as a 256-bit AES, PCROP, JTAG Fuse, PKA (elliptic curve encryption engine), and Root Secure Services (RSS). The RSS allows authenticating OTA communications, regardless of the radio stack or application.
This slide lists some specific features of the STMWB55 microcontroller.

- An integrated autonomous operating Radio sub-system
- A dual-core architecture, where only the application processor boots after reset. The connectivity processor only boots once enabled by the application.
- A single-bank Flash memory, shared by the 2 CPUs, and accessed via a separate AHB bus in the common Run domain.
- A Cortex-M0+ dedicated memory (Flash, SRAM2) and peripheral security.
- A Single frequency HSE at 32 MHz.
- Two LSIs, the standard STM32 low-power LSI1 and a low drift LSI2 to be used when the wireless connectivity is active.
Specific STM32WB features 2/2

- SRAM2 split in 2 parts
  - SRAM2a backup RAM
  - SRAM2b non-backup RAM
- Debug Cross trigger unit including trigger in/out.
- Integrated SMPS to supply Core and Radio LDO’s.

These are additional specific features versus other STM32Ss microcontrollers:
- The SRAM2 is split in 2 parts: SRAM2s is a backup part while SRA%2b is a non-backup part.
- A debug cross trigger unit allows the use of a trigger input/output on a I/O port.
- An integrated Switching Mode Power Supply (SMPS) provides an intermediate voltage for the Core and radio LDOs.
The STM32WB series can be encapsulated in a wide range of packages.
Note that the UQFN package has 7 dedicated Radio pins and 4 dedicated SMPS pins.