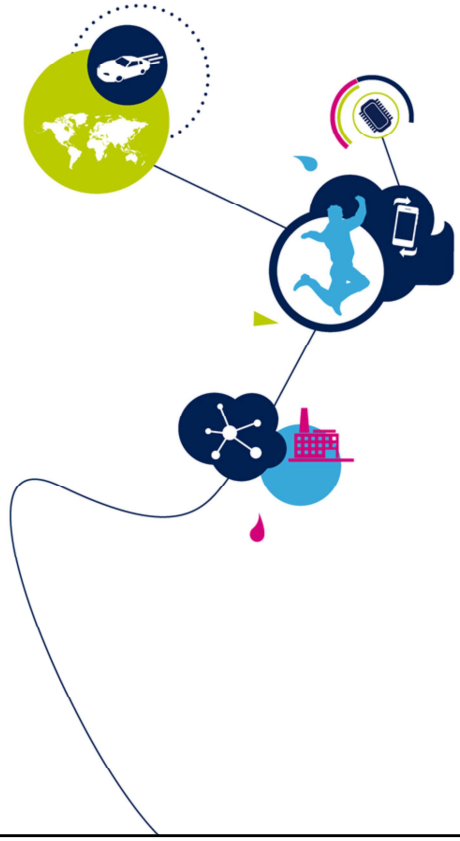
STM32H7 - GPIO

General-purpose input/output interface
Revision 1.0



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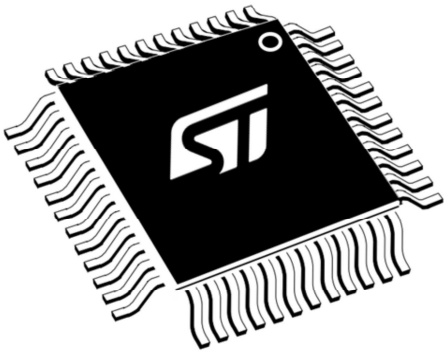
Hello, and welcome to this presentation of the STM32 general-purpose IO interface. It covers the general-purpose input and output interface and how it allows connectivity to the environment around the STM32 microcontroller.

Overview



- Provides an interface for interaction with the external environment
  - Fully configurable
  - Interrupt and wake-up capability
  - Direct connection to AHB bridge

Application benefits

- Direct microcontroller wake-up
- Supports a wide range of supply voltages
- Direct connection to AHB allows fast toggle response

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The general-purpose IO pins of STM32 products provide an interface with the external environment. This configurable interface is used by the MCU as well as the other embedded peripherals to interface with both digital and analog signals. Application benefits include a wide range of supported IO supply voltages, as well as the ability to externally wake up the MCU from low-power modes.

Key features

- Bi-directional operation of up to 168* I/O pins
  - Shared across 11 GPIOx ports named GPIOA to GPIOK, with up to 16 I/O pins per port
  - All with external interrupt and wake-up capabilities
  - Atomic bit set and bit reset operations using BSRR and BRR registers
  - Independent configuration for each I/O pin
  - I/O pin in analog mode after reset
- GPIO register interface is directly connected to D3 AHB4 bus
- Most I/O pins are 5 V tolerant when V_{DD} is above 1.62 V

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** : depends on part numbers and packages*

The general-purpose I/O ports provide bidirectional operation according to the input memory map.
I/O ports are directly connected to the AHB bus. This allows fast I/O pin operations, e.g. toggling and output, with an independent configuration for each I/O pin. They are shared across 11 ports named GPIOA to GPIOK, each of them hosting up to 16 I/O pins. After reset, all GPIOs are in Analog mode to reduce power consumption.
I/O ports support atomic bit set and reset operations through the BSSRR and BRR registers. It allows I/O toggling every 2 clock cycles.
Most of the I/O pins are 5 V tolerant when supplied from V_{DD} above 1.62 V.

Operating modes

Flexible operating modes to best fit application needs

- Input modes
  - Floating (no pull resistor), input with pull-up/down, and analog input modes
- Output modes
  - Push-pull and open-drain modes with optional pull-up/down
- Configurable output slew rate speed
- Alternate function mode
- Locking mechanism to freeze the I/O port configuration (GPIOx_LCKR)

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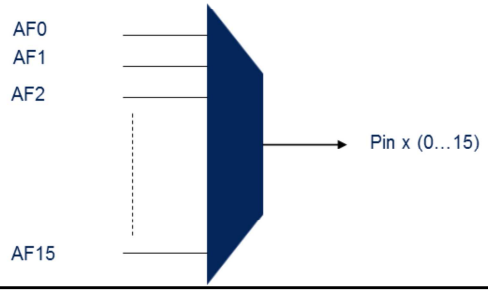
General-purpose I/O pins can be configured for use in several operating modes.
An I/O pin can be configured in an input mode with floating input, input mode with an internal pull-up or pull-down resistor or as an analog input.
An I/O pin can be also configured in an output mode with a push-pull output or an open-drain output with an internal pull-up or pull-down resistor.
For each I/O pin, the slew rate speed can be selected from 4 ranges for the best compromise between maximum speed and emissions from the I/O switching and to adjust the application's EMI performance.
I/O pins are also used by other embedded peripherals to interface with the external environment. Alternate function registers are used to select the configuration for the peripherals in this case.
The configuration of the I/O ports can be locked to

increase robustness of the application. Once the configuration is locked by applying the correct write sequence to the lock register, the I/O pin’s configuration cannot be modified until the next reset.

Alternate functions

Structure of I/O pins is used as an interface by other embedded peripherals

- Several embedded peripherals share the same I/O pins
  - Including USARTx_TX, TIMx_CHx, SPIx_MISO, EVENTOUT, …
- Alternate function multiplexer selects the peripheral connected to the I/O pin
  - Only one alternate function is connected to a specific I/O pin at a single time
  - Configurable through the GPIOx_AFRL and GPIOx_AFRH registers



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Several integrated peripherals such as the USART, timers, SPI and others share the same I/O pins in order to interface with the external environment.
Peripherals are configured through an alternate function multiplexer which ensures that only one peripheral is connected to an I/O pin at a single time. Of course, this selection can be changed while the application is running through the GPIOx_AFRL and AFRH registers.

Special considerations for I/O pins

Only debug pins remain in AF mode under reset

- During and after reset, the alternate functions are not active
  - I/O ports default state to input mode
  - To reduce current consumption, IOs may be configured in Analog mode
- Only JTAG/SWD debug pins remain in AF pull-up/pull-down configuration
  - PA13: JTMS/SWDIO
  - PA14: JTCK/SWCLK
  - PA15: JTDI
  - PB3: JTDO
  - PB4: NJTRST

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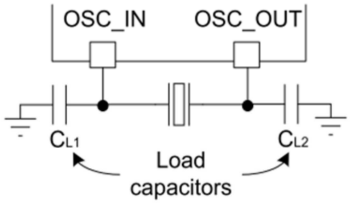
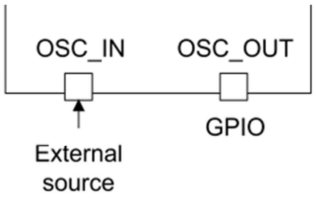
During and after reset, the alternate functions are not active.
Only debug pins remain in AF mode.
JTAG/SWD debug pins remaining in AF configuration mode are listed in this slide.

Special considerations for HSE/LSE pins

Oscillator pins can be used as standard I/O pins

- When the oscillator is switched OFF, related pins behave as I/O pins
  - Valid for both HSE / LSE
  - This state is the default one after reset
- When user external clock mode is used, the second pin behaves as an I/O pin
  - Only OSC_IN or OSC32_IN is used as clock source
  - OSC_OUT and OSC32_OUT are standard I/O pins





When the external oscillator is switched off, pins related to this oscillator can be used as standard I/O pins. This is the default state after device reset.
When the external clock source is used instead of a crystal oscillator, only the related OSC_IN pin is used for the clock and the OSC_OUT pin can be used as a standard I/O pin.

I/O compensation cell

- This cell is used to control the I/O commutation slew rate
- Two configuration modes are available:
  - Using optimal configuration code calculated by the cell for the current PVT (Process Voltage Temperature).
    - This code is generated and the READY flag is set when the CSI clock is enabled and the cell is enabled
  - Using software programmed code to control the I/O slew rate.
- The I/O compensation cell features two voltage ranges: 1.62 to 2.0 V and 2.7 to 3.6 V.

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This cell is used to control the I/O commutation slew rate (t_{fall}/t_{rise}) to reduce I/O noise on the power supply.
The cell is split into two blocks. The first block provides an optimal code for the current Process Voltage Temperature (PVT). The code stored in this block can be read when the READY flag of the SYSCFG_CCSR register is set.
The second block controls the I/O slew rate. The user selects the code to be applied and programs it by software.
The I/O compensation cell features two voltage ranges: 1.62 to 2.0 V and 2.7 to 3.6 V.

I/O speed optimization

- No compromise on communication interfaces at low-voltage
  - High-speed IO configuration bit in the SYSCFG_CCCSR register
- Activating the HSLV bit enables boosting IO performance when the supply voltage is below 2.7 V
- It must be used only when the product supply voltage is below 2.7 V. Setting this bit when V_{DD} is higher than 2.7 V may be destructive.
  - This bit can be activated only if the IO_HSLV user option bit is set in the FLASH_OPTSR register.

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Optimizing the I/O speed when the product voltage is low is allowed by setting the High-speed IO configuration bit in the SYSCFG_CCCSR register.
This bit is active only if the IO_HSLV user option bit is set in the FLASH_OPTSR register. It must be used only when the product supply voltage is below 2.7 V. Setting this bit when V_{DD} is higher than 2.7 V may be destructive.

Direct path to the ADC

- Some pins are directly connected to the Analog to Digital Converter (ADC):
  - PA0_C,
  - PA1_C,
  - PC2_C
  - and PC3_C
- An analog switch can connect these pins directly to the ADC analog inputs
- Connections are handled through the System Configuration Controller (SYSCFG)

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Some pins/balls are directly connected to PA0_C, PA1_C, PC2_C and PC3_C ADC analog inputs. There is a direct path between Pxy_C and Pxy pins/balls, through an analog switch.
Connections are handled through the System Configuration Controller (SYSCFG).