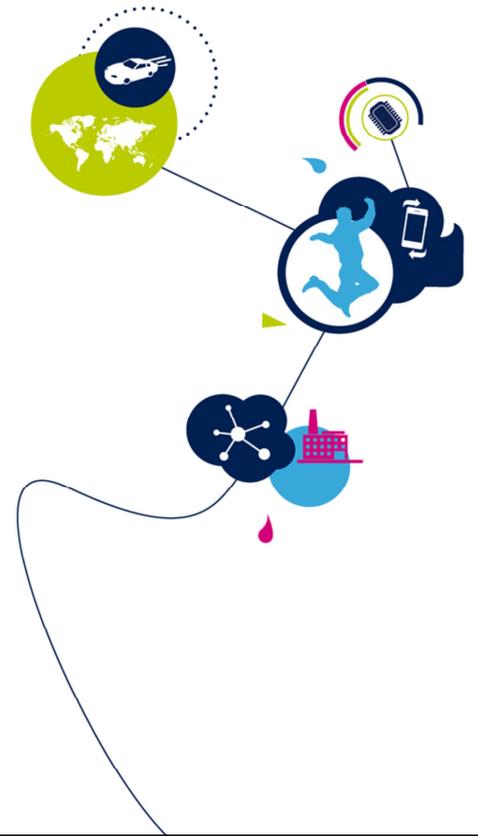


STM32H7 -EXTI

Asynchronous interrupts and events controller
Revision 1.0



Hello, and welcome to this presentation of the STM32H7
Asynchronous interrupts and events controller.

- Up to 89 events / interrupt lines
 - 28 configurable events
 - 61 direct events
- Independent masks and configuration

Application benefits

- Manage external and internal wakeup events / interrupts
- Independent wakeup for CPUs and the D3 domain
- Provide pending flag for configurable events



The EXTI controller provides up to 89 independent events, split into two categories:

- configurable events
- direct events

The EXTI controller can be configured to wake up CPU1, CPU2 or both independently. It can also be used to wake up only the D3 Domain for autonomous operation.

Applications benefit through smarter use of low-power modes, taking advantage of the capability to wake up via external communication or requests.

- Wakeup from Stop mode, interrupt and event generation functions
 - Independent interrupt and event mask for CPUs and the D3 domain
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
 - Active edge selection
 - Dedicated pending flag
 - Trigger-able by software
 - Configurable wakeup events part of the D3 domain have a D3 pending mask and status register and may have a D3 interrupt signal
 - Status flag provided by related peripheral



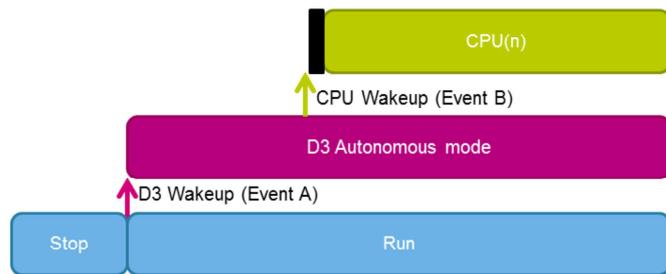
The EXTI controller provides interrupt and event generation functions, as well as the capability to wake up the processors and the D3 domain from Stop modes. Configurable events allow the user to select which active edge generates an interrupt or event, with a dedicated status flag for each line. Requests on configurable lines can also be generated by software. Configurable events are linked with external interrupts from general-purpose input/outputs, comparators, programmable voltage detector, real-time clock, low-power timer, window watchdog, Ethernet controller and HDMI-CEC.

- Direct events (interrupt and wakeup sources from other peripherals, requiring to be cleared in the peripheral)
 - Fixed rising edge active trigger
 - No interrupt pending status register bit in the EXTI (the interrupt pending status is provided by the peripheral generating the event)
 - Individual Interrupt and Event generation mask
 - No SW trigger possibility
 - Direct wakeup events part of the D3 domain have a D3 pending mask and status register and may have a D3 interrupt signal



Direct events provide an interrupt or event from peripherals having a status flag requiring to be cleared. For direct events that are part of the D3 domain and which have a pending mask and status register, an interrupt may be generated.

- When the system is in Run mode, a CPU can be woken up from CStop mode from its domain in DRun, DStop or DStandby.
 - i.e. D3 Autonomous waking up of a CPU.
- Each CPU and the D3 domain must clear its own wakeup events.



EXTI wakeup events may be configured to wakeup a CPU or the D3 domain.

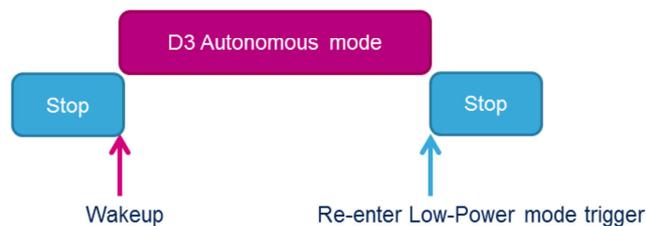
Configurable events need to be cleared by the corresponding CPU which has been awoken.

The D3 domain wakeup events must be cleared by the D3 domain.

D3 Autonomous mode

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- The D3 Domain can be woken up in Autonomous mode from:
 - GPIO, RTC wakeup, COMPx, I2C4, LPUART1, SPI6, and LPTIM2, 3, 4, and 5.
- The D3 Autonomous mode can re-enter low-power mode by a trigger from
 - BDMA ch6 and ch7
 - LPTIM4 output
 - LPTIM5 output



Some peripherals are able to wake up the D3 domain Autonomous mode, where both CPUs remain in CStop mode.

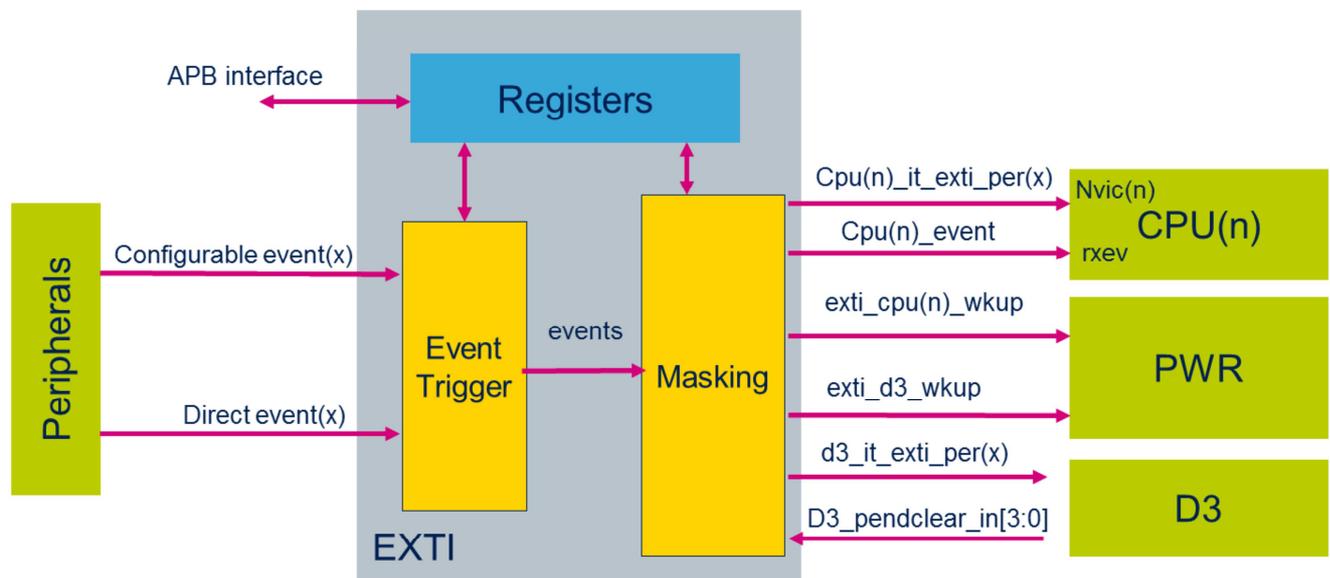
In this mode, the D3 domain is able to transfer data between communication peripherals and memory using the BDMA and DMAMUX2. The BDMA trigger is used to clear the D3 autonomous mode wakeup event and re-enter low-power mode.

The timers can be used to wakeup the D3 domain Autonomous mode on regular basis, i.e. to perform polling tasks.

In addition, timers can be used to clear the D3 autonomous mode wakeup event and re-enter low power mode.

EXTI block diagram

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As shown in this figure, the EXTI consists of a register block accessed via an APB interface, an event input trigger block, and a masking block.

The register block contains all EXTI registers.

The event input trigger block provides event input edge triggering logic.

The masking block provides the event input distribution to the different wakeup, interrupt and event outputs, and their masking.