Hello, and welcome to this introduction to the STM32H7 Series training session.
It describes the feature sets of the various lines available in the STM32H7 microcontroller series.

CORE, MEMORIES AND ACCELERATION
- Single-core Cortex-M7 up to 550 MHz
- Dual-core Cortex-M7 480 MHz and Cortex-M4 240 MHz
- Flash and RAM acceleration
- SP-FPU and DP-FPU
- 4 x DMA
- Mathematics (only H723/733/725/735/730)

CONNECTIVITY
- Up to 2 x USB2.0 OTG FS/HS
- 2 x SDMMC
- USART, UART, SPI, I²C
- Up to 3 x CAN (2 x FD and 1 x TT)
- HDMI-CEC
- FMC, Dual-mode Quad-SPI or 2 x Octo-SPI
- Camera I/F

AUDIO
- 3 x I²S + audio PLL
- 4 x SAI
- 2 x 12-bit DAC
- SPDIF-RX

GRAPHIC
- Chrom-ART Accelerator™

OTHER
- Crypto/Hash option (except H742)
- Security services option (except H742)
- TRNG
- DFSDM
- 16- and 32-bit timers
- HRTimer (except STM32H7A/H7B/H7B0/H723/H725/H730/H733/H735 +
- Up to 3 x 16-bit ADC (up to 3.6 MSPS)
- 1 x 12-bit ADC (up to 5 MSPS) (only on H723/733/725/735/730)
- Analog (comp, AOP)
- Voltage range 1.62 to 3.6 V (except 100-pin and VFQFPN68 packages : 1.71 to 3.6 V)
- Multi-power domains
- -40°C up to 85°C ambient
- -40°C up to 125°C ambient[2]

Product line	f_{max} (MHz)	Dual-Bank Flash memory (bytes)	RAM (bytes)	OctoSPI & OT - FDEC	Ethernet	Graphic	Power supply	Stop mode (typical) / RAM reten - tion
Dual-core lines								
STM32H747/757[1]	480 + 240	Up to 2 Mbytes	1 Mbyte (incl.128 Kbytes DTCM + 64 Kbytes ITCM + 64 Kbytes backup1) + 4 Kbytes backup2		•	TFT-LCD JPEG codec MIPI-DSI	SMPS + LDO	360 µA / 1 MB 250 µA / 768KB
STM32H745/755[1]	480 + 240	Up to 2 Mbytes	1 Mbyte (incl.128 Kbytes DTCM + 64 Kbytes ITCM + 64 Kbytes backup1) + 4 Kbytes backup2		•	TFT-LCD JPEG codec	SMPS + LDO	360 µA / 1 MB 250 µA / 768KB
Single-core lines								
STM32H7A3/7B3[1]	280	Up to 2 Mbytes	1,4MB (incl.128K DTCM, 64K ITCM, 1184K+SRAM, 4K backup)	•		TFT-LCD JPEG codec Chrom-GRC	SMPS + LDO	32 µA / 1.4MB 28 µA / 32KB
STM32H743/753[1]	480	Up to 2 Mbytes	1 Mbyte (incl.128 Kbytes DTCM + 64 Kbytes ITCM + 64 Kbytes backup1) + 4 Kbytes backup2		•	TFT-LCD JPEG codec	LDO	1270 µA / 1MB 910 µA / 768KB
STM32H742	480	Up to 2 Mbytes	692 Kbytes (incl.128 Kbytes DTCM + 64 Kbytes ITCM + 16 Kbytes backup1) + 4 Kbytes backup2		•		LDO	1270 µA / 692KB 910 µA / 704KB
STM32H725/735[2]	550	Up to 1 Mbyte	564KB (incl.128K DTCM, 432KB Syst + 4K bckup)		•	TFT-LCD	SMPS[3] + LDO	200 µA / 564KB
STM32H723/733[3]	550	Up to 1 Mbyte	564KB (incl.128K DTCM, 432KB Syst + 4K bckup)		•	TFT-LCD	LDO	520 µA / 564KB
Value line								
STM32H7B0	280	128 Kbytes	1,4MB (incl.128K DTCM, 64K ITCM, 1184K+SRAM, 4K backup)	•		TFT-LCD JPEG codec Chrom-GRC	SMPS + LDO	32 µA / 1.4MB 28 µA / 32KB
STM32H750	480	128 Kbytes	1 Mbyte (incl.128 Kbytes DTCM + 64 Kbytes ITCM + 64 Kbytes backup1) + 4 Kbytes backup2		•	TFT-LCD JPEG codec	LDO	1270 µA / 1MB 910 µA / 768KB
STM32H730	550	128 Kbytes	564KB (incl.128K DTCM, 432KB Syst + 4K bckup)		•	TFT-LCD	SMPS[4] + LDO	200 µA / 564KB 520 µA / 564KB

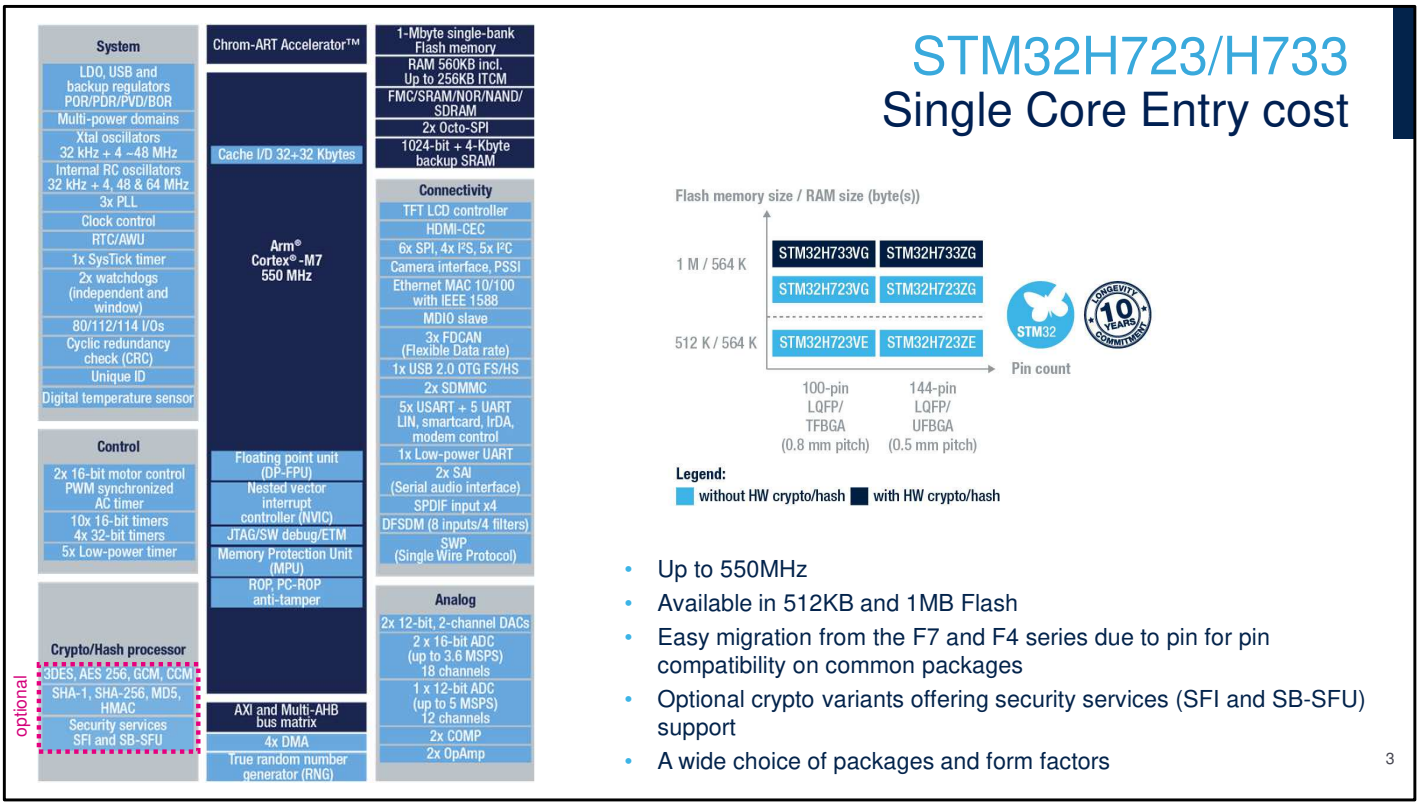
Notes :
1. Optional - dedicated CPN, STM32H733, STM32H735, STM32H753, STM32H755, STM32H757, STM32H7B3 for the Crypto Variants
2. 125 °C ambient / 140 °C junction. Dedicated part numbers on STM32H725/H735, STM32H745/H755
3. Crypto and Security services on CPN : STM32H730, STM32H735 and STM32H750
4. SMPS available only on STM32H730Q CPN
5. SMPS only on the QFN68 variant (no LDO)

STM32H7 High performance Tailored for your needs

- Single and Dual core versions
- High performance up to **480MHz** in Dual core and up to **550MHz** in Single core
- 128KB to 2MB Flash Dual Bank
- Up to 1.4MB RAM
- More security features (Boot, Tamper …), OTFDEC on external memories, Crypto/Hash and security services (optional)
- 35 communication peripherals
- 16-bit ADC up to 3.6Msps, up to 5 MSPS in 12-bit, Comparators, Op Amp
- TT-FD-CAN and FD-CAN
- High-Resolution timer (2.1ns)
- Low-Power Timers
- LDO and SMPS option
- Up to 140 °C junction temperature / 125 °C ambient (optional)

2

The STM32H7 series of very high-performance MCUs comes with an ARM® Cortex®-M7 core and an optional ARM® Cortex®-M4 core for a dual-core CPN.
Taking advantage of up 2 x 32-Kbytes L1 cache for instruction and data, the STM32H7 devices deliver the maximum theoretical performance of the Cortex-M7 core no matter whether the code is executed from the embedded Flash or from the external memory: 2424 CoreMark /1027 DMIPS at 480 MHz fCPU1 and 2778 CoreMark/1177 DMIPS at 550MHz fCPU1.
In dual core variants, the Cortex-M4 core offers 800 CoreMark /300 DMIPS at 240 MHz fCPU2



STM32H723/H733
Single Core Entry cost

- Up to 550MHz
- Available in 512KB and 1MB Flash
- Easy migration from the F7 and F4 series due to pin for pin compatibility on common packages
- Optional crypto variants offering security services (SFI and SB-SFU) support
- A wide choice of packages and form factors

3

The STM32H723/33 line offers the performance of the Cortex-M7 core (with double-precision floating point unit) running at up to 550 MHz. It's L1 cache provides 32 KBytes for instruction and 32 Kbytes for data, the ITCM RAM can be increased to 256 KBytes, all those fast memory accesses boost execution performance.
The STM32H733 integrates a crypto/hash processor providing hardware acceleration for AES-128, -192 and -256, with support for GCM and CCM, Triple DES, and hash (MD5, SHA-1 and SHA-2) functions.

STM32H725/H735
Single Core Entry cost with SMPS

- Up to 550MHz
- Available in 512KB and 1MB Flash
- SMPS power supply
- Optional crypto variants offering security services (SFI and SB-SFU) support
- Optional support of extended Temperature range: 125 ° C on specific part numbers
- A wide choice of packages and form factors

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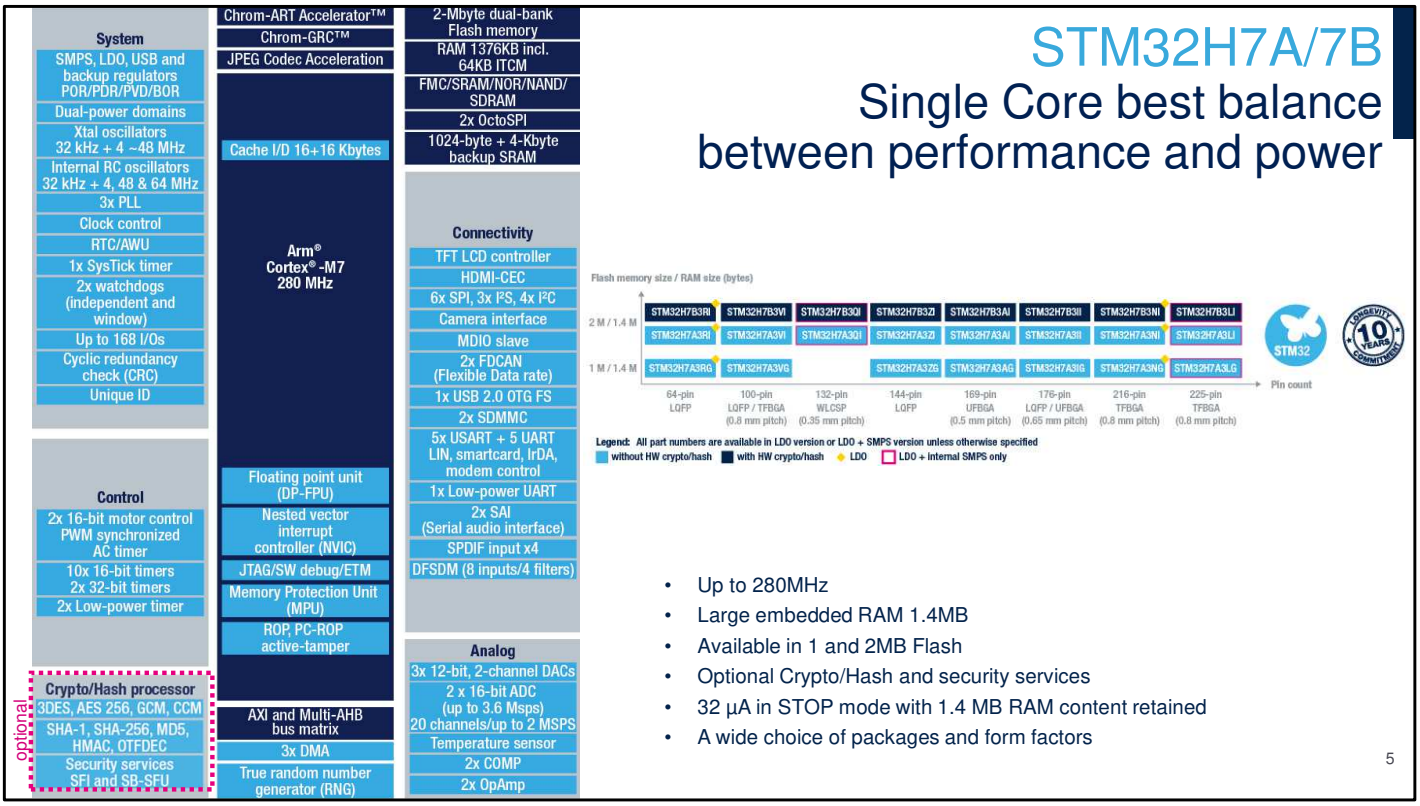
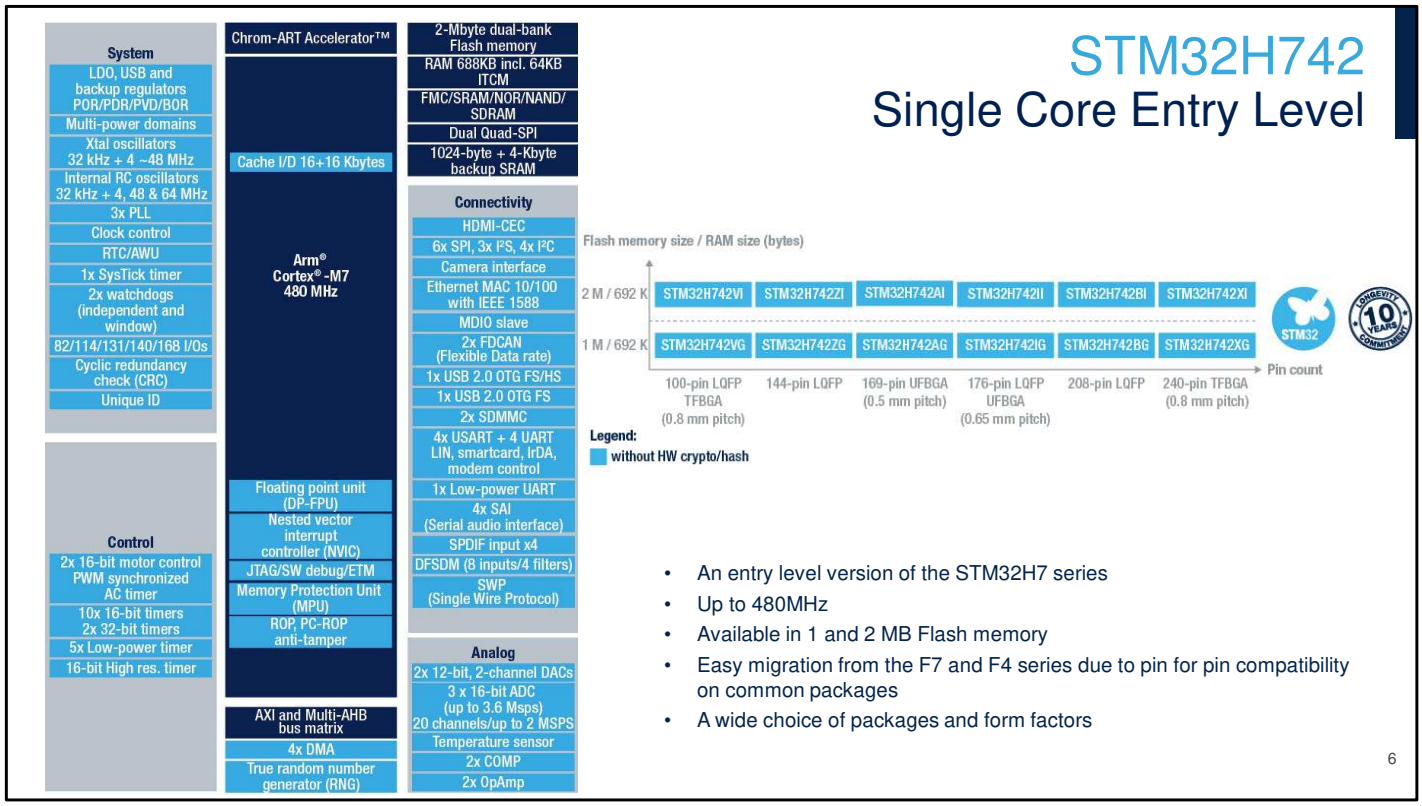
On top of features provided by the STM32H723/33 line, the STM32H725/35 line embeds a SMPS to scale down the supply voltage, decreasing device power consumption. It can also be used to supply external circuitry and can also be combined with the LDO for specific use cases. It proposes an optional extended ambient temperature range up to 125 °C with junction temperature range up to 140°C. The STM32H735 integrates the same crypto function as STM32H733.



The STM32H7A/H7B lines offers the best balance between the performance of the Cortex-M7 core (with double-precision floating point unit) running up to 280 MHz and a very contained power consumption in low power modes for energy sensitive applications. It embeds 1.4 MByte RAM and up to 2 MBytes flash. The STM32H7B integrates a crypto/hash processor providing hardware acceleration for AES-128, -192 and -256, with support for GCM and CCM, Triple DES, and hash (MD5, SHA-1 and SHA-2) functions.



STM32H742
Single Core Entry Level

- An entry level version of the STM32H7 series
- Up to 480MHz
- Available in 1 and 2 MB Flash memory
- Easy migration from the F7 and F4 series due to pin for pin compatibility on common packages
- A wide choice of packages and form factors

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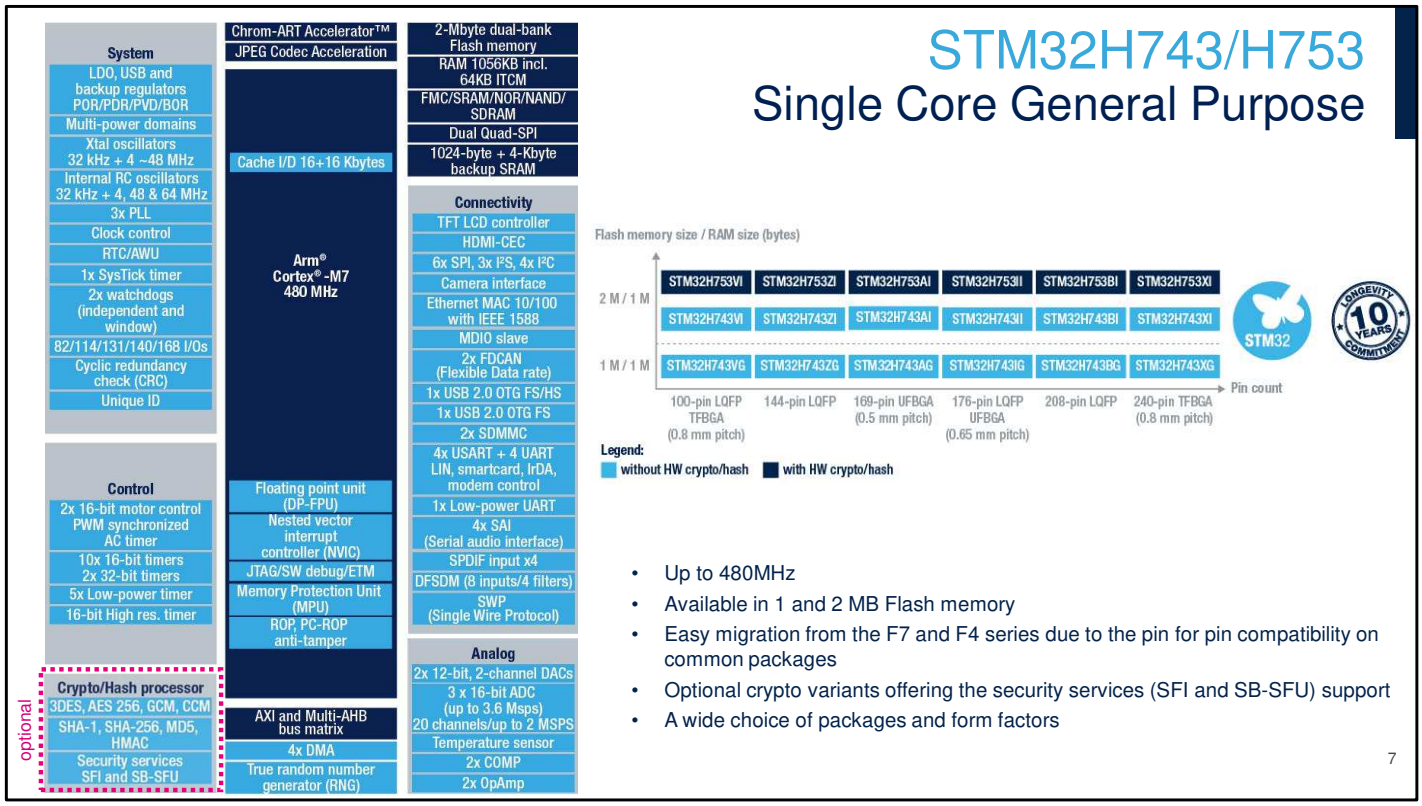
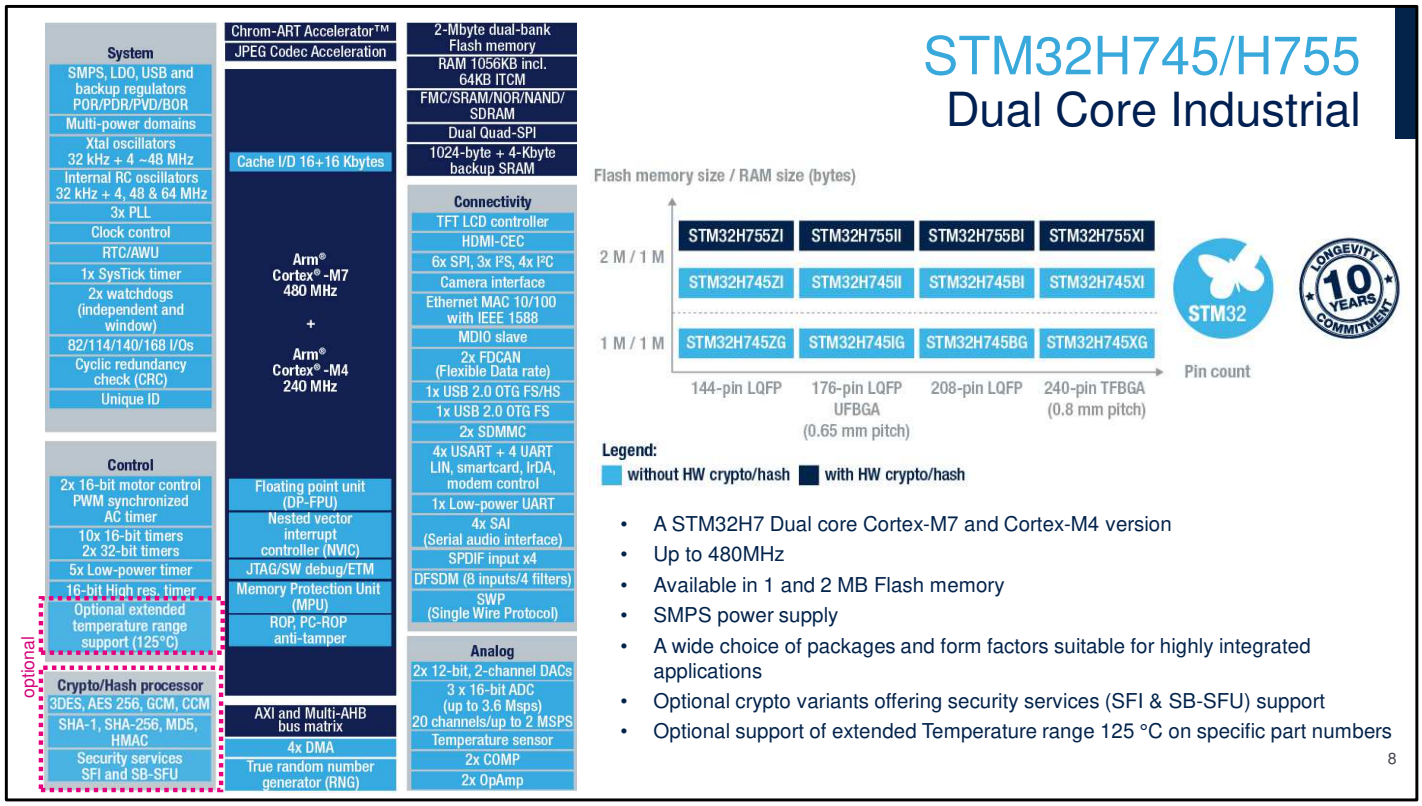
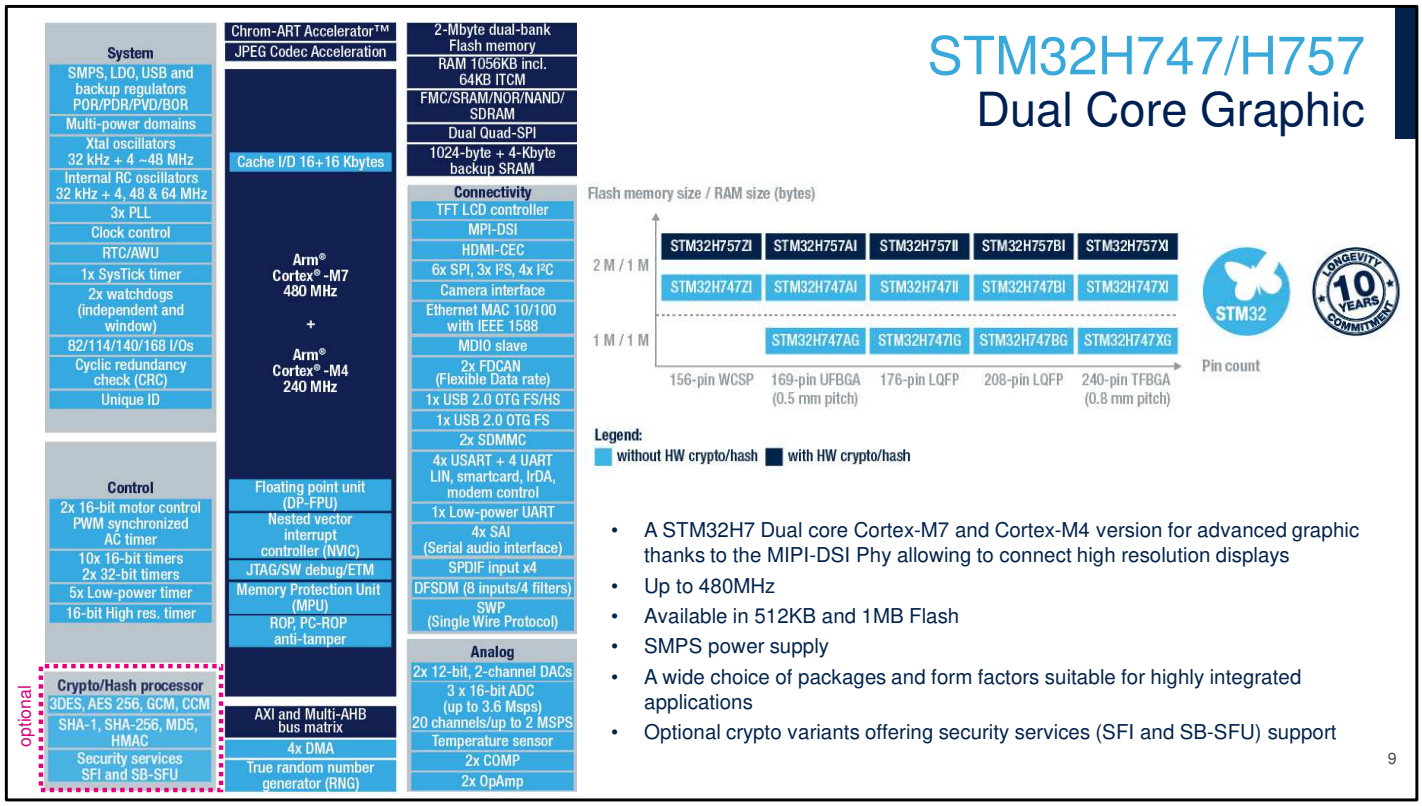
The STM32H742 line offers the performance of the Cortex-M7 core (with double-precision floating point unit) running up to 480 MHz. It embeds up to 2MBytes of Flash. memory



On top of features proposed by the STM32H742 line, the STM32H743/753 line offers more RAM, an LCD-TFT controller interface with dual-layer support, and a JPEG hardware accelerator for fast JPEG encoding and decoding, off-loading the CPU.
The STM32H753 integrates a crypto/hash processor providing hardware acceleration for AES-128, -192 and -256, with support for GCM and CCM, Triple DES, and hash (MD5, SHA-1 and SHA-2) functions.



On top of features proposed by STM32H743/753, the STM32H745/755 embeds a SMPS to scale down the supply voltage, decreasing device power consumption. It proposes an optional extended ambient temperature range up to 125 °C with junction temperature range up to 140°C. The STM32F755 integrates the crypto/hash processor.



STM32H747/H757
Dual Core Graphic

- A STM32H7 Dual core Cortex-M7 and Cortex-M4 version for advanced graphic thanks to the MIPI-DSI Phy allowing to connect high resolution displays
- Up to 480MHz
- Available in 512KB and 1MB Flash
- SMPS power supply
- A wide choice of packages and form factors suitable for highly integrated applications
- Optional crypto variants offering security services (SFI and SB-SFU) support

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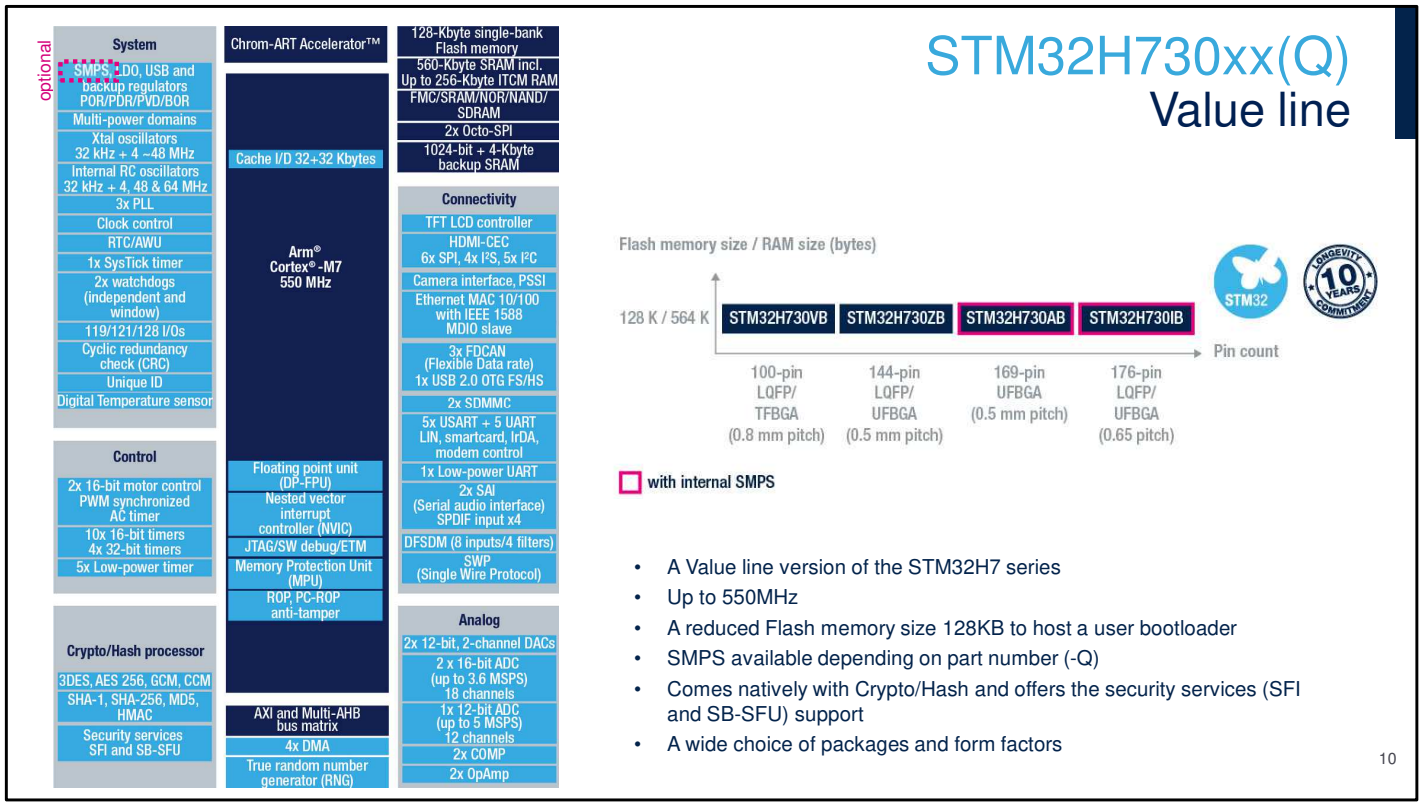
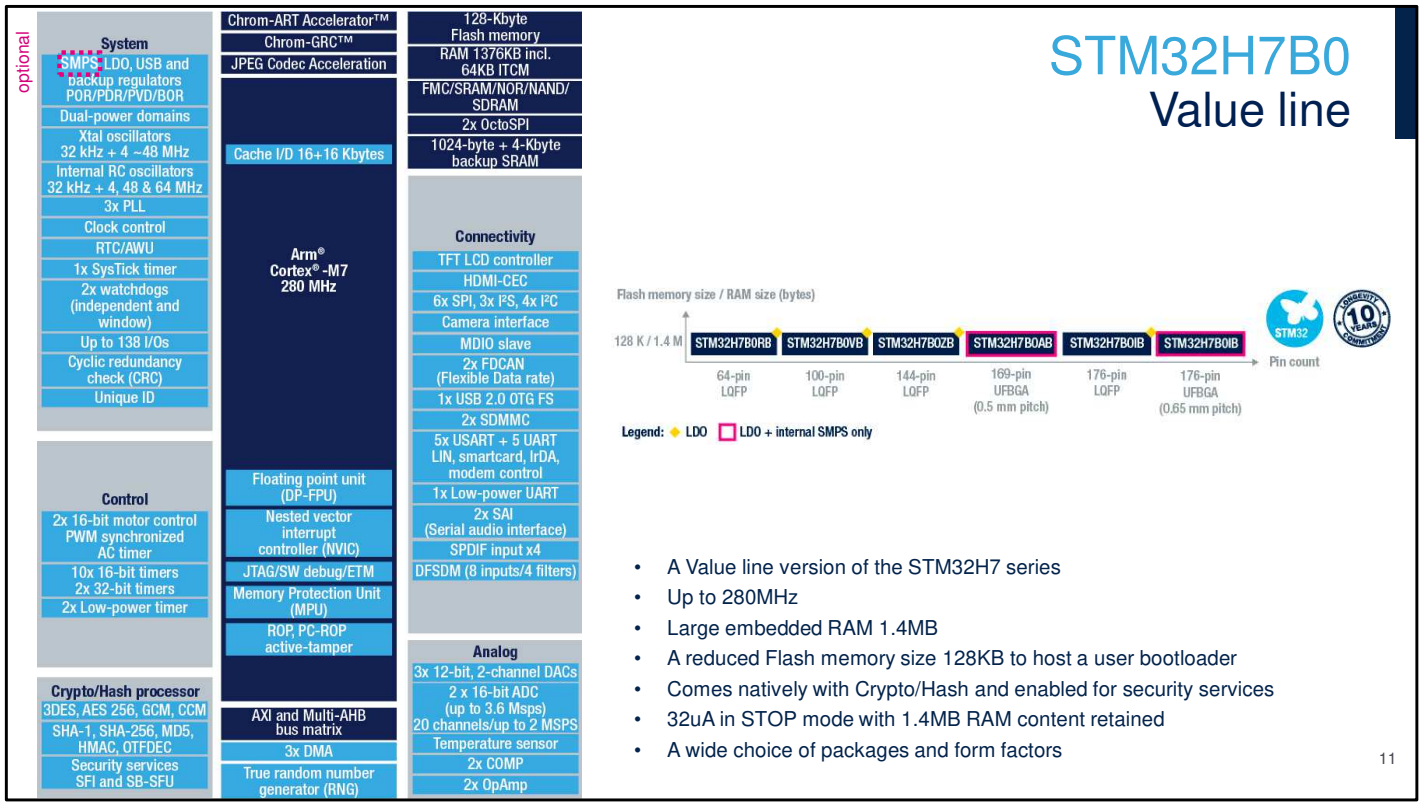
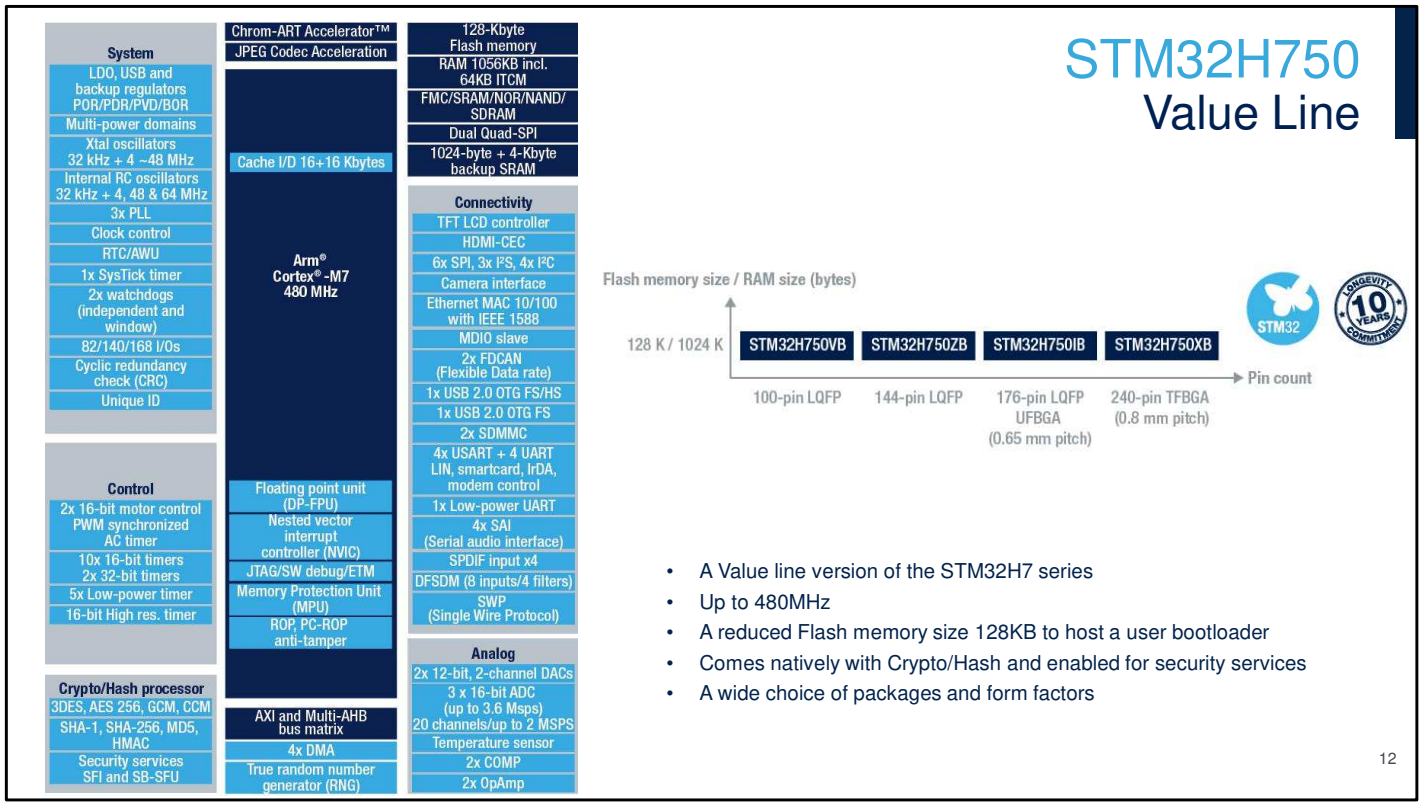
The STM32H747/757 graphic line expands the family, offering an additional Cortex-M4 core (with single-precision floating point unit), the MIPI-DSI interface and some additional power schemes with SMPS. The STM32F757 integrates the crypto/hash processor.



The Value Line STM32H730/H7B0/H750 offers an entry point to the STM32H7 series, cost effective, while the devices come with 128KB Flash memory to host for example a user Bootloader. This line is very suitable for applications where external memories are required. It comes natively in crypto variants only.
STM32H730 is the value line of the STM32H723/33/25/35 family.



STM32H7B0 is the value line of the STM32H7A3/B3 family.



STM32H750 is the value line of the STM32H742/43/45/55 family.

Pick the right STM32H7 development tool



STM32H7 class	Cores/Speed	Part numbers	Evaluation boards	Discovery Kits	Nucleo boards
STM32H74/5	Single Core 480 MHz	**STM32H743**	STM32H743I-EVAL2	-	NUCLEO-H743ZI2
		STM32H753, Crypto enabled	STM32H753I-EVAL2	-	NUCLEO-H753ZI
		STM32H750 Value Line, Crypto enabled	-	STM32H750B-DK	-
	Dual Core 480MHz + 240MHz	**STM32H745**	-	STM32H745I-DISCO	NUCLEO-H745ZI-Q
		STM32H747	STM32H747I-EVAL	STM32H747I-DISCO STM32H747I-DISC1	-
		STM32H755/757, Crypto enabled	STM32H757I-EVAL	-	NUCLEO-H755ZI-Q
STM32H7A/B	Single Core 280 MHz	**STM32H7A3**	-	-	NUCLEO-H7A3ZI-Q
		STM32H7B3, Crypto enabled	STM32H7B3I-EVAL	STM32H7B3I-DK	-
		STM32H7B0, Value line, Crypto enabled	*STM32H7B3I-EVAL **	*STM32H7B3I-DK **	-
STM32H72/3	Single Core 550MHz	**STM32H723/733**	-	-	NUCLEO-H723ZG
		STM32H725/735	-	STM32H735G-DK	-
		STM32H730, Value line, Crypto enabled	-	*STM32H735G-DK **	-

** Recommended board (no dedicated board for this part number)*

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The STM32H7 family benefits from the software and hardware tools available for STM32 microcontrollers. A wide range of development boards is proposed to map all features and variants

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