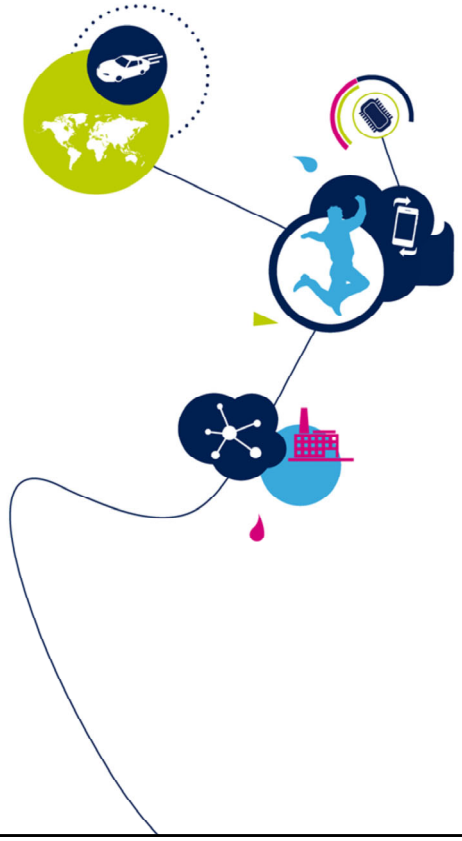
STM32WB - GPIO

General-purpose input/output interface

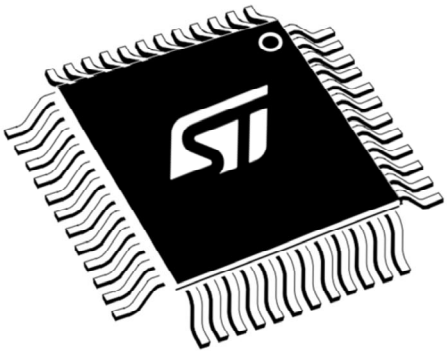
Revision 1.0



life.augmented

Hello, and welcome to this presentation of the STM32 general-purpose I/O interface. It covers the general-purpose input and output interface and how it allows connectivity to the environment around the STM32 microcontroller.

Overview



- Provides an interface for interaction with the external environment
  - Fully configurable
  - Interrupt and wake-up capability
  - Direct connection to AHB2 bridge

Application benefits

- Direct microcontroller wake-up
- Supports a wide range of supply voltages
- Direct connection to AHB2 allows fast toggle response

life.augmented

The general-purpose I/O pins of STM32 products provide an interface with the external environment. This configurable interface is used by the MCU and also all other embedded peripherals to interface with both digital and analog signals. Application benefits include a wide range of supported I/O supply voltages, as well as the ability to externally wake up the MCU from low-power modes.

Key features

3

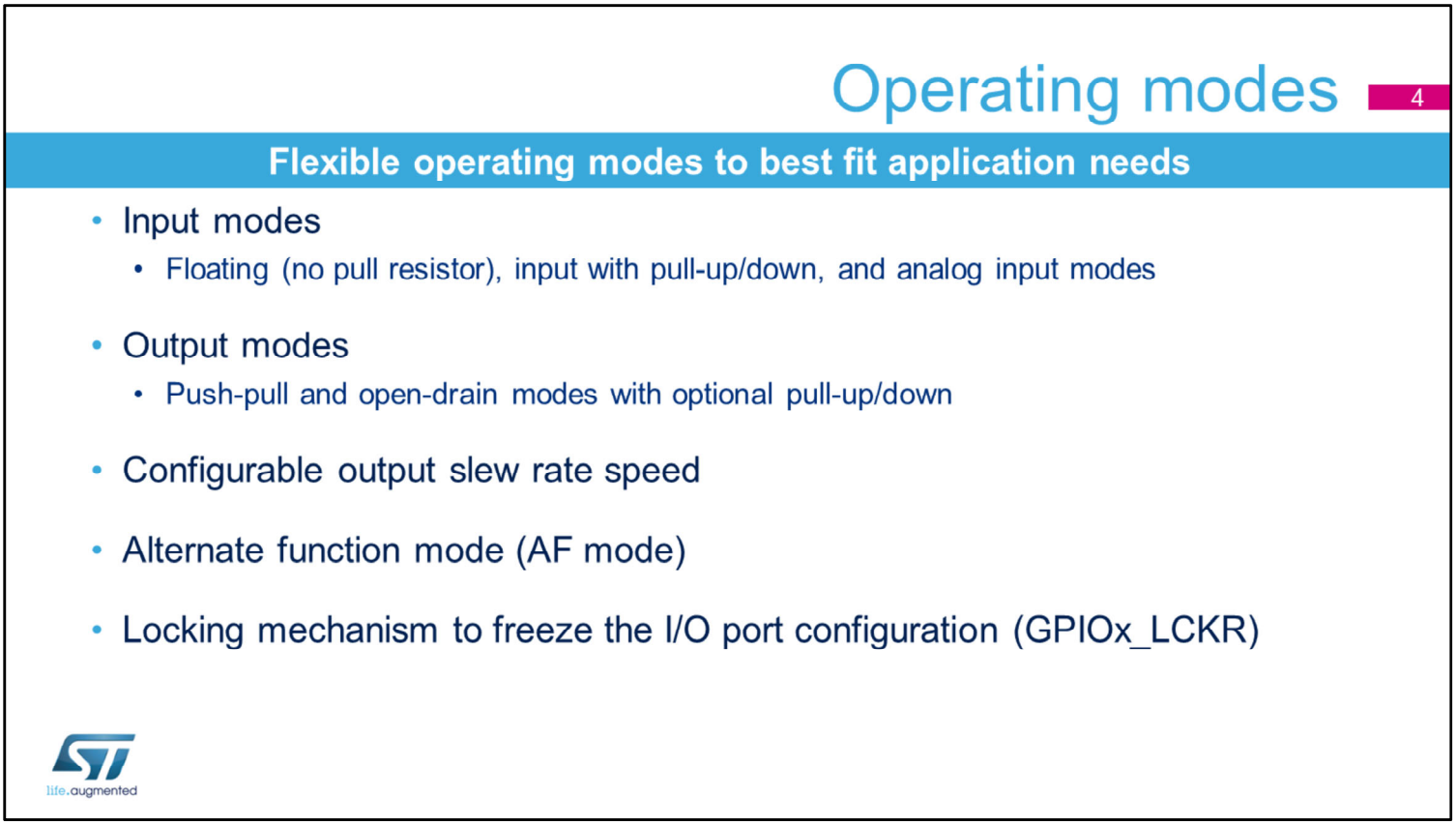
- Bi-directional operation of up to 72* I/O pins
  - Shared across 6 GPIOx ports named GPIOA to GPIOE and GPIOH, with up to 16 I/O pins per port
  - All with external interrupt and wake-up capabilities
  - Atomic bit set and bit reset operations using BSRR and BRR registers
  - Independent configuration for each I/O pin
  - I/O pin in Analog mode after reset
- GPIO register interface is directly connected to AHB2 bus
- Most I/O pins are 5 V tolerant when V_{DD} is above 1.62 V
- Independent I/O supply
  - Up to 3* I/O pins under V_{DDUSB} domain

life.augmented

** : depends on part numbers and packages*

The general-purpose I/O ports provide bidirectional operation according to the input memory map.
I/O ports are directly connected to the AHB2 bus. This allows fast I/O pin operations, e.g. toggling and output, with an independent configuration for each I/O pin. They are shared across 6 ports named GPIOA to GPIOE and GPIOH, each of them hosting up to 16 I/O pins. After reset, all GPIOs are set in Analog mode to reduce power consumption.
I/O ports support atomic bit set and bit reset operations through the BSSRR and BRR registers. This allows I/O toggling every 2 clock cycles.
Most of the I/O pins are 5 V tolerant when supplied from a VDD above 1.62 V.
Up to 3 I/O pins are supplied by externally providing a voltage within the VDDUSB supply domain. This supply is independent of the VDD provided to the MCU. This functionality allows users to adapt logic levels of the MCU's I/O pins to the levels required by external logic which may be

supplied by different voltage domains without the need for external level shifters.



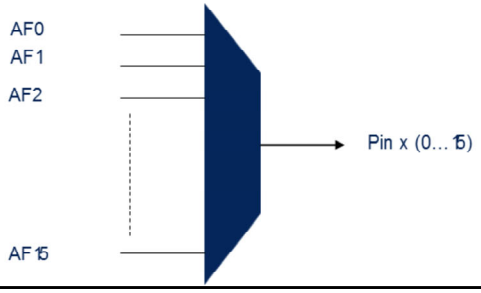
General-purpose I/O pins can be configured into several operating modes.
An I/O pin can be configured in an input mode with floating input, input mode with an internal pull-up or pull-down resistor or as an analog input.
An I/O pin can be also configured in an output mode with a push-pull output or an open-drain output with an internal pull-up or pull-down resistor.
For each I/O pin, the slew rate speed can be selected from 4 different ranges to compromise between maximum speed and emissions from the I/O switching and to adjust the application's EMI performance.
I/O pins are also used by other embedded peripherals to interface with the external environment. Alternate function registers are used to select the configuration for the peripherals in this case.
Configuration of the I/O ports can be locked to increase robustness of the application. Once the configuration is

locked by applying the correct write sequence to the lock register, the I/O pin’s configuration cannot be modified until the next reset.

Alternate functions

Structure of I/O pins is used as an interface by other embedded peripherals

- Several embedded peripherals share the same I/O pins
  - Including USARTx_TX, TIMx_CHx, SPIx_MISO, EVENTOUT, …
- Alternate function (AF) multiplexer selects the peripheral connected to the I/O pin
  - Only one alternate function is connected to a specific I/O pin at a single time
  - Configurable through the GPIOx_AFRL and GPIOx_AFRH registers



life.augmented

Several integrated peripherals such as the USART, timers, SPI and others share the same I/O pins in order to interface with the external environment.
Peripherals are configured through an alternate function multiplexer which ensures that only one peripheral is connected to an I/O pin at a single time. Of course, this selection can be changed while the application is running through the GPIOx_AFRL and AFRH registers.

Independent V_{DDUSB} supply

Independent V_{DDUSB} brings benefits in a multi-supply environment

- V_{DDUSB} supply domain is independent of V_{DD}
- Pins in the V_{DDUSB} domain can be used to communicate with other circuits, i.e. USB, which are supplied by voltage rails other than V_{DD}
- Up to 3 I/O pins

Application benefits

- Well suited for applications with two different power supplies / supply voltage without the need for external of level shifters

life.augmented

The Independent VDDUSB supply domain allows operation in an environment with several different logic supply voltages. It allows the STM32 to communicate with different logic supplies.
Up to 3 I/O pins in this domain can be used to communicate with other logic circuits, for instance USB, which are supplied by voltage rails other than VDD.
The use of independent voltage supplies may eliminate the need for external voltage shifters in the design.

Special considerations for I/O pins

Only debug pins remain in AF mode under reset

- During and after reset, the alternate functions are not active
  - I/O ports default state to input mode
  - To reduce current consumption, IOs may be configured in Analog mode
- Only JTAG/SWD debug pins remain active in AF pull-up/pull-down configuration
  - PA13: JTMS/SWDIO
  - PA14: JTCK/SWCLK
  - PA15: JTDI
  - PB3: JTDO
  - PB4: NJTRST

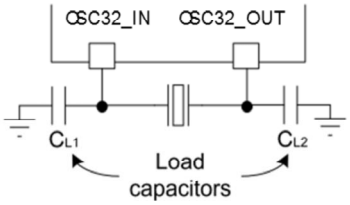
life.augmented

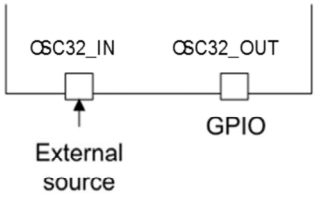
During and after reset, the alternate functions are not active.
Only debug pins remain active in AF mode.
JTAG/SWD debug pins remaining in AF configuration mode are listed in this slide.

Special considerations for LSE pins

Oscillator pins can be used as standard I/O pins

- When the oscillator is switched OFF, related pins behave as I/O pins
  - Valid for LSE
  - This state is the default one after reset
- When user external clock mode is used, the second pin behaves as an I/O pin
  - Only OSC32_IN is used as clock source
  - OSC32_OUT are standard I/O pins





life.augmented

When the external oscillator is switched off, pins related to this oscillator can be used as standard I/O pins. This is the default state after a device reset.
When the external clock source is used instead of a crystal oscillator, only the OSC32_IN pin is used for the clock and the OSC32_OUT pin can be used as a standard I/O pin. The STM32WB high-speed oscillator pins are dedicated to the OSC_IN and OSC_OUT functions and have no standard I/O function.

Multi-supply I/O pins

Some I/O pins can be supplied from different sources

- New I/O pin supply scheme brings new I/O pin structures and names
  - TT and FT definition is extended by new abbreviation suffix
  - Maximum V_{IN} is defined by lowest supply voltage connected to the structure of given I/O pin
  - For example, formula $V_{IN} < \min (V_{DD}, V_{DDA}) + 4.0$ V applies for FT_a pin

Abbreviation suffix	Description	Example
_f	I/O with Fm+ capability, supplied by V_{DD}	FT_f, FT_fa
_l	I/O with LCD function, supplied by V_{LCD}	FT_l
_a	I/O with analog function, supplied by V_{DDA}	FT_a, TT_a
_u	I/O with USB function, supplied by V_{DDUSB}	FT_u

life.augmented

A new multi-supply scheme of I/O pins brings new I/O pin structures. Previously-used naming – FT, TT – has been extended by abbreviation suffixes to highlight alternate supply sources for each FT and TT I/O pin.
Previously-used name FTf for Fm+ capable pins has been transformed to FT_f, the new _l suffix has been added to mark pins supplied through LCD supply, suffix _a marks pins supplied by analog supply, suffix _u is used for pins supplied from USB supply.
The absolute maximum rating for each I/O pin is defined by the lowest voltage of the supplies listed for each I/O pin.

Low-power modes

Mode	I/O Description
Run	Active.
Sleep	Active.
Low-power run	Active.
Low-power sleep	Active.
Stop 1	Active.
Stop 2	Active.
Standby	Only as input with internal pull-up, pull-down or floating.
Shutdown	Only as input with internal pull-up, pull-down or floating. Configuration lost when exiting.
Reset	Forced to Analog input mode when the MCU is under reset.

life.augmented

I/O pins remain active in all modes except Standby and Shutdown, where the only available configuration is input with internal pull-up, pull-down resistor or floating input. When exiting Shutdown mode, the I/O configuration is lost. When the MCU is under reset, I/O pins are forced into an analog input mode.

Thank you.