Welcome to the presentation of the STM32G4 UCPD (USB Type C / Power Delivery) interface. It covers the main features of this module.
The UCPD unit embeds a PD physical layer (PHY) with a direct connection to the Configuration Channel pins (CC1 and CC2).

The UCPD can be configured as a Downstream Facing Port (DFP) or an Upstream Facing Port (UFP) and also supports the Fast Role Swap protocol that enables swapping DFP and UFP states.

In order to implement the protocol layers based on message exchange over CC1 or CC2, the UCPD offers a programming interface, enabling software to receive or send message payload bytes. Requests to external DMA channels may also be used to automatically transfer protocol messages to/from memory.

The block diagram shows the two important parts of the UCPD module:
- The register interface on the left clocked by PCLK, that is used by software to configure and determine
the current state of the module. Messages are transferred byte per byte by means of the Tx and Rx registers

- The PD physical layer that encodes/decodes bytes, appends and checks the CRC and also manages the transmission of ordered sets.

The application benefits are:

- Integrated on-chip PD PHY, including Rp and Rd resistors
- Dead Battery mode supported allowing connection detection at the peer device in a dead battery situation
- PD message transmission and reception, software is only in charge of handling the payloads.
The UCPD controller is compliant with
• USB Type-C Rev. 1.2 and
• USB Power Delivery Rev. 3.0 specifications. Regarding the PHY, only the CC signaling method is supported, so the Type-C cable is required.
The Reset and Clock Controller (RCC) unit is in charge of resetting the UCPD unit by asserting the nPReset signal. It also provides the following reference clocks to the UCPD unit:

- **PClk**, which is the APB clock, used to access memory-mapped registers
- **UsbPdClk**, which is the main functional clock. UsbPdClk can be prescaled in order to obtain the half-bit clock required by the Bi Mark Phase coding.

Note that for the timings called tTransitionWindow and tInterFrameGap, the clock frequency uncertainty should be taken into account in order to respect the timings in all cases.

The UCPD module asserts ClkReq to the RCC in order to exit a clock-gating low-power state.

- A single reset signal nPReset (APB bus reset) is used
- The register section of UCPD is directly clocked on PClk
- The main functional part is clocked on UsbpdClk
  - This clock can be pre-scaled
  - The receiver is designed to work for any clock input from 9 to 18 MHz
This slide describes the pinout of the UCPD unit. Pins UCPD_CC1 and UCPD_CC2 are the only signals to be routed to the USB Type-C receptacle. Note that the cable contains a unique CC signal, connected to either CC1 or CC2 in the receptacle because the cable can be flipped.

The UCPD_FRSTX pin is relevant when the Dual Role Port protocol is supported. It is used to control an external NMOS transistor that pulls down the CC1 or CC2 line respectively, which is the way to request a role swap.

Pins UCPD_DBCC1 and UCPD_DBCC2 are used when the STM32G4 USB Type-C port indicates to the peer port a dead battery condition, by connecting UCPD_DBCC1 to UCPD_CC1 and UCPD_DBCC2 to UCPD_CC2.
The STM32G4 implements internal Rp and Rd resistors connected to CC1 and CC2 pins required by the USB PD specification to:
- Detect a connection.
- Determine whether the cable is flipped.
- Determine the default available power as the current-carrying capability depends on the values of Rp.

Finally, a unique CC pin, CC1 or CC2 according to cable flip, is used to transport PD messages. The unused CC pin may become the VCONN pin, which supplies the power to integrated circuits present in active cables.

In order to conserve power, the unused CC pin can also be disabled by programming the CCENABLE control field in the UCPD_CR register.
The UCPD is configured by software as either a Downstream Facing Port (DFP) or an Upstream Facing Port (UFP).

In DFP mode, assuming no cable flip, CC1 is connected to Rp. The value of Rp indicates the value of the default power that the DFP can source on Vbus.

In DFP mode, assuming no cable flip, CC2 is connected to Vconn. VCONN is a 5 Volt 1.0 Watt power supply used to power devices within the plug that are needed to implement electronically marked cables and VCONN-powered accessories.

In UFP mode, assuming no cable flip, CC1 and CC2 are connected to Rd, which is a 5.1 Kilo ohm resistor.

Since the UCPD supports both DFP and UFP operation, the internal switches represented in the figure select the current configuration.
When the UCPD is used as an upstream facing port, the dead battery feature enables the UCPD to indicate to the peer node that it needs to be powered. This analog setting is functional even when the MCU power supply is switched off. This default behavior is configured by connecting the DBCC pins to the respective CC pins.

After power arrives and the STM32G4 boots, the desired behavior (e.g. sink) should be programmed in the ANAMODE and ANASUBMODE fields of the UCPD_CR register before writing SYS_CONFIG[USBPDstrobe] to activate this behavior.

Connecting DBCC pins to ground disables Dead Battery mode. In this case, the peer DFP is unable to distinguish a dead battery state from an unattached state.
The Fast Role Swap protocol swaps the roles of DFP and UFP. The default power source node becomes the sink node and the default sink node becomes the source node. To request a FRS to the source node, the sink device temporarily connects the appropriate CC line to ground. This is achieved by external N-MOS transistors on both CC lines, however only one receives the FRSTX pulse. The N-MOS on the inactive CC line should be driven with a logic 0 level using GPIO mode. The FRSRXEN bit in the UCPD_CR register controls the FRS detection in the sink node. When this bit is set, the FRS detection is enabled.
The digital controller is in charge of:
- USB Type-C™ level detection with de-bounce, generating interrupts
- Fast Role Swap (FRS) detection
- CRC generation/checking
- 4b5b encode/decode
- Bi-Phase Mark (BMC) encode/decode
- Transmission and reception of ordered sets.

A clock data recovery unit in the receiver recovers the transmission clock from the received bitstream.

The digital controller offers a byte-level interface for USB Power Delivery payload, generating interrupts. A DMA channel can assist the transfer of message payloads, because the UCPD unit is able to request DMA transfers.

The UCPD module implements two clock domains: APB register interface clocked by PCLK and PHY clocked by UsbPdClk.

UsbPdClk is divided by a programmable prescaler to
provide the CC clock, whose maximum frequency is 300 Kbps (kilobits per second). Due to the bi-phased mark coding, two transitions may occur per transmitted bit, therefore the actual maximum clock frequency is 600 kHz.
The PHY monitors the state of CC1 and CC2, either continuously or by polling, to detect and signal events to the software by setting flags in the UCPD_SR register. In order to optimize power consumption, it is recommended to use polling, because Type-C detectors are OFF between polls, rather than wakeup from STOP, which requires Type-C detectors permanently ON. The static level on the CC pins is determined via threshold detectors in the PHY to give a voltage range value in registers, facilitating the Type-C state machine implementation in software, and also allowing the cable orientation to be determined. The Type C de-bounce subunit filters events to be reported to software. It is also in charge of ensuring the coordination between event signaling and power delivery Tx/Rx activity.
The PD software stack is executed by the Cortex-M4 core in the STM32G4. It is based on messages and events. Events are reported to the Cortex-M4 core through interrupts. Regarding messages, only the payload is under software control. The digital controller performs message encapsulation with Preamble, Start of Packet, CRC and End of Packet. The software stack includes the protocol layer, the policy engine, the device policy manager and the system policy manager. The system policy manager may control several PD ports, in order to implement platform level power management.
Three software layers are defined in the PD specification:

1. **Device Policy Manager (DPM)** is in charge of device level system management and monitoring. It determines the power plan and contracts depending on current power state.

2. **Policy Engine (PE)** controls a single UCPD port. Message sequences are defined to request power resources, performing source or sink transitions. This layer implements power negotiation, swapping and handles message flow errors and reset.

3. **Protocol Layer (PL)** is in charge of constructing and deconstructing PD messages. This layer automatically returns GoodCRC when a message is correctly received and also handles transmission errors, such as timeout and retries.

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<th>Protocol layer</th>
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| **DPM** Device Policy Manager | **DPM is responsible of the overall system management and monitoring**
- Interacts with the policy engine, power supply, cable detect, and system policy manager
- Determines the power plan and actions (contracts) required depending on current power state |
| **PE** Policy Engine | **One instance per port, that determines the Local Policy to be enforced**
- Message sequences are specified for various operations:
  - Request power resources for the port
  - Power source or sink transitions
  - This layer implements power negotiation and swapping
- Handles message flow errors and resets |
| **PL** Protocol Layer | **On transmit, this layer builds the message and passes it to the Digital Controller. On receive, this layer gets the message from the Digital Controller, passes and deconstructs it**
- CRC generation/checking is performed by this layer, which automatically returns GoodCRC for correctly received messages
- Communication errors are also handled by this layer |
Two parts are fully managed by STMicroelectronics (USBPD core stack and USBPD devices), so the user only needs to focus development effort on two other parts:

- **User application part:** called the 'Device Policy Manager' inside the USB organization specification. ST delivers an application template to be completed according the application need.
- **Hardware part:** the effort is mainly focussed on energy management, which depends on the resource materials chosen by the user to manage Type-C power aspects. STMicroelectronics has released the STM32CubeMonitor-UCPD (STM32CubeMonUCPD), which is a software tool to configure and monitor the USB Type-C™ Power Delivery (UCPD) ports on equipped STM32 boards.

The configuring part allows the modification of the USB
Type-C Power Delivery port default configuration. Checks of Power Delivery contract establishment and activity are possible with the monitoring tool.
In addition to transporting data digits, converted into 5-bit codes, the PD protocol also transports signaling patterns called ordered sets. They are composed of four 5-bit K codes and are tolerant to transmission errors through a redundancy mechanism. Ordered sets, such as Start of Packet (SOP) are necessarily present in packets. The digital controller automatically inserts them in the transmitter and strips them in the receiver after having checked their validity. The ordered sets defined in the PD specification are used to:

- Signal a cable or hard reset condition
- Delimit the beginning of packets.
The PHY automatically inserts the preamble, the Start of Packet (SOP), the CRC and the End of Packet (EOP). The receiver PHY handles these fields and removes them.

The header field and possibly the payload fields are entirely handled by software.

The PHY does not interpret their contents.

The Preamble is not encoded.

It is used by the receiver PHY to recover clock data.

All the subsequent fields are encoded in the transmitter and decoded in the receiver.
The Type-C connector does not support a dedicated reset signal. Consequently, reset conditions are signaled by using specific PD packets transferred over the CC line. These packets, called ordered sets, are completely handled by the physical layer.

Two types of reset are defined: hard reset, which aborts the on-going transfers and the cable reset, which does not require a high-priority treatment.

The sequence required to issue the reset packet is described in this slide.
The PD specification describes Built-In Self test (BIST) packets, used to test whether the CC line is functional. BISTs are sent on a software decision, based on fields in the UCPD_CR register. Software can enforce the transmission of a BIST packet and can also configure the receiver in test mode: received BIST packets are not submitted to software, however their CRC is checked. Two formats of BIST packets are defined in the PD specification:

- BIST test data, which is a packet containing a payload, used to test the digital controller
- BIST carrier mode, which is a single pattern, infinite length message is used to test the physical link by capturing the CC in an oscilloscope for example.
The Type-C™ state machine is implemented in software. The Type-C™ state machine depends not only on CC pin levels, but also on the port role:

- In sink mode, it depends on the VBUS presence detection,
- In source mode, it depends on the VCONN generation and the VBUS state: ON, OFF, voltage level and discharge.

The UCPD module only controls the CC lines. Other modules are involved to control the VBUS and VCONN power supplies.

In Source mode, GPIOs are required to control the power delivery dynamically.
In Sink mode, ADC channels are used to monitor VBUS and VCONN supplies.
The UCPD can be programmed to remain active in Stop 0 and Stop 1 modes. The detection of a PD event while the MCU is in Stop mode causes a wakeup condition, signaled to the EXTI unit and then to the PWR unit. The following events can be configured to cause a wakeup request: 
- Events on the BMC receiver, such as message receipt 
- Fast Role Swap request 
- Events on the Type-C detector, such as attachment/detachment.
The UCPD is able to wakeup the MCU from Stop mode (if enabled by setting the WUPEN bit in the UCPD_CFG2 register) when it recognizes one of the relevant events listed below:

- Type-C event relating to a change in the voltage range seen on either of the CC pins, visible in TYPEC_VSTATE_CCx
- Power delivery receive message with an ordered set matching those filtered according to RXORDSETEN[8:0], visible by reading RXORDSET.

At UCPD level, three types of events requiring kernel clock activity may occur during Stop mode: Type-C™, BMC Rx, and FRS detection.

In order to function correctly with the RCC, the clock request signal is activated (conditional on WUPEN) when the following events are detected:

- Activity on the analog PHY voltage threshold
detectors which could later be confirmed to be a stable change between voltage ranges defined in the Type-C specification

- Activity on Power Delivery BMC receiver (coming from the selected CC pin) which could potentially generate an Rx message event (RXORDSET) later
- Activity on Power Delivery FRS detector which could potentially generate an FRS signaling detection event (FRSEVT) later
- Type-C voltage threshold detectors (coming from either CC pin)
- The Power Delivery receiver signal (coming from the selected CC pin)
- The FRS detection signal (coming from the selected CC pin)
When an interrupt from the UCPD is received, then the software has to determine the source of the interrupt by reading the UCPD_SR register. Depending on which bit is set to “1”, the interrupt service routine should handle that condition and clear the bit by writing to the appropriate bit in the UCPD_ICR register. This slide summarizes all the events detected by the UCPD module that can cause interrupt requests.
Please refer to the training linked to this peripheral for more information:

- STM32G4 DMA controller (DMA)
- Reset and Clock Controller (RCC)
- Extended Interrupt and Event Controller (EXTI)
- System Configuration Controller (SYSCFG)
- Power Controller (PWR).