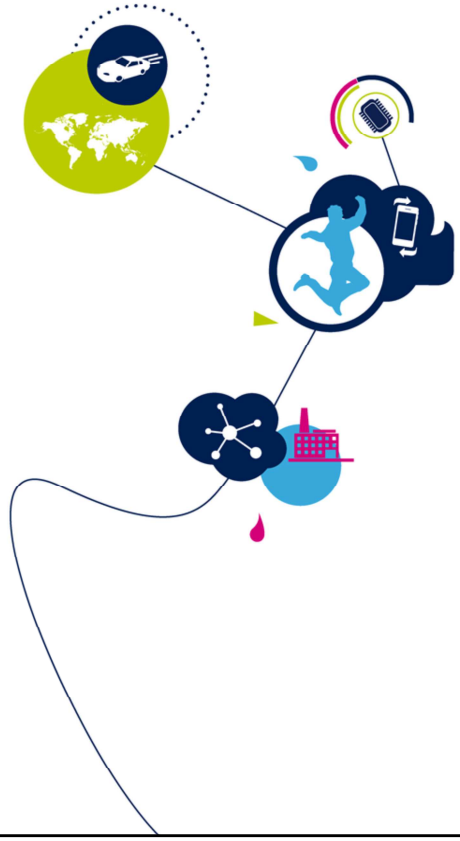
STM32MP1 - GIC

Global Interrupt Controller
Revision 2.0



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Hello, and welcome to this presentation of the STM32 Global interrupt controller (GIC).

Overview

WWDG1_EWIT	Window Watchdog 1 Early Wakeup interrupt
PVD	PVD & AVD detector through AIEC
TAMP	Tamper interrupt (include LSECSS interrupts)
RTC_WKUP_ALARM	RTC Wakeup Timer and Alarms (A and B) interrupt
TZC_IT	TrustZone DDR Address Space Controller
RCC	RCC global interrupt (rcc_mpu_irq)
EXTI0	EXTI Line 0 interrupt through AIEC
EXTI1	EXTI Line 1 interrupt through AIEC
EXTI2	EXTI Line 2 interrupt through AIEC
EXTI3	EXTI Line 3 interrupt through AIEC
EXTI4	EXTI Line 4 interrupt through AIEC
GPDMA1_STREAM0	DMA1 Stream0 global interrupt
...	...

- ARM® Cortex® -A7 MultiCore support
- ARM® TrustZone® and Virtualization support
- Up to 288 interrupts

Application benefits

- Supports prioritization levels with dynamic control
- Full security support with ARM® TrustZone®
- Distribution of the interrupts to the target core

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The Global Interrupt Controller embedded inside the STM32MP1 microprocessor provides up to 288 interrupt channels with support of TrustZone and Virtualization. Application can benefit from dynamic prioritization of the interrupt levels, ARM TrustZone security extension and, for multi-core product, the interrupt distribution to each core .

Key features

- Tightly coupled with ARM® Cortex® -A7 processor
- Dynamic reprioritization of interrupts
- Support of Multicore*, distribution of the interrupts to the target core
- Generation of interrupts by software
- Support for Security Extensions
- Support for Virtualization Extensions

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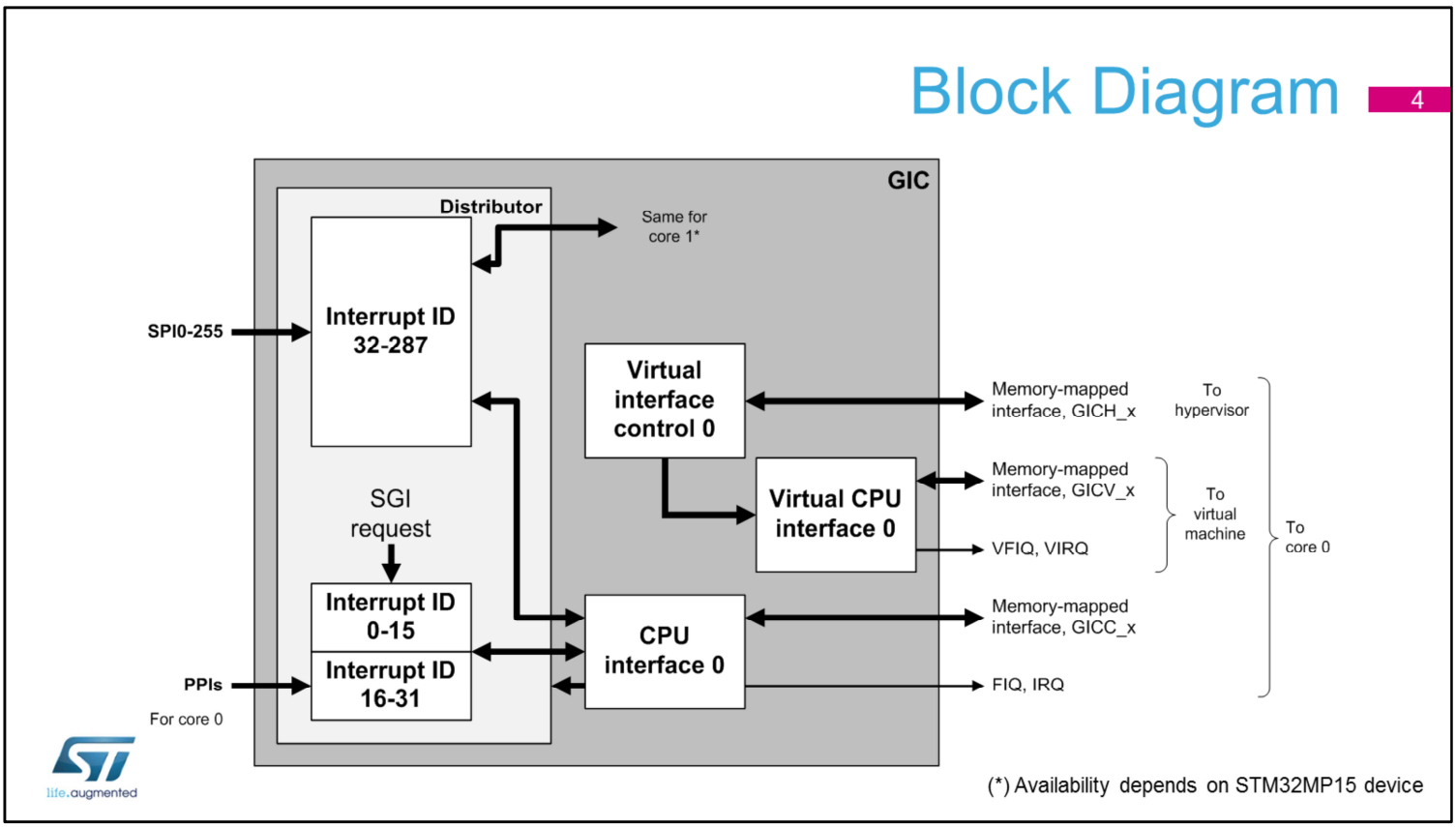
(*) Availability depends on STM32MP15 device

The Global Interrupt Controller is tightly coupled with the ARM Cortex-A7 processor and provides a dynamic reprioritization of interrupt requests, allowing an application to better serve the incoming events. Most of the peripherals have a unique interrupt line, making the development of the application easier (no need to determine the source of an interrupt during the interrupt handling). In case of multicore Cortex-A7 processor, each interrupt can be distributed to a single or both cores. GIC also fully supports ARM TrustZone security and virtualization extensions.



The GIC receives up to 256 interrupts from STM32MP15 peripherals shared between the two Cortex-A7 cores. In addition, up to 16 internal private peripheral interrupts (PPI) and up to 16 software generated interrupts (SGI) are managed by each Cortex-A7 core.
The GIC signals interrupt to each core with FIQ and IRQ. In a usual software implementation, FIQ is dedicated to secure interrupts.
The GIC also provides virtual control and interface for each Cortex-A7 core, helping hypervisor and virtual machine implementation.

Type of Interrupts

- Software Generated Interrupts (SGI)
  - Generated by writing to the Software Generated Interrupt Register
  - A maximum of 16 SGIs, ID0-ID15, can be generated for each core interface
  - ARM recommend to use SGI ID0-ID7 for non-secure interrupts and SGI ID8-ID15 for secure interrupts
- Private Peripheral Interrupts (PPI)
  - A PPI is an interrupt generated by a peripheral that is specific to a single core
    - Secure Physical Timer event (PPI1)
    - Non-secure Physical Timer event (PPI2)
    - Virtual Timer event (PPI4)
    - Hypervisor Timer event (PPI5)
    - Virtual Maintenance Interrupt (PPI6)

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Here is the list of the different type of interrupt sources managed by the Global Interrupt Controller.

- Software generated interrupt can be used to send an interrupt to the other core
- Private peripheral interrupts are mostly from timers. Note that there is one set of private interrupts for each core which is completely independent from the other core.

Type of Interrupts

- Shared Peripheral Interrupts (SPI)
  - SPIs are triggered by events generated on associated interrupt input lines
  - The GIC can support up to 256 SPIs corresponding to the peripherals IRQs signals
  - The SPIs can be configured to be rising-edge-triggered or active-high-level sensitive
- Interrupt IDs
  - Interrupts from sources are identified using ID numbers
  - ID32-ID287 are used for SPIs
  - ID0-ID31 are used for interrupts that are private to a CPU interface. A banked interrupt is identified uniquely by its ID number and its associated CPU interface number
    - ID0-ID15 are used for SGIs
    - ID16-ID31 are used for PPIs

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The shared peripheral interrupts are the usual STM32MP15 interrupts coming from peripherals (e.g. UART).
These interrupts are shared between the multiple Cortex-A7 cores and can generate interrupt to one or both cores.
Note that an interrupt does not have programmable polarity and can be either rising-edge or high-level sensitive.
Within FIQ or IRQ interrupt routine, interrupts pending is identified inside the GIC by an ID number from 0 to 287.

Description

- Interrupt priority
  - The GIC in STM32MP15x microprocessor implements a 5-bit version of the interrupt priority field for 32 interrupt priority levels
    - ARM strongly recommends that Group1 interrupts (non-secure) have assigned priority values in the upper half priority value range (highest number is lower priority)
- GIC Distributor
  - Centralizes all interrupt sources,
  - For each core, forwards the interrupt with the highest priority to the CPU interface for priority masking and preemption handling

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There is up to 32 interrupt priority levels. GIC includes a mechanism to avoid non-secure interrupt to get higher priority than secure interrupt.
Using half of the priority range for non-secure interrupts allows the secure interrupts to use the full range of priority and choosing which secure interrupt could be protected from non-secure interruption.
In that case, non-secure software can only see the lower 16 possible interrupt priority levels.
Finally, the GIC distributor selects which priority is presented to each core.

Description

- CPU interfaces
  - Each CPU interface block provides the interface for a processor that is connected to the GIC. Each CPU interface provides a programming interface for:
    - enabling the signaling of interrupt requests to the processor
    - acknowledging an interrupt
    - indicating completion of the processing of an interrupt
    - setting an interrupt priority mask for the processor
    - defining the preemption policy for the processor
    - determining the highest priority pending interrupt for the processor

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There is a separated CPU interface for each Cortex-A7 core which presents either shared or banked register and either secure or non-secure register view.

ARM® TrustZone® support

Security

- Security Extensions support
  - Group0 interrupts are Secure interrupts, and Group1 interrupts are Non-secure interrupts
    - Each interrupt can be assigned either to Group0 or Group1
  - The rights for each core to access GIC registers depends on whether the access is Secure or Non-secure
  - Secure software can manage interrupt sources securely without the possibility of interference from Non-secure software

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The Global Interrupt Controller fully supports TrustZone security and allows a flexible implementation of secure and non-secure interrupts.

Virtualization

- Virtualization support in GIC
  - The processor Virtualization Extensions provide hardware support for virtualizing the Non-secure state
    - The extensions support system use of a virtual machine monitor, known as the hypervisor, to switch in between guest operating systems
  - Whether implemented in a single processor or in a multiprocessor system, the processor Virtualization Extensions supports running multiple virtual machines on a single processor.
  - The hypervisor can either handle a physical interrupt itself, or generate a corresponding virtual interrupt that is signaled to a virtual machine. It is also possible for the hypervisor to generate virtual interrupts that do not correspond to physical interrupts

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Virtualization is a system supporting more than one operating system at a time (or multiple independent instances of the same operating system).
The GIC helps support of such virtualization, by example, by providing virtual interrupts to a virtual machine.

References

- For more details, please refer to following documents:
  - ARM® Generic Interrupt Controller Architecture Specification (ARM IHI 0048)
  - STM32MP15 reference manual
- Visit the MP1 Wiki pages for additional information

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For detailed information, please refer mainly to the ARM Generic Interrupt Controller Architecture Specification (ARM IHI 0048).
Please visit also the MP1 Wiki pages for details.