Hello, and welcome to this presentation of the STM32 general-purpose IO interface. It covers the general-purpose input and output interface and how it allows connectivity to the environment around the STM32F7 microcontroller.
The general-purpose IO pins of STM32 products provide an interface with the external environment. This configurable interface is used by the MCU as well as the other embedded peripherals to interface with both digital and analog signals. Application benefits include a wide range of supported IO supply voltages, as well as the ability to externally wake up the MCU from low-power modes.
The general-purpose I/O ports provide bidirectional operation according to the input memory map. I/O ports are directly connected to the AHB bus. This allows fast I/O pin operations, e.g. toggling and output, with an independent configuration for each I/O pin. They are shared across 11 ports named GPIOA to GPIOK, each of them hosting up to 16 I/O pins. I/O ports support atomic bit set and reset operations through the BSSRR and BRR registers. It allows I/O toggling every 2 clock cycles. Most of the I/O pins are 5 V tolerant when supplied from VDD above 1.8 V.

Up to 10 I/O pins are supplied by independent voltage supplies (VDDUSB and VDDSDMMC). These supplies are independent of the VDD provided to the MCU. This functionality allows users to adapt logic levels of the MCU's I/O pins to the levels required by external logic.
which may be supplied by different voltage domains without the need for external level shifters.
General-purpose I/O pins can be configured for use in several operating modes. An I/O pin can be configured in an input mode with floating input, input mode with an internal pull-up or pull-down resistor or as an analog input. An I/O pin could be also configured in an output mode with a push-pull output or an open-drain output with an internal pull-up or pull-down resistor. For each I/O pin, the slew rate speed can be selected from 4 ranges to compromise between maximum speed and emissions from the I/O switching and adjust the application’s EMI performance. I/O pins are also used by other embedded peripherals to interface with the external environment. Alternate function registers are used to select the configuration for the peripherals in this case. The configuration of the I/O ports can be locked to
increase robustness of the application. Once the configuration is locked by applying the correct write sequence to the lock register, the I/O pin’s configuration cannot be modified until the next reset.
Several integrated peripherals such as the USART, timers, SPI and others share the same I/O pins in order to interface with the external environment. Peripherals are configured through an alternate function multiplexer which ensures that only one peripheral is connected to an I/O pin at a single time. Of course, this selection can be changed during run time of the application through the GPIOx_AFRL and AFRH registers.
During and after reset, the alternate functions are not active. Only debug pins remain in AF mode. JTAG/SWD debug pins remaining in AF configuration mode are listed in this slide.
When the external oscillator is switched off, pins related to this oscillator can be used as standard I/O pins. This is the default state after device reset.
When the external clock source is used instead of a crystal oscillator, only related OSC_IN pin is used for the clock and OSC_OUT pin can be used as standard I/O pin.