Hello, and welcome to this presentation of the STM32 Serial Peripheral Interface.
The internal Serial Peripheral Interface or SPI provides a simple communication interface allowing the microcontroller to communicate with external devices. This interface is highly configurable to support many standard protocols. Applications benefit from the simple and direct connection to components which only requires a few pins. Thanks to the highly configurable capabilities of the SPI, many devices can be simply accommodated in the existing project.
The STM32 SPI offers various operating modes that are explained in more detail in this presentation. The communication speed can’t exceed half of the internal bus frequency, and a minimum of two wires is required to provide the serial data flow synchronized by clock signal in a single direction. An optional hardware slave select control signal can be added. The data size and transmit shift order are configurable, as well as the clock signal polarity and phase or polarity and timing adjustment of the slave select signal.

At the protocol level, the user can use specific data buffers with an optional automatic cyclic redundancy check or CRC calculation, and transfers through the DMA controller. There are a wide range of SPI events that can generate interrupt requests.
The simplified SPI block diagram shows its basic operation and functions. There are four I/O signals associated with the SPI peripheral. All data passes through the receive and transmit buffers via their specific interfaces. Data is temporarily stored in two 32-bit embedded Rx and Tx FIFOs with DMA capability. The Slave Select signal is managed by hardware or software for both master and slave, enabling dynamic change of master/slave operations. The SPI controller supports a hardware cyclic redundancy check (CRC) feature for reliable communication: the CRC value can be transmitted as last bytes in transmit mode and an automatic CRC error check is done on the last received bytes.
The SPI master always controls the bus traffic and provides the clock signal to the dedicated slave through the SCK line. The master can select the slave it wants to communicate with through the optional Slave Select or SS signal. Data stored in the dedicated shift registers can be exchanged synchronously between the master and slave through the MOSI (Master Output, Slave Input) and the MISO (Master Input, Slave Output) data lines. In Full-duplex mode, both data lines are used and synchronous data flows in both directions.
In Simplex mode, one node transmits data while the other receives the data. Data only flows in one direction. Depending on the communication direction, only one data line is used. Unused SPI pins can be used for other purposes.
Half-duplex mode integrates the previous two modes by sharing a single line for data exchanges and data flows in a single direction at a time. There is a cross connection between the master MOSI and the slave MISO pins in this mode. The master and slave have to alternate their transmitter and receiver roles synchronously when having a common data line. It is common to add a serial resistor on the half duplex data line between MISO and MOSI pins to prevent possible temporary short-circuit connection, since master and slave nodes are not usually synchronized.
When the SPI network includes more than one slave, a star topology is commonly used. The master communicates with one slave at a time, selected by its Slave Select input. In this topology, a separate Slave Select signal from the master has to be provided to each slave node, so the master can select which slave to communicate with via dedicated GPIO pin. Thanks to separate Slave Select signals, SPI data and clock format can be adapted for each slave, if the multiple slave nodes do not have a common configuration.
Another multi-slave configuration is the circular topology where the inputs and outputs of all the nodes are connected together in a closed serial chain. A common Slave Select signal is used for all the nodes as communication occurs at the same time. All nodes must have the same data and clock format configuration. Usually, the internal transmit and receive shift registers of a node are physically separated, so the internal data transfers have to be handled by software in this circular mode. The master node has to pace the internal data transfer accurately enough to remain synchronized with the other external data transfers.
SPI networks can operate in a multi-master environment. This mode is used to connect two master nodes exclusively. When neither node is active, they are by default in a slave mode. When one node wants to take control of the bus, it switches itself into Master mode and asserts the Slave Select signal on the other node through a GPIO pin. Both Slave Select (SS) pins work as a hardware input to detect potential bus conflicts between nodes as only one can master the SPI bus at a single time. After the session is completed, the active node master releases the Slave Select signal and returns back to passive slave mode waiting for the next session to start.
Several parameters are used to setup the data format. Users can define the data frame size and the transmit order of the shift register. The clock can be set to one of four basic configurations defined in the Motorola SPI specifications. The combination of two bits controls the polarity and phase of the clock signal. When the phase control bit is cleared, data bits are sampled on the odd clock edges, and the even clock edges synchronize the shifting of the next bit onto the data line. This is the opposite when the phase control bit is set. The clock polarity bit defines the idle state of the clock signal and which clock edge is used for data sampling or shifting.
When the communication speed is fast and data frames too short, it can be a demanding task to ensure correct data flows especially when the clock signal becomes continuous and Full-duplex mode is used. Slave nodes are more critical as they have to follow properly all the transactions timing provided by the master to prevent any data overrun or underrun conditions. When the data frame size fits into a byte, Packing mode can be used. Then multiple data patterns can be written or read in a single access to the FIFO registers. Together with the proper setting of the FIFO threshold event, the number of events to service decreases to better control the data flow. When the DMA is used additionally, the overall load on the system is significantly reduced. In this figure, you can see the principle of how two short 8-bit data frames can be written and read by a single 16-bit access in the dedicated FIFO registers. The read or write data access is performed just upon a single event raised.
SPI peripheral features two 32-bit FIFOs to handle the data flow. The FIFOs can be accessed by using either 8-bit or 16-bit data access instructions. During reception, the event generated from the FIFO depend on threshold setting. The table gives an overview on how the event flag behavior changes depending on the configuration. It is important to keep the FIFO access balanced with the threshold setting so the data consistency is not lost. During transmission, the FIFO occupancy depends on data access. The system can never predict next access to the transmission FIFO, so the FIFO capability is not fully used when 8-bit write access is applied to fill the second half of the FIFO. At this case, TxE flag is cleared as a consequence in spite of the Tx FIFO is not fully occupied. Look at the star in the figure.
During protocol level communications, the DMA controller can be used to automatically handle the data flow events, the CRC calculations, and the updating of the FIFO threshold. In case of threshold control, the last odd data frame is correctly applied in packed mode when the number of frames is not aligned with the packet size.

If the CRC is enabled, separate CRC calculators are used for the transmitter and receiver. The CRC calculation result is automatically appended at the end of each transfer by the DMA controller or by software control. The CRC frame length has to be equal or a multiple of the data size. The CRC calculation is frozen during the CRC pattern transaction.

Results from the transmitter CRC calculator register are loaded directly into the shift register, and the received CRC value is stored in the FIFO and compared with the receiver CRC result. The CRC polynomial used for the calculation is programmable, and the length of the CRC pattern can be set.
to either 8- or 16-bit frames.
The Slave Select signal is commonly used by the master node to select the slave node for communication. The signal implementation is mandatory in multi-master and multi-slave topologies. Though it is not mandatory at a single master-slave pair, it could be helpful for data flow synchronization, regardless of the topology case. The Slave Select signal can operate either as an input or as an output. The NSS input can be managed by hardware or software depending on the SSM and SSI control bits. As a slave input, it is used to identify itself as the active slave for communication. As a master input, it signalizes a potential conflict between masters in a multi-master system. The NSS only works as an output in Master mode and is managed by hardware in a standard or specific control mode. Additional slave select outputs can be provided by the GPIOs under software control.
There are a few enhanced modes when the Slave Select signal is under specific hardware control. The Slave Select signal can operate in a pulse mode where the master generates pulses on the signal between data frames.

- NSS goes high between data frames for 1 SCK period for continuous transactions.
- The clock polarity and phase are fixed, the CPOL setting is ignored, and the CPHA has to be kept cleared.

Another enhanced mode is the TI mode where the data flow is synchronized by the SS pulses provided by the master on the last bit of data.

- The clock polarity and phase configuration is fixed and the slave data output is automatically switched into high impedance when the bus traffic stops and on a specific configurable timeout.
- CPOL=0 CPHA=1 setting has to be kept if CRC is applied in TI mode.
A CRC cannot be applied in NSS pulse mode.
Here is an overview of the SPI interrupt events. There are FIFO and error detection events to handle data flow. DMA requests are triggered internally by FIFO threshold events.

### Interrupts and DMA

<table>
<thead>
<tr>
<th>Interrupt event</th>
<th>Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmit FIFO ready</td>
<td>TXE</td>
<td>Set when TxFIFO is ready to accept new data.</td>
</tr>
<tr>
<td>Receive FIFO ready</td>
<td>RXNE</td>
<td>Set when data is received in the RxFIFO.</td>
</tr>
<tr>
<td>Master mode fault</td>
<td>MODE</td>
<td>Set when there is a bus conflict detected in the multi-master bus configuration.</td>
</tr>
<tr>
<td>Data overrun error</td>
<td>OVR</td>
<td>Receiver can't accept next data flow as the RxFIFO is full.</td>
</tr>
<tr>
<td>TI frame format error</td>
<td>FRE</td>
<td>NSS signal doesn't correspond to the data format.</td>
</tr>
<tr>
<td>CRC protocol error</td>
<td>CRCERR</td>
<td>At the end of the data and CRC transfer, the CRCERR flag is set if corruption occurred during the transfer.</td>
</tr>
</tbody>
</table>

- DMA access is requested internally based on TXE and RXNE FIFO events
  - DMA handles CRC and data threshold control automatically.
Here is an overview of the SPI status in specific low power modes. The device is not able to perform any communication in Stop, Standby or Shutdown modes. It is important to ensure that all the SPI traffic is completed before the peripheral enters Stop or Power down mode.
The SPI performance depends mainly on the applied clock. At a minimum, the clock frequency should be twice the required communication frequency. The actual rate of communication can be decreased by application factors. The user has to consider SPI bus loads such as the number of nodes, the connection distance, the input capacitance, as well as the GPIO settings. Fast GPIO mode should be applied on the data and clock signals. Lower power supply voltage and extreme ambient temperatures slow down edges. Sometimes slower data hold or setup time requirements have to be respected between nodes. Applications can’t always manage the fast data flow due to frequent servicing of exceptions.

The DMA capacity has to be considered as well as the number of DMA channels used by the system, frequent interrupt services or execution of non-interruptible instructions.
The SPI can be used in a wide range of applications where a simple data transfer is required without the need for a complex communication protocol.
Here are some helpful tips:
The user should be aware that traffic on the bus can still be ongoing even if the DMA transaction is complete or the transmit FIFO becomes empty. This is why the user has to carefully check the peripheral’s status and follow the suggested procedures before disabling the SPI or placing it in Stop mode.
Use the DMA if you have a specific verification that requires CRC handling, or receive FIFO threshold verification (when the number of data is not aligned at packet mode), or to receive an exact amount of data in Receive-only mode. These types of verifications must be applied during a specific time window within a frame transaction exclusively so all the following transactions are handled properly.
The DMA and data packing can increase the system’s overall performance. These features can help when data frames are short and a high-speed continuous communication flow is required.
Hardware management of NSS signal is not quite necessary in a single-master/single-slave pair, but it can help synchronize the data flow and prevent conflicts in a multi-master system.

- There are some additional specific aspects which should be taken into account when designing for an SPI network.
- The receiver always loads CRC information into the receive FIFO. The user has to account for this in the buffer and flush it.
- The Busy flag should not be used for any data handling but to check for ongoing traffic. The BSY bit stays set between data frames during the master continuous data transactions. It always drops low for at least one SPI clock cycle between data frames in slave mode, no matter if the communication is continuous or not.
- When the node transmits data only, the receive flow stays active. The user must ignore all receive and associated overrun events in this case.
- The data size to be processed by the DMA when including the CRC is dependent on mode. When a CRC is used, the data size has to be set differently for transmitting and receiving in Full-duplex mode as well as in Receive-only mode.
SPI related peripherals

- Refer to these other peripherals:
  - RCC (SPI clock enable, Clock Control in Sleep, Reset)
  - Interrupts (FIFO and Error events)
  - GPIO (Speed control, GPIO configuration)
  - DMA

Refer to these other trainings which are linked directly to the SPI. Users should be familiar with all the peripherals that can affect the behavior of the SPI.
There are four SPI instances within the STM32G4 microcontroller, and each support all the features described in this presentation. Two of them feature I2S capability in addition.
There are some dedicated SPI application notes. To learn more about general SPI connections and interface issues, there are many web pages, as well as SPI bus monitoring tools available. Many digital oscilloscopes support direct reading and analysis of data and clock signals on the SPI bus.

References

- For more details, please refer to following resources
  - AN4286 - SPI protocol used in the STM32 bootloader
  - AN3364 - Migration and compatibility guidelines for STM32 microcontroller applications
  - Web (connection examples, available monitoring tools)