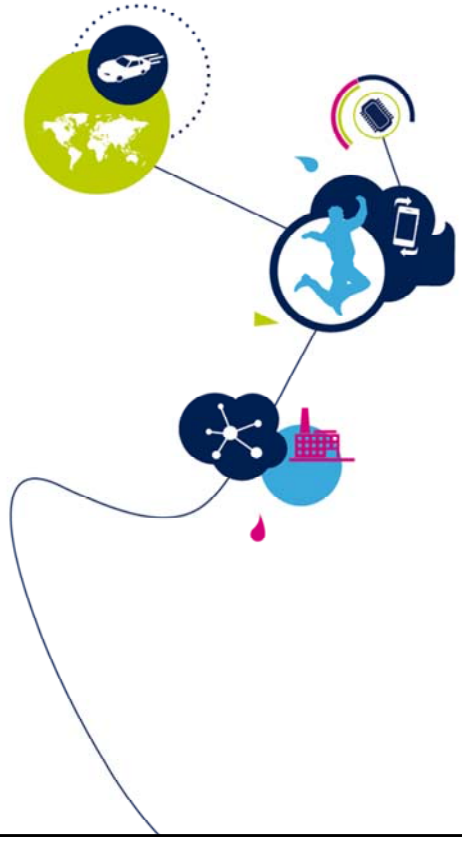
STM32MP1 - USBH

USB Host controller high speed interface
Revision 1.0



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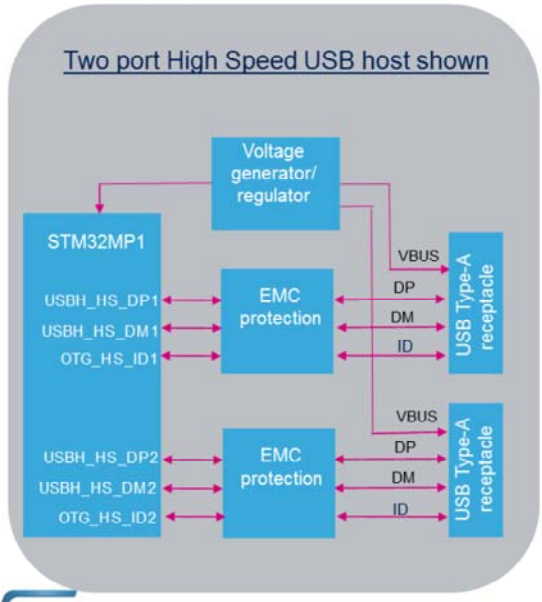
Hello, and welcome to this presentation of the STM32MP1 USB Full Speed and High Speed interfaces. It covers all the features of these interfaces, which are widely used to connect either a PC or a USB device to the microcontroller.

Overview



- Provides USB 2.0 High Speed interfaces
- Two host ports available

Application benefits

- High Speed integrated PHY
- Low-power implementation

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This figure shows the connections between a STM32MP1 microcontroller and two USB connectors. The STM32MP1 features a two port USB High Speed communication interface, allowing the microcontroller to communicate for example with two USB storage devices.

Key features

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- USB 2.0 High Speed (480 Mbits/s) host controller
  - Standard EHCI and OHCI controllers
  - Integrated High Speed PHY
    - Note that the “OTG” can control the 2nd HS port if desired
  - Supports Link Power Management (LPM)

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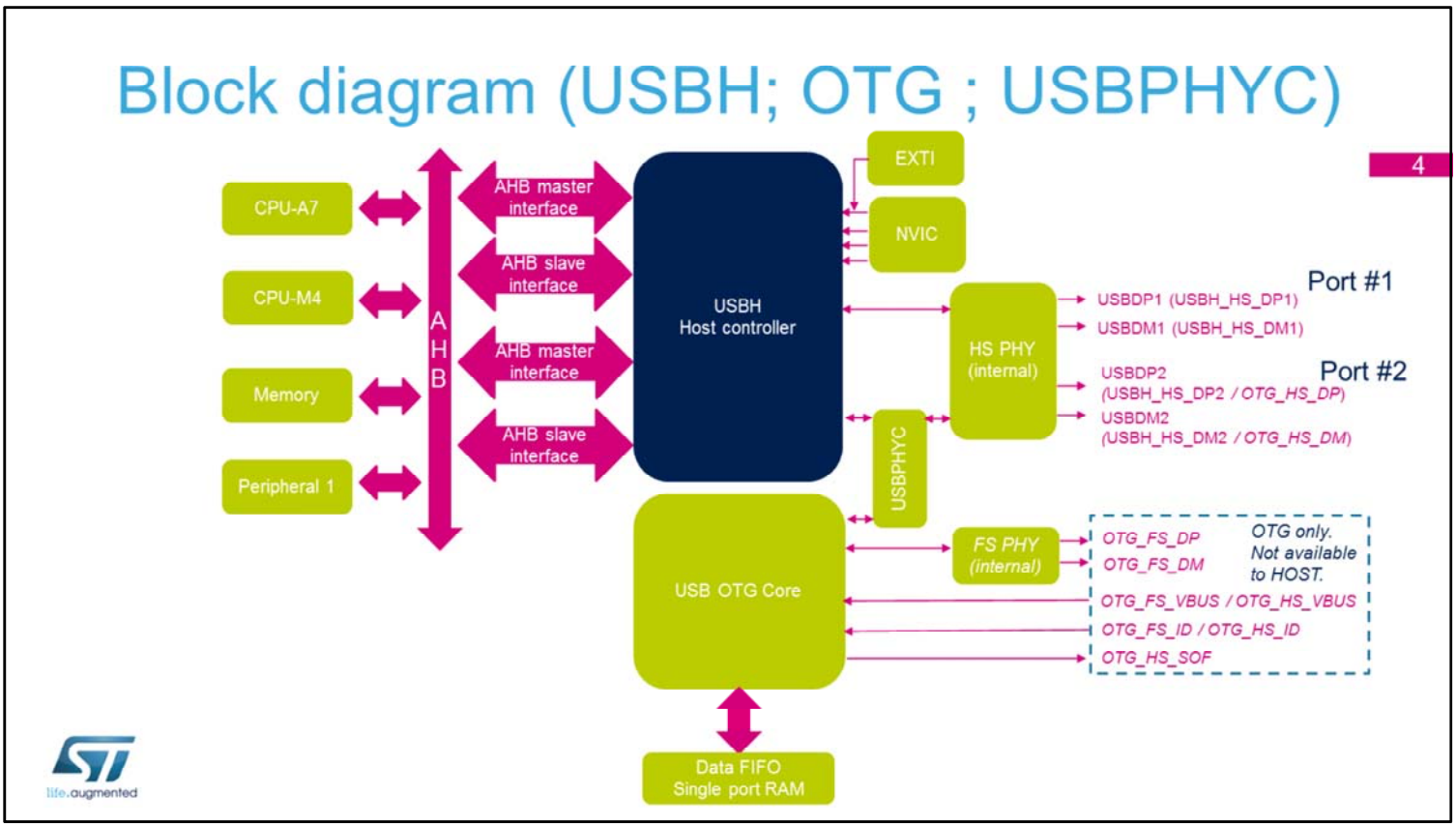
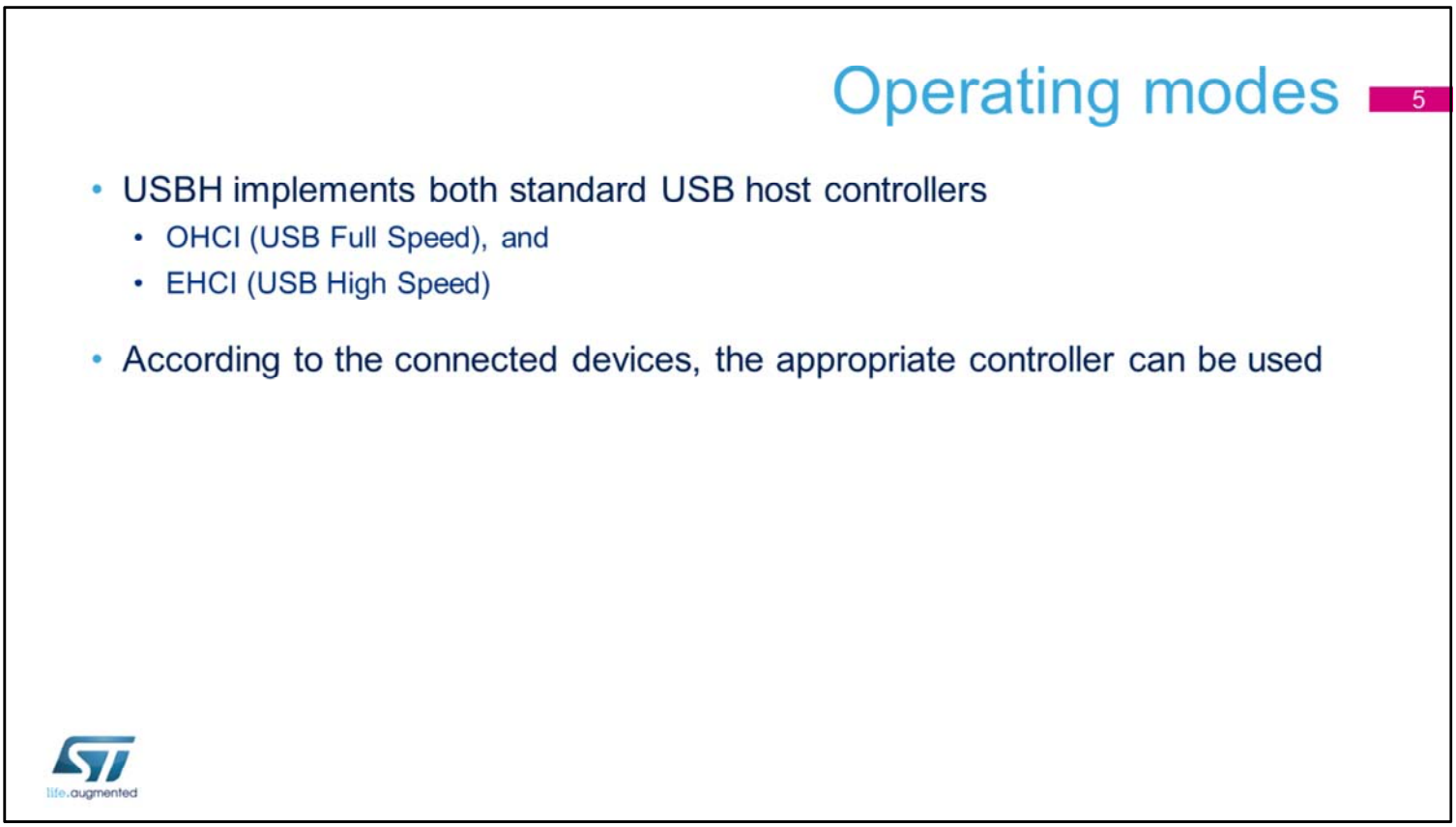
Let’s look at some of the key features of this USB high speed interface, which is a USB specification 2.0 compliant interface that operates at a 480 Megabits per second bit rate.
A USB 2.0 High Speed PHY is integrated on-chip avoiding the need for external ULPI transceivers.
Built-in support for Link Power Management adds enhanced power modes on top of the USB 2.0 specification.
The battery charger detection function allows for increased current to be drawn from BC1.2-compliant chargers up to 1.5A.



In this block diagram, the USB OTG Host controller core is shown at the top. It can be used with both ports of the HS (high speed) PHY. If desired, the 2nd port can be controlled by the OTG controller which also has unique access to the FS (full speed) PHY. These PHYs on its right side handle the analog signal levels including many specific level detections relating to On-The-Go and Battery Charger detection functions. The USB interrupt goes to the Cortex processor to signal various USB events. The AHB slave interface enables read/write access of the controller registers and the Power& Clock control block. Transfers to and from memory are handled by a DMA engine inside the controller via the AHB master interface.



At any given time, one of the two operating modes will be functional:

- Peripheral mode, which will be used for a regular device or an OTG device when operating in Peripheral mode.
- Targeted host mode, which will be used for an embedded host or an OTG device when operating in Host mode.

Interrupts

Interrupt event	Description
OHCI : General interrupt	Combined OHCI interrupt
EHCI : Interrupt on Async Advance	Standard EHCI interrupt
EHCI : Host system error	Standard EHCI interrupt
EHCI : Frame list rollover	Standard EHCI interrupt
EHCI : Port change detect	Standard EHCI interrupt
EHCI : USB error interrupt (USBERRINT)	Standard EHCI interrupt
EHCI : USB interrupt (USBINT)	Standard EHCI interrupt

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Interrupts from this USB block can be triggered by a large number of events or state changes.
This slide shows all the events that can trigger an interrupt.
As can be seen, these interrupt sources are diverse events.

Low-power modes (core level)

Mode	Description
Suspend Gate HCLK	Most of the system clock domain internal to the OTG high-speed core is switched off by clock gating.
Suspend USB system stop	Application may decide to drastically reduce the overall power consumption by a complete shut down of all the clock sources in the system.

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Low-power modes for the High Speed core are similar to the Full Speed, but the modes concerning the PHY are not listed as in this case the PHY (or transceiver) is an external component.

Low-power modes (of the circuit)

MCU mode	Description	USB availability
Run	MCU fully active.	Required until USB enters Suspend mode.
Sleep	Peripheral interrupts cause the device to exit Sleep mode. Peripheral registers content is kept.	Available while USB is in Suspend mode.
Stop/ LV Stop	Peripheral interrupts cause the device to exit Stop mode. Peripheral registers content is kept.	Available while USB is in Suspend mode, offers optimal power reduction.
LP LV Stop	Lower voltage stop mode.	Not compatible with USB applications (no wakeup from SUSPEND possible).
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.	Not compatible with USB applications.

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The USBH controller is fully active in Run mode. During USB suspend, Sleep, Stop and LP Stop modes may be used.

USBPHYC usage

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- USBPHYC is needed in order to use the two port High Speed (HS) UTMI PHY that is integrated in the STM32MP1 microcontroller.
- USBPHYC functions
  - controls the PLL associated with the HS PHY
  - controls the UTMI switch on the shared PHY port #2, enabling the USBH to use that port
  - enables fine tuning of the HS PHY transmitter and receiver, necessary for optimal performance

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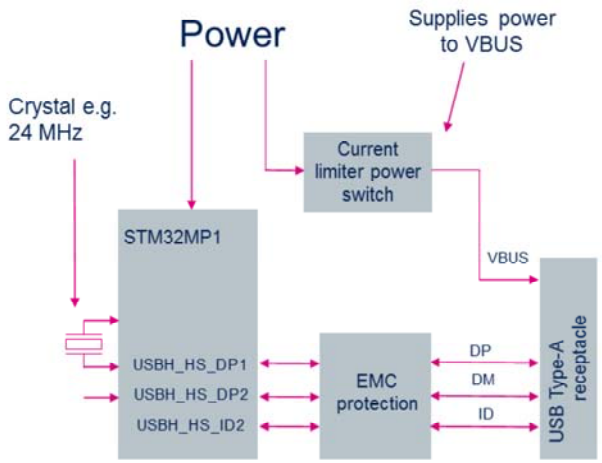
USBPHYC is a small controller needed whenever the High Speed PHY will be used. It is to be used for controlling the PLL inside the High Speed PHY and enabling the USBH controller access to its second port. Fine tuning of the High Speed PHY should also be done by using USBPHYC, this is necessary to get notably a well adjusted eye diagram.

Application: Single port High Speed host



- The schematic shows an example of a single port High Speed host design
- A single 24 MHz crystal oscillator may be used

Here is an application example of a low-power device.
Power is drawn directly from the USB VBUS signal.
A single crystal oscillator (starting from 4 MHz) is needed outside.

References

- For more details, please refer to the following source pages:
  - www.usb.org : Document library page
  - "USB2 specification" => a ZIP file containing:
    - USB2.0 specification
    - On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification (USB2), latest version 1.1a
    - USB 2.0 ECN: Link Power Management Addendum
  - OHCI specification
  - EHCI specification
  - ST Microelectronics MPU Wiki pages

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For complete USB specification documents, please refer to USB.org.
USB2.0 document home page has a ZIP file containing the USB2.0 and OTG2.0 specifications and an ECN for LPM
The USB device class documents page has the battery charger specification.