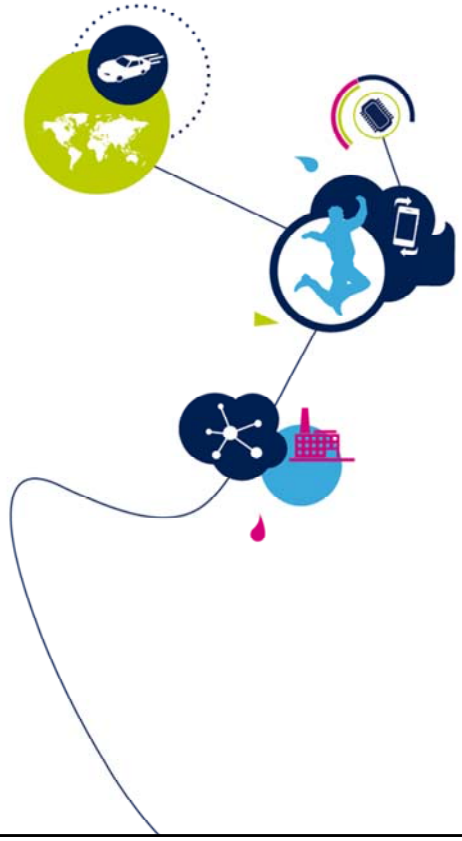
STM32MP1 -EXTI

Extended interrupts and events controller

Revision 1.0



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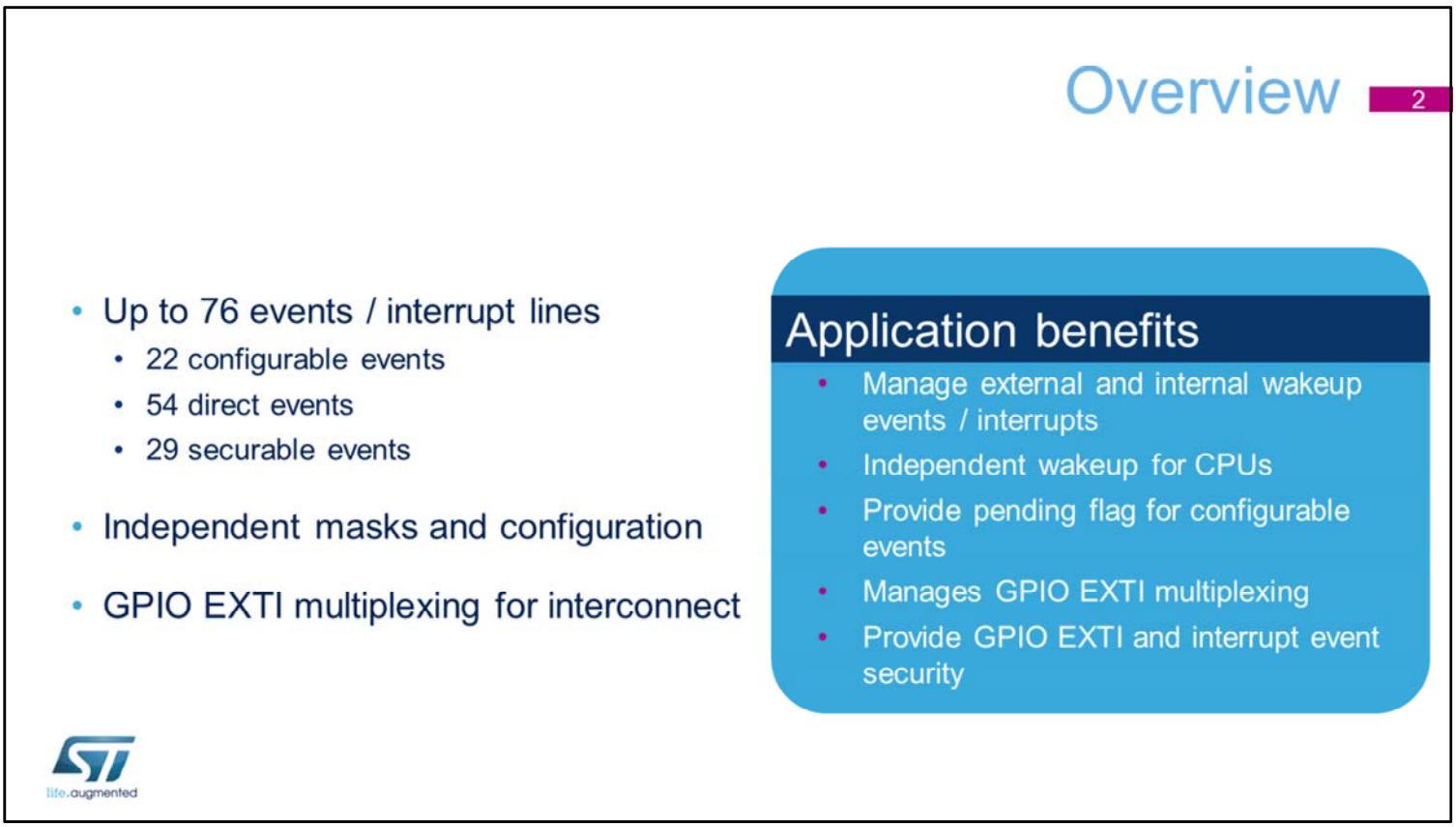
Hello, and welcome to this presentation of the STM32MP1 Extended interrupts and events controller.



The EXTI controller provides up to 105 independent events, split into three categories:

- configurable events
- direct events
- securable events

The EXTI controller can be configured to wake up CPU1, CPU2 or both independently.
Applications benefit through smarter use of low-power modes, taking advantage of the capability to wake up via external communication or requests.
It also is managing the external interconnect line connection to the GPIOs.

Key features (1/2)

- Wakeup from Stop mode, interrupt and event generation functions
  - Independent interrupt and event mask for CPUs
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Active edge selection
  - Dedicated pending flag
  - Trigger-able by software
  - Status flag provided by related peripheral

The EXTI controller provides interrupt and event generation functions, as well as the capability to wake up the processors from Stop modes.
Configurable events allow the user to select which active edge generates an interrupt or event, with a dedicated status flag for each line.
Requests on configurable lines can also be generated by software.
Configurable events are linked with external interrupts from general-purpose input/outputs, comparators, programmable voltage detector, real-time clock, low-power timer, window watchdog, Ethernet controller and HDMI-CEC.

Key features (2/2)

- Direct events (interrupt and wakeup sources from other peripherals, requiring to be cleared in the peripheral)
  - Fixed rising edge active trigger
  - No interrupt pending status register bit in the EXTI (the interrupt pending status is provided by the peripheral generating the event)
  - Individual Interrupt and Event generation mask
  - No SW trigger possibility

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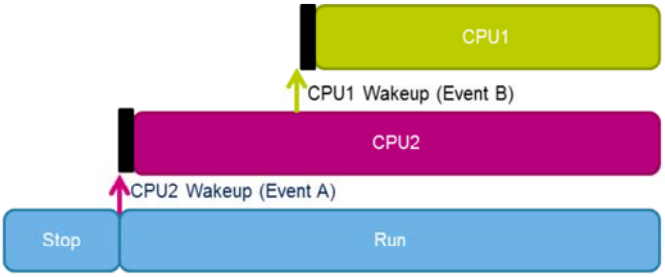
Direct events provide an interrupt or event from peripherals having a status flag requiring to be cleared.

Key features

- When the system is in Run mode, a CPU can be woken up from CStop mode
  - i.e. CPU2 waking up of a CPU1 through IPCC.
- Each CPU must clear its own wakeup events.

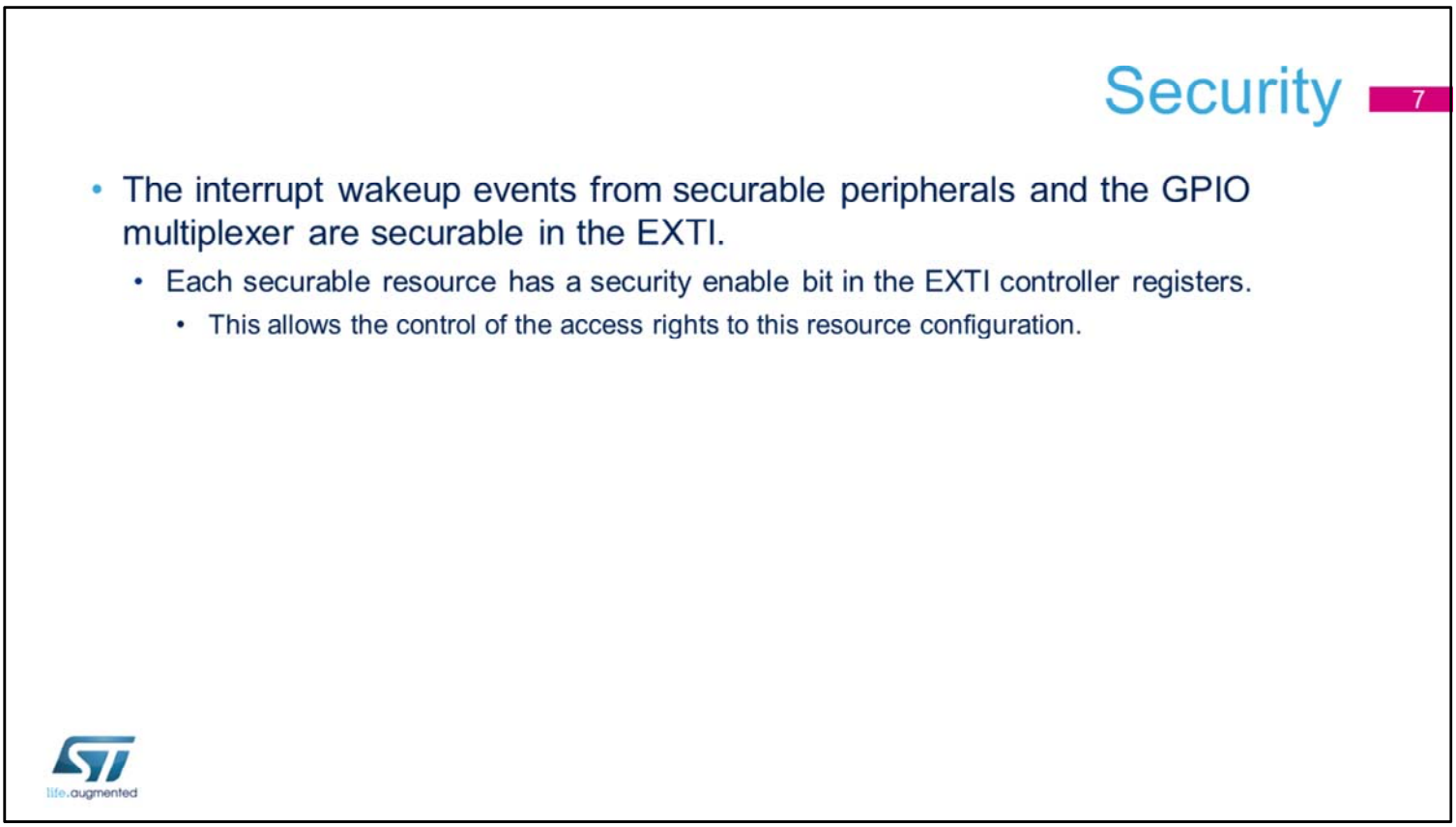


EXTI wakeup events may be configured to wakeup a CPU. Configurable events need to be cleared by the corresponding CPU which has been awaken.

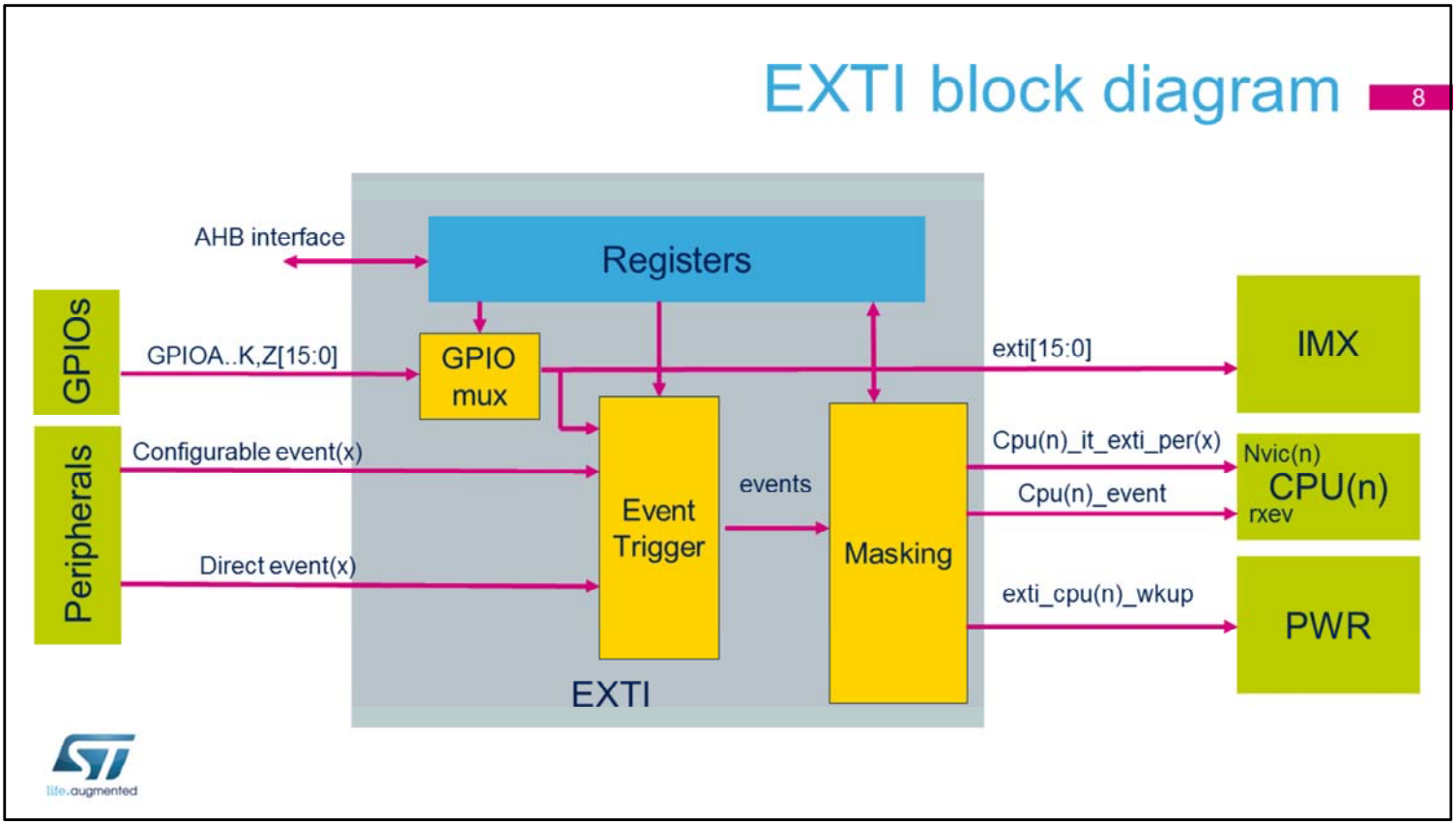
GPIO EXTI multiplexing

- Manage the multiplexing of external interrupt from GPIO (x=A…K, Z) to EXTI event signal
  - 16 Multiplexers to select EXTIn between PA[n] PB[n] …. PK[n], PZ[n] (n=0,…15)
  - select a GPIOx pin to be used as
    - internal interconnect trigger signal to peripherals in the interconnect matrix.
    - CPU interrupt and wakeup from Stop mode via a configurable event.

The External Interrupts and Event Controller allows the selection of GPIOs as sources of interrupts or wakeup events. The GPIOs are connected
via multiplexers to the 16 EXTI events as configurable event to trigger other peripherals through the interconnect matrix (IMX). GPIOs can also be used as configurable interrupt event signal, to generate asynchronous external interrupt or event with wakeup from Stop mode capability. It also allows the selected GPIO pin to be used as an internal interconnect trigger signal to the peripherals.



The interrupt wakeup event from securable peripherals can be secured thanks to enable bits in the EXTI controller registers.
Also the GPIO multiplexer provides individual security enable bits for the 16 peripheral interconnect external event lines.



As shown in this figure, the EXTI consists of a register block accessed via an AHB interface, an event input trigger block, a masking block, and the GPIO multiplexing.
The register block contains all EXTI registers.
The event input trigger block provides event input edge triggering logic.
The masking block provides the event input distribution to the different wakeup, interrupt and event outputs, and their masking.
The GPIO multiplexing block allows to select a GPIO pin to be used as a configurable interrupt trigger event and or as a signal to the peripherals interconnect matrix (IMX).