

STM32H7x5 and STM32H7x7 Lines WDSO

Watchdog Timers System Overview
Revision 1.0



Hello, and welcome to this presentation of the system overview of the Watchdog Timers for the STM32H7x5 and STM32H7x7 MCU lines.

- STM32H7x5 and STM32H7x7 microcontrollers feature four embedded watchdog blocks
- Option bytes can be used to adapt the behavior of the watchdogs to the user application

Application benefits

- High safety
- Timing accuracy and flexibility



STM32H7x5 and STM32H7x7 microcontrollers feature four embedded watchdog blocks which offer a combination of high safety, timing accuracy and flexibility. Option bytes can be used to adapt the behavior of the watchdogs to the user application.

Watchdog features

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- Two independent watchdogs (IWDG1/2), each dedicated to a CPU
- Two window watchdogs (WWDG1/2), each dedicated to a CPU
- Each CPU can receive an interrupt if the other CPU has been reset due to a window watchdog timeout.
- Each CPU can receive the early interrupt of its dedicated window watchdog.
- Watchdog functions can be configured through option bytes.

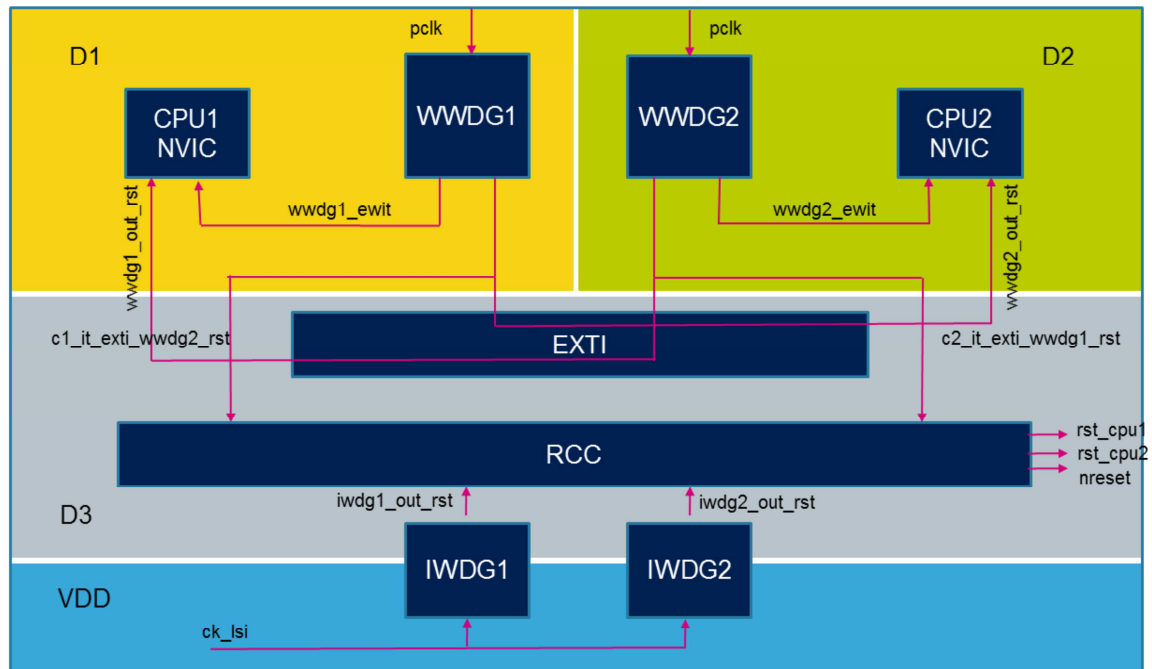


The embedded watchdog blocks feature two independent watchdogs (IWDG1/2), and two window watchdogs (WWDG1/2), each dedicated to a CPU. Each CPU can receive an interrupt if the other CPU has been reset due to a window watchdog timeout and each CPU can receive the early interrupt of its dedicated window watchdog.

Watchdog functions can be configured through option bytes.

Block diagram

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Watchdogs IWDG1 and WWDG1 are dedicated to CPU1, while watchdogs IWDG2 and WWDG2 are dedicated to CPU2. Both watchdog peripherals (Independent and Window) allow detecting and resolving malfunctions due to software or hardware failures.

The window watchdogs (WWDG1/2) clocks are derived from the APB clocks and have a configurable time window that can be programmed to detect abnormally late or early application behavior.

The WWDGs are best suited for monitoring software execution. Each WWDG provides a reset and an early interrupt signal.

The independent watchdogs (IWDG1/2) are clocked by the low-speed clock (LSI) and thus stay active even if the main clock fails. They are consequently best suited for applications which require the watchdog to run totally independently of the main application. The IWDGs are

ideal solutions to recover from unexpected software or hardware failures.

Watchdog clock enable

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- Each core can enable the window watchdog clocks via the RCC block.
 - CPU1 enables WWDG1 with RCC_APB3ENR register, while CPU2 enables WWDG2 with RCC_APB1LENR register.
 - A core cannot enable the window watchdog managed by the other core
 - WWDG cannot be stopped by setting WWDGxEN bit to 0
- The IWDG1/2 watchdogs do not need their clock to be enabled by the RCC block.
 - IWDG1 is implicitly allocated to CPU1, and IWDG2 to CPU2.
 - IWDG1 and IWDG2 are automatically enabled after a system reset via an option byte.



Each core can enable the window watchdog clocks via the RCC block. Setting the WWDG1EN bit in the RCC_APB3ENR register enables the WWDG1 block clock, while setting the WWDG2EN bit in the RCC_APB1LENR register enables the WWDG2 block clock.

The software cannot stop WWDG1 and WWDG2 down-counting by setting WWDG1EN and WWDG2EN bit to '0', respectively.

Note that none of the cores can enable the window watchdog managed by the other core.

The independent watchdogs do not need their clock to be enabled by the RCC block. IWDG1 is implicitly allocated to CPU1, and IWDG2 to CPU2. An option byte allows IWDG1 and IWDG2 watchdogs to be automatically enabled after a system reset.

Watchdog behavior versus CPU state

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- WWDG block is frozen when the corresponding CPU enters CSTOP mode.
- When the domain enters DSTANDBY state, the WWDG block located in this domain is reset.
- IWDG blocks always remain enabled once enabled. Two option bytes allow freezing IWDG down-counting:
 - IWDG_FZ_STOP option byte allows freezing IWDG1/2 down-counting when the CPU1/CPU2 is entering CSTOP mode or deeper low-power mode.
 - IWDG_FZ_STANDBY option byte allows freezing IWDG1/2 down-counting only when the product enters Standby mode.



A WWDG block is frozen when the corresponding CPU enters the CSTOP mode. When the domain enters DSTANDBY state, the WWDG block located in this domain is reset.

IWDG blocks always remain enabled once enabled. Two option bytes allow freezing IWDG down-counting:

- IWDG_FZ_STOP option byte allows freezing IWDG1/2 down-counting when the CPU1/CPU2 is entering CSTOP mode or deeper low-power mode (DSTOP ["D" "STOP"], DSTANDBY or product Standby mode).
- IWDG_FZ_STANDBY option byte allows freezing IWDG1/2 down-counting only when the product enters Standby mode.

Related peripherals

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- Please refer to these peripheral trainings for more information if needed.
 - Reset and clock control (RCC)
 - System window watchdog (WWDG)
 - Independent watchdog (IWDG)



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