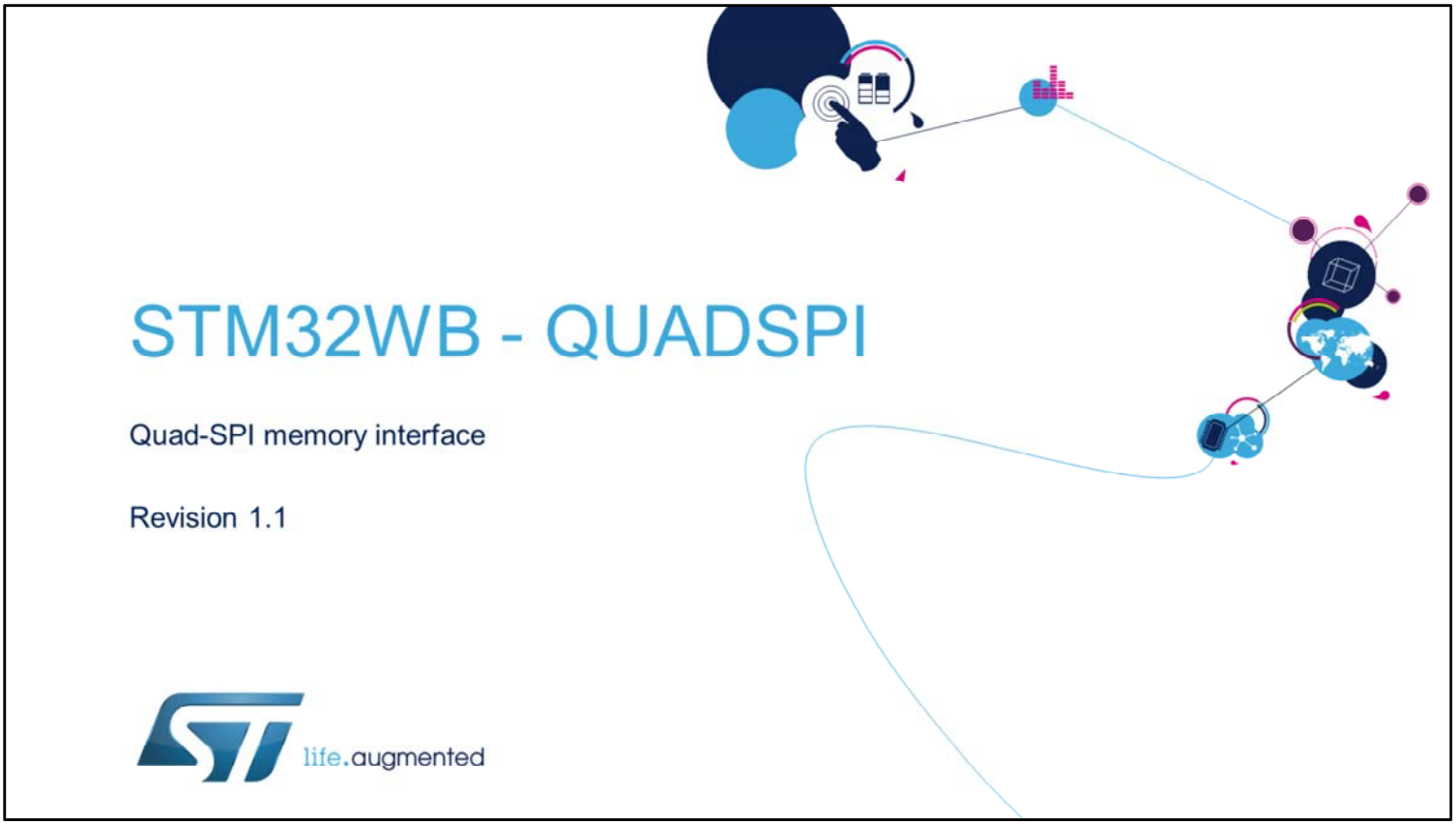
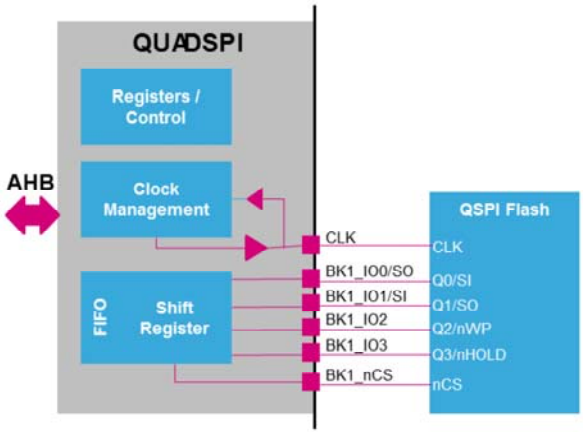


Hello, and welcome to this presentation of the STM32 Quad-SPI memory interface. It covers the main features of this interface, which is widely used for connecting external memories to the microcontroller.

Overview



- The Quad-SPI memory interface provides a communication interface with external serial Flash memories
  - Fully configurable
  - Supports Execute in Place (XiP)
  - Memory mapped

Application benefits

- Supports all SPI Flash memories
- Only a few pins needed
- Simple to integrate additional memory in existing project

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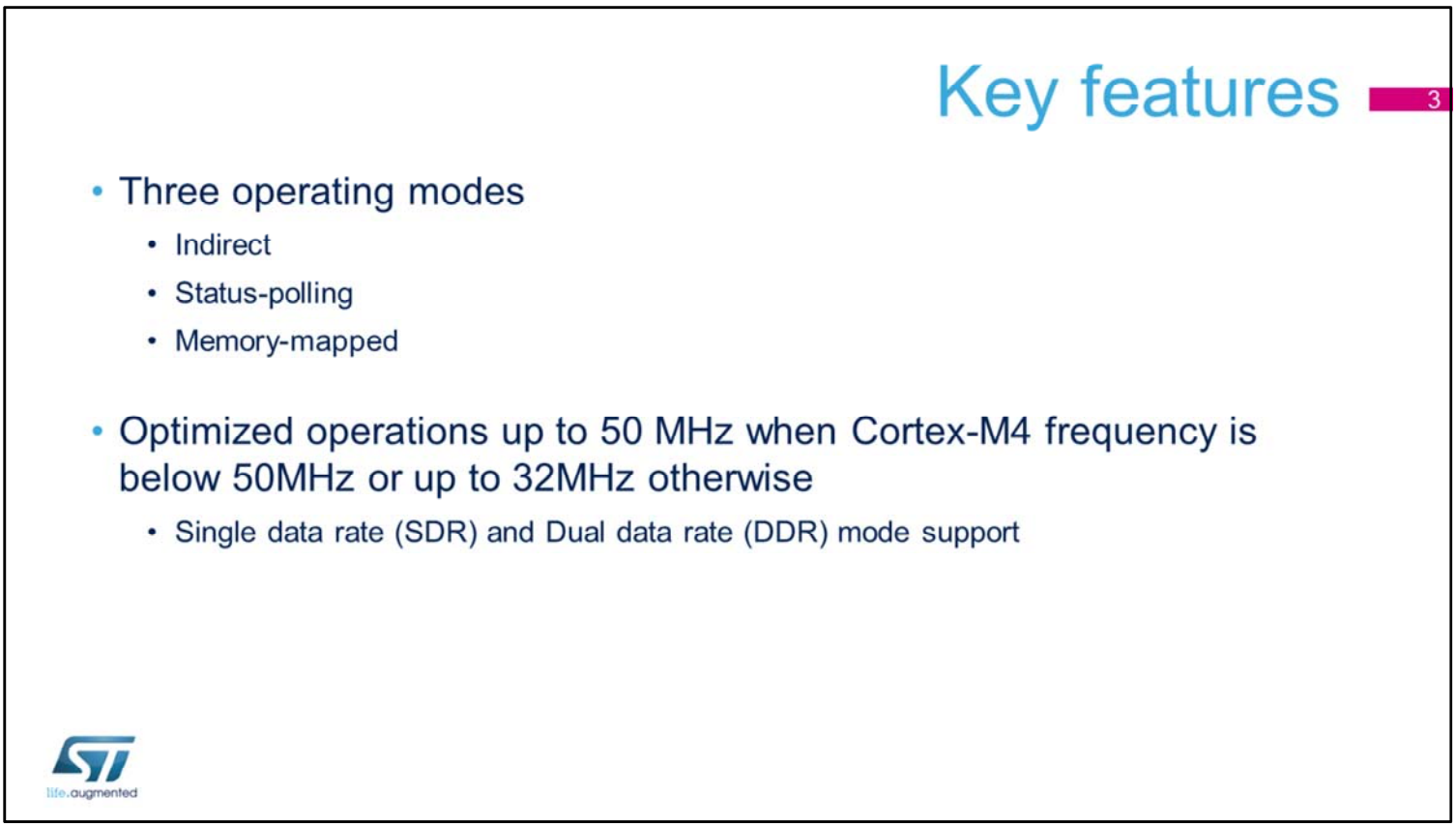
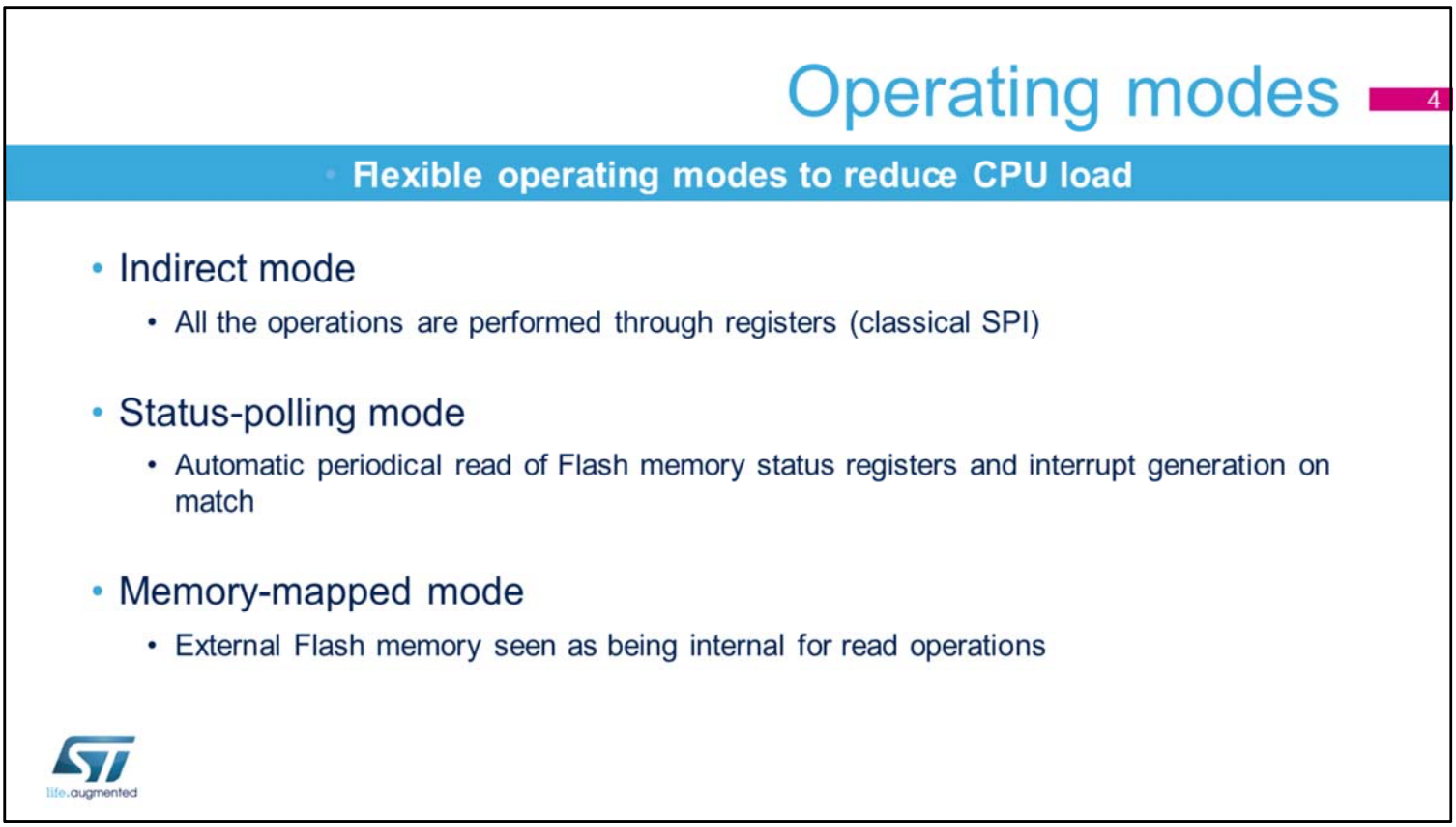
The Quad-SPI memory interface integrated inside STM32 products provides a communication interface, allowing the microcontroller to communicate with external SPI and Quad-SPI memories. This interface is fully configurable, allowing easy connection of any existing serial memories available today on the market. Applications can benefit from the easy connection of external serial memories, requiring only few pins. Thanks to the memory mapping feature, external memories can be simply accommodated in the existing project whenever more memory space is needed.



The Quad-SPI memory interface integrated inside STM32 products offers three operating modes and is optimized for communication with external memories with support for both single- and dual-data rate operation, allowing the access of 8 bits in single read cycle in DDR mode.
When the Cortex-M4 frequency is below 50 MHz, the Quad-SPI block can use the same clock frequency for the bus. When the Cortex-M4 frequency is higher (up to 64MHz), the Quad-SPI prescaler must ensure a clock division by at least 2.

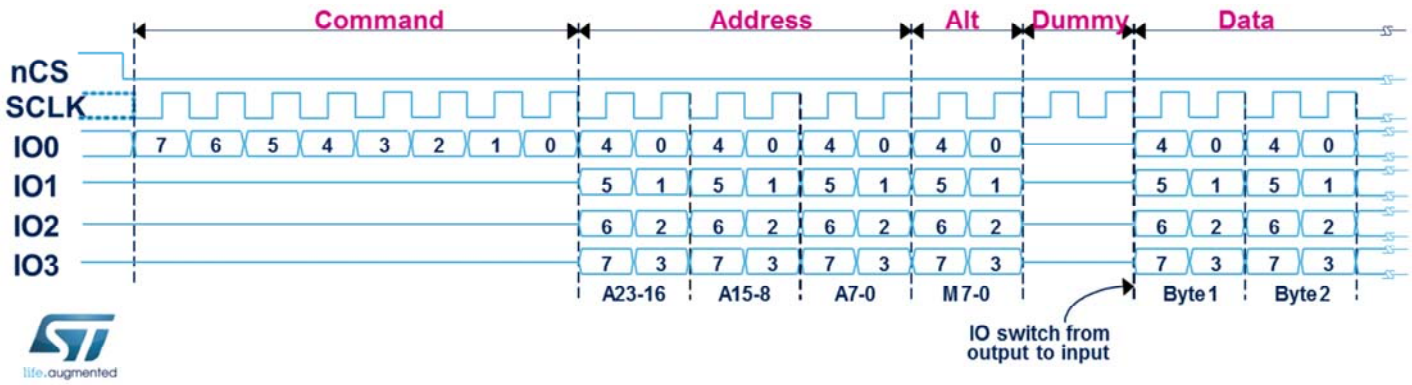


The Quad-SPI memory interface operates in three different modes:
1. Indirect mode, where it behaves as classical SPI interface and all operations are performed through registers,
2. Status-polling mode, where the Flash status registers are read periodically with interrupt generation,
3. Memory-mapped mode, where the external memory is seen as an internal memory for read operations.

Frame format

Compatible with any single/dual/quad SPI serial Flash memory

- QSPI commands contains up to 5 configurable phases
  - Each phase can be enabled or disabled
  - Configurable length for each phase
  - Configurable number of lines for each phase



The Quad-SPI memory interface offers high flexibility in frame format configuration. This flexibility allows addressing any serial Flash memory. Users can enable or disable each of the five phases and configure the length of each phase as well as the number of lines used for each phase.

Indirect operating mode

Classical SPI interface

- Same usage as a classical communication IP
  - The data is transferred writing or reading data register
  - Number of bytes specified in the data length register
- Management of data FIFO with
  - Interrupts flag (Transfer Complete flag)
  - DMA support
- Launching a command
  - When writing the instruction if only instruction is needed
  - When writing the address if only instruction & address are needed
  - When writing the data when only data phase is needed

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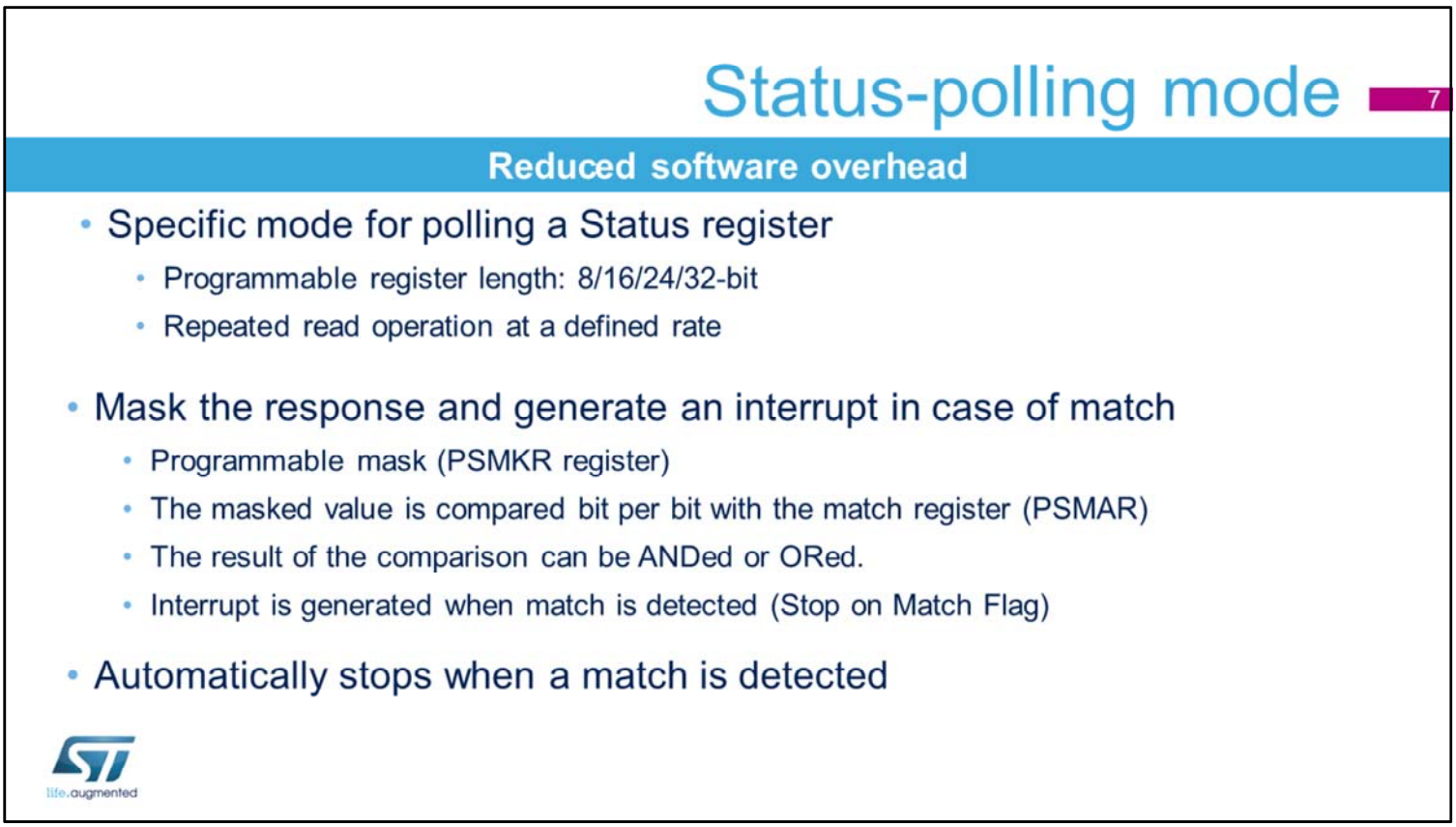
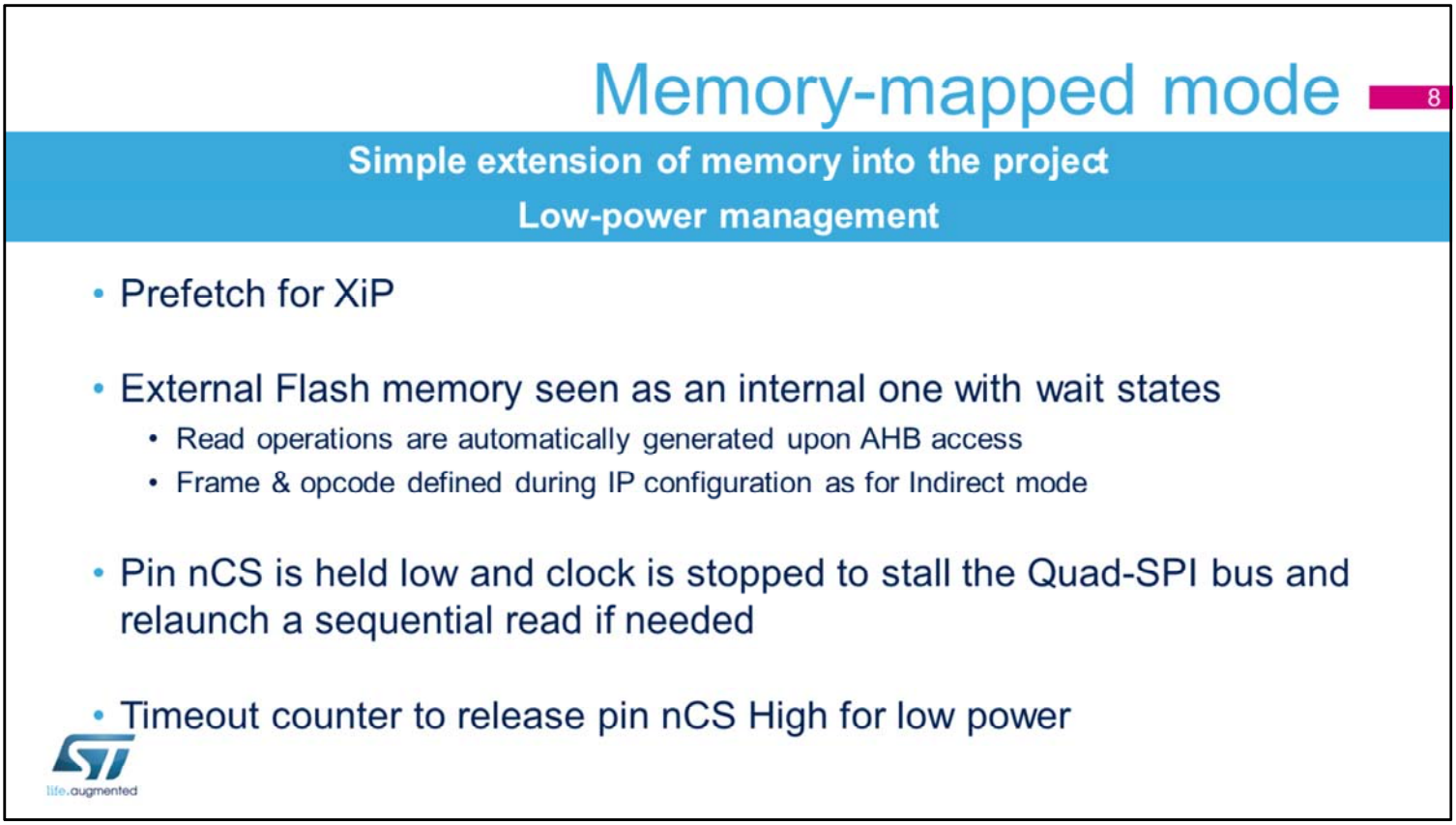
The Quad-SPI memory interface used in indirect operating mode behaves like a classical SPI interface. Transferred data goes through the data register with FIFO. Data exchanges are driven by software or by DMA, using related interrupt flags in the Quad-SPI status registers.
Each command is launched by writing the instruction, address or data, depending on the instruction context.

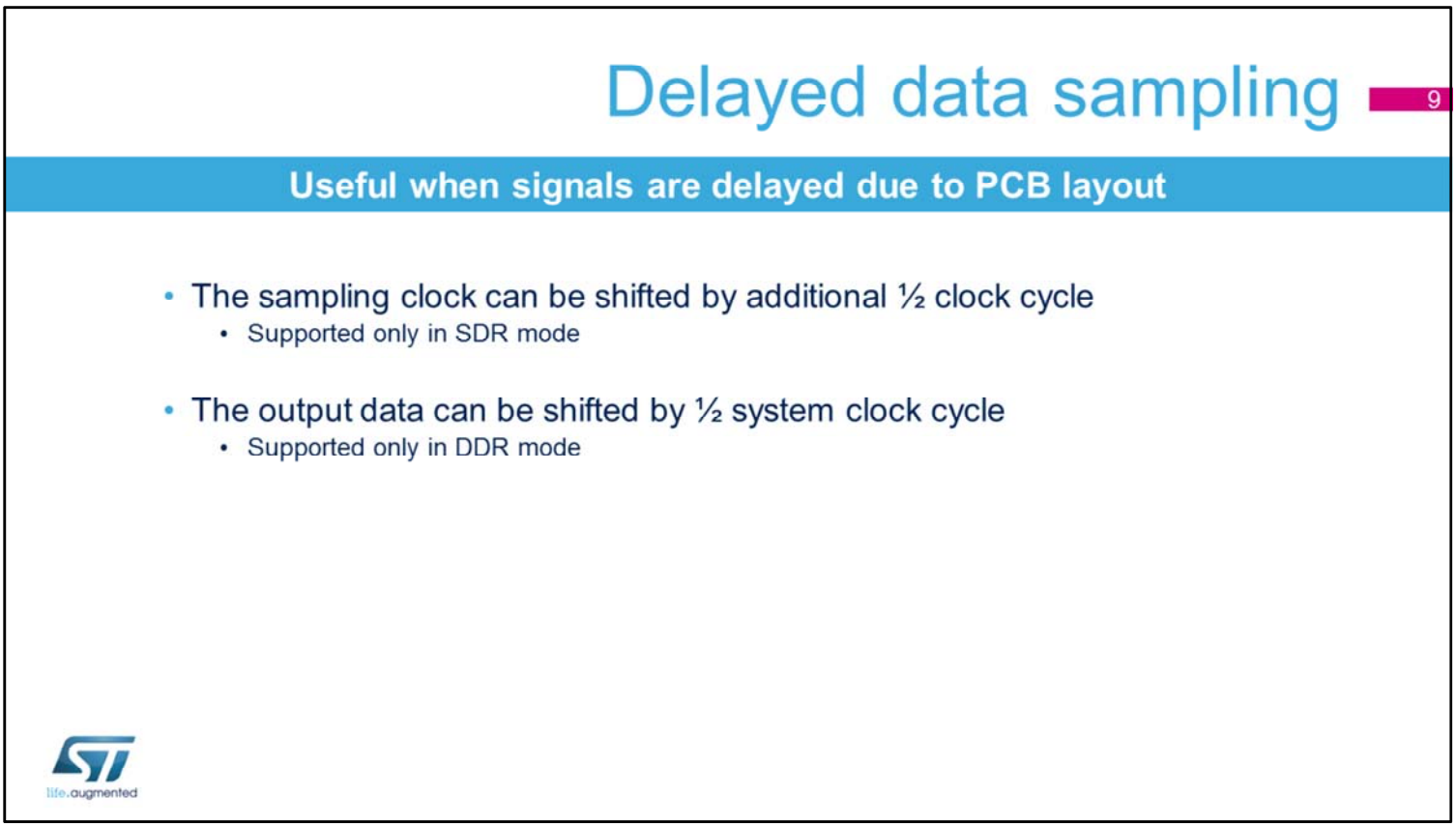


A specific mode has been implemented in the Quad-SPI interface to autonomously poll the status registers in the external Flash memory. The Quad-SPI interface can also be configured to periodically read a register in the external Flash memory. The returned data can be masked to select the bits to be evaluated. The selected bits are compared with their required values stored in the match register. The result of the comparison can be treated in two ways: in ANDed mode, if all the selected bits are matching, an interrupt is generated. In ORed mode, if one of the selected bits is matching, an interrupt is generated. When a match occurs, the Quad-SPI interface can stop automatically.



The Quad-SPI memory interface also has a Memory-mapped mode. The main application benefit introduced by this mode is the simple integration of an external memory extension thanks to their being no difference between the read accesses of internal or externally-connected memories, except the number of wait states. This mode is only suitable for read operations and the external Flash memory is seen as internal one with wait states included to compensate for the lower speed of the external memory. The maximum size supported by this mode is limited to 256 Mbytes.
The prefetch buffer supports execution in place, therefore code can be executed directly from the external memory without having to download it into the internal RAM.
This mode also supports SIOO mode (Send Instruction Only Once) supported by certain Flash memories, which

allows the controller to send an instruction only once and to remove the instruction phase for following accesses.



Delayed data sampling allows users to compensate for the delay of the signals due to constraints on the PCB layout optimization. It allows applications to shift the data sampling time by an additional ½ clock cycle when operating in SDR mode. In DDR mode, the output data can be shifted by ½ system clock cycle to relax hold constraints.

Interrupts and DMA

Interrupt event	Description
Timeout	Set when timeout occurs.
Status match	Set in Automatic Polling mode when the masked received data matches the corresponding bits in the match register.
FFO threshold	Set in Indirect mode when the FIFO threshold has been reached.
Transfer complete	Set in Indirect mode when the programmed number of data has been transferred or in any mode when the transfer has been aborted.
Transfer error	Set in Indirect mode when an invalid address is being accessed.

- DMA requests can be generated in Indirect mode when FIFO threshold is reached.

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The Quad-SPI memory interface has 5 interrupt sources: Timeout, Status Match when the masked received data matches the corresponding bits in the match register in Automatic Polling mode, FIFO Threshold, Transfer Complete and Transfer Error.
DMA requests can be generated in Indirect mode when the FIFO threshold is reached.

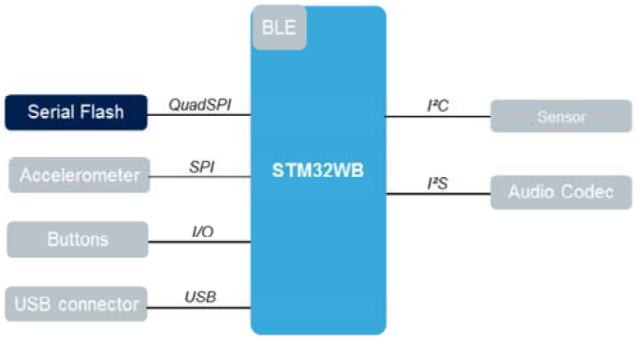
Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Low-power run	Active.
Low-power sleep	Active. Peripheral interrupts cause the device to exit Low-power sleep mode.
Stop 0/Stop 1/Stop 2	Frozen. Peripheral registers content is kept.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.
Shutdown	Powered-down. The peripheral must be reinitialized after exiting Shutdown mode.

The Quad-SPI memory interface is active in Run, Sleep, Low-power run and Low-power sleep modes. A Quad-SPI interrupt can cause the device to exit Sleep or Low-power sleep modes. In Stop 0, Stop1 or Stop2 mode, the Quad-SPI is frozen and its registers content is kept. In Standby or Shutdown mode, the Quad-SPI is powered-down and it must be reinitialized afterwards.

Application examples

- Wearable application including connectivity and user interface:



- External Quad-SPI can store sensor data logging or audio data required for user interfaces.

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Wearable applications require low-power management functions together with sensor data logging and possible audio interface. This can be achieved using the Quad-SPI interface to store in an external Flash memory data log for sensor. Additional audio data for ringtones or audio message generation can also benefit from the large space offered by an external Flash memory. The low pin-count needed to drive such devices allows for a highly optimized system integration.

Related peripherals

- Refer to these peripherals trainings linked to this peripheral:
  - RCC (Quad-SPI clock control, Quad-SPI enable/reset)
  - Interrupts (Quad-SPI interrupt mapping)
  - DMA (Quad-SPI data transfer)
  - GPIO (Quad-SPI input/output pins)

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You can refer to the Peripherals training slide related to RCC, interrupts, DMA and GPIO for additional information.

References

- For more details, please refer to following resources
  - AN4760 - Quad-SPI (QSPI) interface on STM32 microcontrollers

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For more details, please refer to application note AN4760, Quad-SPI interface on STM32 microcontrollers.
Thank you