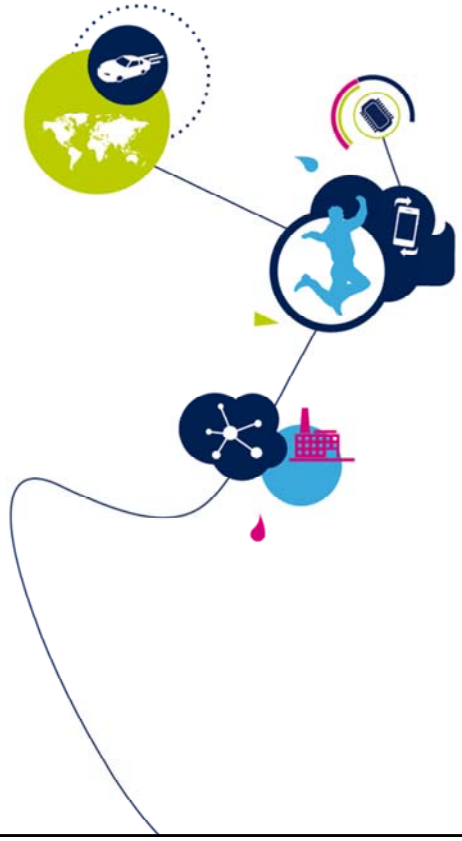
# STM32MP1 - DMA

Direct memory access controller (DMA)
Revision 1.0



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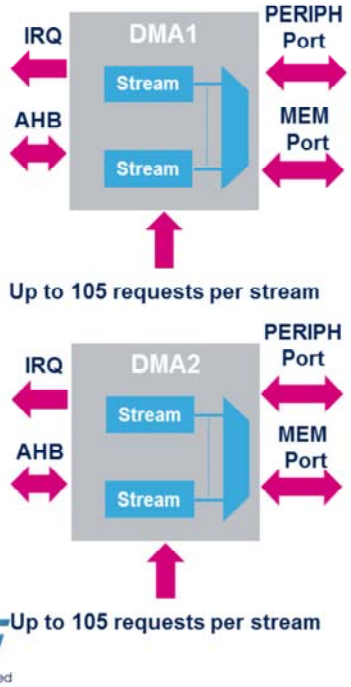
Welcome to the presentation of the STM32 direct memory access controller (DMA). It covers the main features of this module, which is widely used to handle the STM32 peripheral data transfers.

# Overview






- DMA1/2 features
  - Dual AHB master bus
  - Flexible configuration
  - Hardware and software priority management
  - Configurable data transfer modes
    - Peripheral-to-Memory, Memory-to-Peripheral, and Memory-to-Memory modes

## Application benefits

- DMA support for timers, ADC, and communication peripherals in D2 domain
- Offloads CPU from data transfer management
- Simple integration

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The two identical instances of Direct Memory Access (named DMA1 and DMA2 ) embedded on the STM32MP1 series are used to provide high-speed data transfers between peripherals and the memory and between memory and memory. Data can be quickly moved by the DMA without any CPU action. This keeps CPU resources free for other operations.

The DMA controller combines a powerful dual AHB master bus architecture with an independent FIFO to optimize the system’s bandwidth, based on a complex bus matrix architecture.

# Key features



- 16 independent configurable streams over DMA1 & DMA2
  - Streams provide a unidirectional transfer link between a source and a destination
  - Hardware request or software trigger on each stream
  - Software-programmable priorities with hardware priority in case of equality
- Independent and flexible stream configuration
  - Fully programmable transfer (data format, increment type, and address)
  - Independent stream interrupt flags (half transfer, transfer complete, transfer error,…)
  - Dedicated 4x32-bit FIFO memory for each stream (FIFO mode can be enabled or disabled).
  - Support for circular buffer and double buffer management.
- Faulty stream is automatically disabled in case of errors:
  - DMA Transfer Error and Direct Mode Error

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The two DMA controllers (DMA1 and DMA2) have 16 streams in total, each dedicated to managing memory access requests from many peripherals. Each stream has flexible hardware requests and support for software triggers. The stream software priority is programmable and a hardware priority is used in case of equality. Streams are independently configurable. Each stream has its own data format, increment type and data address for both source and destination.

A four-word FIFO per stream allows performing data packing/unpacking and burst transfers.

Independent stream interrupt flags allow triggering half transfer, transfer complete, and transfer error events. In case of a transfer error, the faulty stream is automatically disabled without any impact on the other active DMA streams.

# Individual DMA stream flexibility

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- Programmable features
  - Independent source and destination data size (8/16/32 bits)
  - Independent source and destination transfer types:
    - Single or incremental burst (4x, 8x or 16x beats)
  - Independent source and destination addresses
  - Independent source and destination pointer address increment
  - Programmable number of data to be transferred up to 65,535 requests
- Circular mode
  - Handles circular buffers with continuous data flow
  - Source and Destination addresses are automatically reloaded
  - Data transfer size is automatically reloaded
  - Double buffer mode (Double buffer mode can enabled or disabled).

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For each stream, the source and destination data size format is independently configurable for 8-, 16- or 32-bit packets. The transfer type for the source and the destination can be independently programmed in single mode or burst mode. The source and destination addresses and pointer increment are also independently configurable. The transfer data size can be pre-programmed up to 65535. Circular buffer mode is available to support a continuous flow of data. The source and the destination addresses and the number of data to be transferred are automatically reloaded after the complete transfer. Double Buffer mode allows the switching between two memory buffers to be managed by hardware.

# Stream transfer management



- Memory-to-Memory mode
  - Transfer starts as soon as the stream is enabled (No hardware request)
- Peripheral-to-Memory, Memory-to-Peripheral,
  - A transfer on DMA peripheral port occurs on each hardware request
  - Once the transfer is completed, the request is acknowledged
- The peripheral DMA request signal is routed to the DMA controller stream request line via the DMA request router (DMAMUX)

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Memory-to-memory mode allows transfers from one address location to another without a hardware request. Once the stream is configured and enabled, the transfer starts immediately. When data is transferred to or from a peripheral, the hardware request coming from the selected peripheral is used to trigger the data transfer on the DMA Peripheral port. Once the transfer is completed, the request is acknowledged.

# FIFO: data packing/unpacking

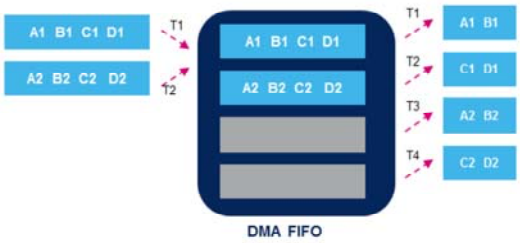


- Supported operations:
  - 8-bit / 16-bit → 32-bit / 16-bit (Packing)
  - 32-bit / 16-bit → 8-bit / 16-bit (Unpacking)

**Data Packing Example (8-bit → 32-bit)**


- Source data width = 8-bit
- Destination data width = 32-bit
- 8 transfers are performed from source to DMA FIFO.
- 2 transfers are performed from DMA FIFO to destination.

**Data Unpacking Example (32-bit → 16-bit)**




- Source data width = 32-bit
- Destination data width = 16-bit
- 2 transfers are performed from source to DMA FIFO.
- 4 transfers are performed from DMA FIFO to destination.

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When FIFO mode is enabled (Direct mode disabled) the DMA controller manages the data format difference between source and destination (data packing and unpacking). Thanks to its internal FIFO, the DMA stream can reduce software overhead and the number of transactions over the AHB Bus.

# FIFO: Threshold & Burst mode



- Threshold level triggers the data transfers to/from Memory.
- Each stream has independent configurable threshold levels:
  - Four threshold levels available:¼ FIFO Full ,1/2 FIFO Full, ¾ FIFO Full, and FIFO Full
- Burst mode:
  - Burst mode is available only when FIFO mode is enabled (Direct mode dsabled)
  - Available Burst modes:
    - INC4: 1 burst = 4 beats (4 Words, 8 Half-Words or 16 Bytes)
    - INC8: 1 burst = 8 beats (8 Half-Words or 16 Bytes)
    - INC16: 1 burst = 16 beats (16 Bytes)
  - FIFO threshold should be compatible with Burst size

| Memory data size | Burst Size | Allowed threshold levels |
|---|---|---|
| Byte | 4 beats (INC4) | ¼½ ¾ and Full |
| | 8 beats (INC8) | ½ & Full |
| | 16 beats (INC16) | Full |
| Half-Word | 4 beats (INC4) | ½ & Full |
| | 8 beats (INC8) | Full |
| Word | 4 beats (INC4) | Full |

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In Single or Burst mode, the FIFO threshold level determines when the data in the FIFO should be transferred to/from memory.

There are four configurable threshold levels per stream starting from “one quarter FIFO Full” to “FIFO Full”.

Depending on the transfer direction on the memory port, when the FIFO threshold is reached, the FIFO is filled from or flushed to the memory location.

Burst mode is only available when FIFO mode is enabled. When setting Burst mode, the FIFO threshold should be compatible with burst size. It allows the DMA streams to have the burst data available in the FIFO to carry out a burst transfer.

# Circular & Double buffer modes

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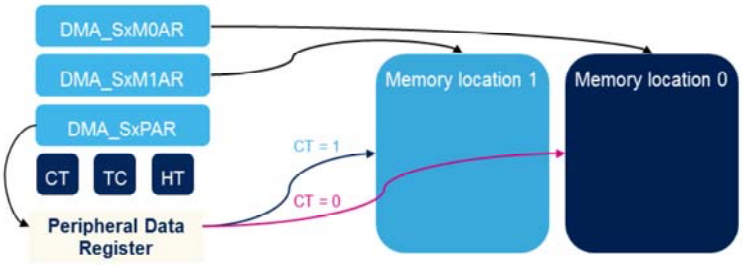
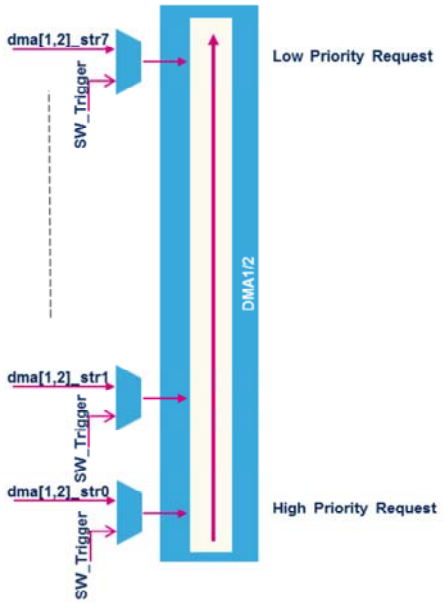
- Circular mode:
  - All FIFO features and DMA events (TC, HT, TE) are available in this mode.
  - The number of data items is automatically reloaded and transfer restarted
  - This mode is NOT available for Memory-to-Memory transfers.
- Double Buffer mode: (Circular mode only)
  - Two memory address registers are available (DMA_SxM0AR & DMA_SxM1AR)
  - Allows switching between two memory buffers to be managed by hardware.
  - Memory-to-Memory mode is prohibited
  - A flag & control bit (CT) is available to monitor which destination is being used for data transfers
  - TC flag is set when transfer to memory location 0 or 1 is complete.




DMA controllers support Circular mode allowing to configure the number of data items to transfer once, and automatically restart the transfer after a Transfer Complete event. Double buffer mode is only available in Circular mode. It allows to switch automatically by hardware between two memory addresses each time a Transfer Complete event occurs. In Double buffer mode, a status flag and control bit (CT) is available to monitor which destination is being used for data transfers.

# DMA controller






The DMA controller provides access to 8 streams with up to 115 channels (requests) per stream. Each of the 8 streams are connected to dedicated hardware DMA channels (requests).

The priorities between the DMA stream requests are software-programmable (4 levels consisting of very high, high, medium, and low) or hardware in case of equality (request 0 has priority over request 1, etc.).

Each DMA controller stream request can be connected to DMA requests from up to 115 possible peripherals by the DMA request router (DMAMUX). This selection is software-configurable and allows a great number of peripherals to initiate DMA requests.

Each stream also supports software trigger for memory-to-memory transfers.

# Interrupts



- Interrupt events for each channel

| Interrupt event | Description |
|---|---|
| Half transfer | Set when half of the data tansfer size has completed. |
| Transfer complete | Set when the full data tansfer size has completed, can be used as tigger to MDMA or DMAMUX. |
| Transfer error | Set when a bus error occurs during the data tansfer. |
| FIFO Error | Set when FIFO Underrun/overrun condition or Threshold-burst size incompatibility. |
| Direct Mode Error | Only available in Peripheral-to-Memory mode, in Direct mode, when Memory Incrementation is disabled.<br>Indicates that a new data is being transferred to memory location whereas the previous transfer is not complete yet. |

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Each DMA stream is designed with this group of interrupt events. The Half Transfer interrupt flag is set when half the data has been transferred; the Transfer Complete flag is set when the transfer is complete; the Transfer Error flag is set when an error occurs during the data transfer; the FIFO Error flag is set whenever a DMA FIFO underrun/overrun condition is detected or Threshold-burst size incompatibility; the Direct Mode Error flag is set in Peripheral-to-Memory mode, in Direct mode, when Memory Incrementation is disabled. It indicates that new data is being transferred to a memory location whereas the previous transfer is not complete yet.

# Related peripherals



- Refer to these trainings linked to this peripheral:
  - DMAMUX (DMA request router)
  - MDMA (Master direct memory access controller)

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You can refer to training slides related to the DMA request multiplexer (DMAMUX) and master direct memory access (MDMA) peripherals for additional information.