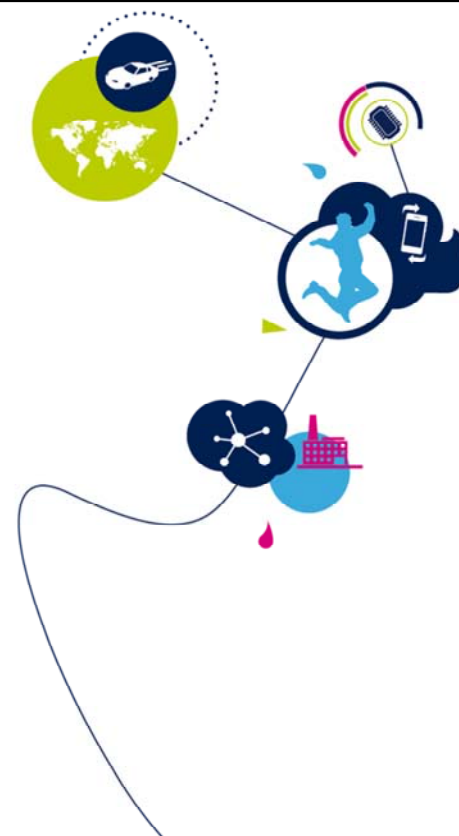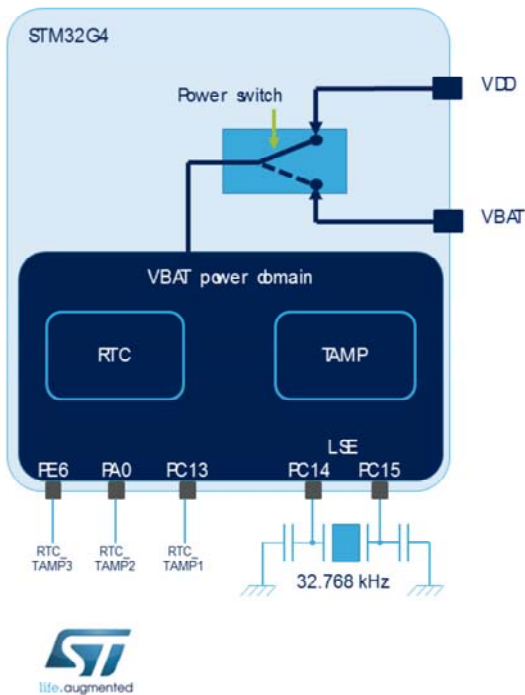# STM32G4 – TAMP

Tamper and backup registers
Revision 1.0

life.augmented

Hello, and welcome to this presentation of the STM32 tamper and backup registers. It covers the main features of this peripheral, which is used to provide security against tamper events.

- The TAMP features 32 backup registers, erased on tamper detection
- Two types of tamper input: external (3 GPIOs) and internal (4 sources)
- Belongs to the Battery Backup Domain, so it remains functional when the main supply is off

Application benefits

- Tamper-protected backup registers
- Ultra-low-power tamper detection with filtering

The TAMP peripheral features 32 32-bit backup registers used to preserve data when the main supply is off. These backup registers can be used to store secure data, as they are erased when a tamper event is detected on the tamper pins or on some internal events. The tamper detection is functional in low-power modes when the VBAT domain is supplied by a backup battery. The anti-tamper circuitry includes ultra-low-power digital filtering, avoiding false tamper detections.

Key features

- **32 backup registers:**
  - The backup registers (TAMP_BKP0-31R) are implemented in the battery backup domain that remains powered-on by VBAT when the VDD power is switched off

- **3 external tamper detection events**
  - External passive tampers with configurable filter and internal pull-up

- **4 internal tamper events**

- **Any tamper detection can generate an RTC timestamp event**

- **Any internal tamper detection erases the backup registers**
 - Regarding external tamper, erasure can be disabled

The key features of the TAMP are:
128 bytes of backup registers, split into 32 32-bit backup registers.
These registers are preserved in all low-power modes and in VBAT mode, and are erased when a tamper detection event occurs on any one of the three tamper pins, or the 4 internal tamper events. Regarding external tamper events, software can select whether backup registers are erased when the tamper event is detected.
The 3 tamper pins are available in VBAT mode.
The external tamper events can be detected on a programmable edge, or on level with a configurable filter and using an internal pull-up in an ultra-low power mode.
A timestamp function is used to save calendar contents in timestamp registers, depending on any tamper event.
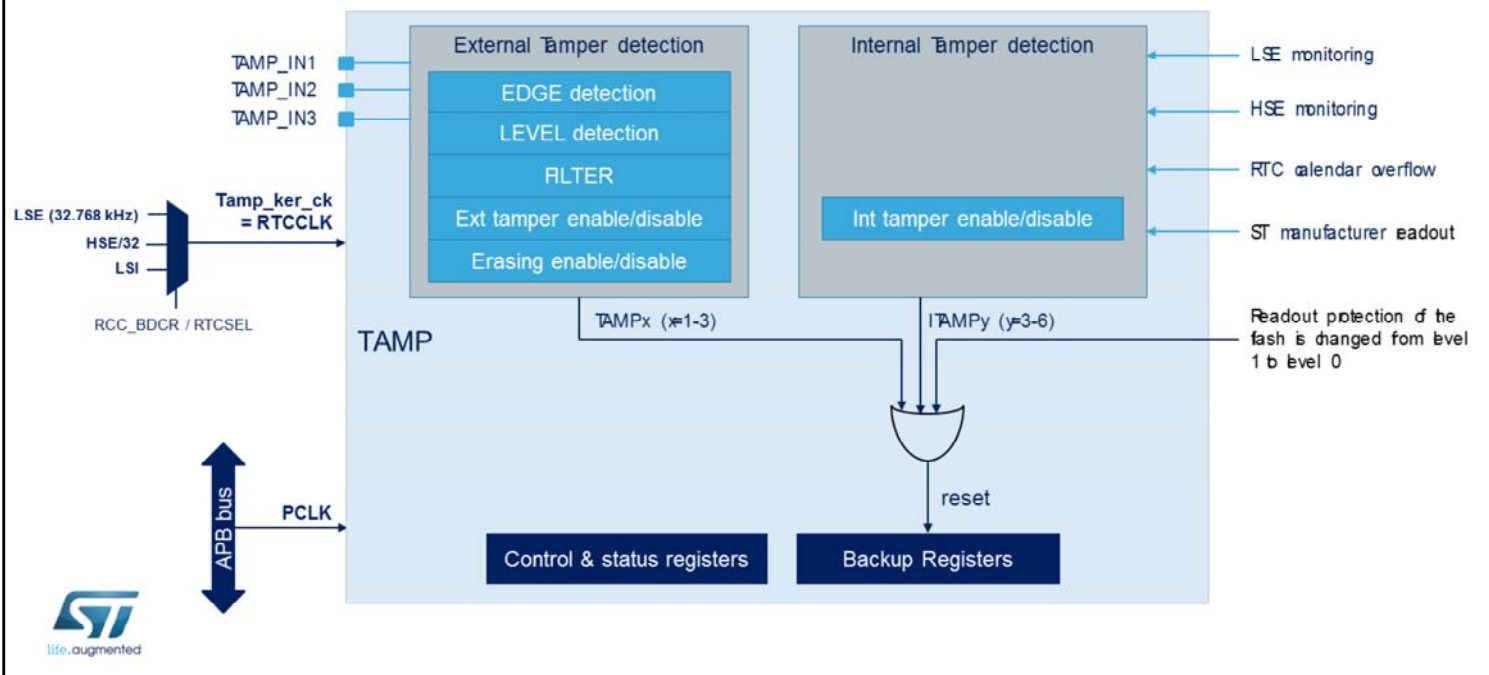
Here is the TAMP block diagram.
The TAMP has two clock sources: the TAMP clock (or RTCCLK) is only used for the tamper detection in Level Detection mode with filtering, and the APB clock is used for TAMP and backup registers read and write accesses.
The TAMP clock can use either the high-speed external oscillator (or HSE), divided by 32, the low-speed external oscillator (or LSE), or the low-speed internal oscillator (or LSI).
Only LSE or LSI are functional in Stop and Standby modes.
Only LSE is functional in Shutdown and VBAT modes.
Several internal features can generate a tamper event: LSE monitoring, HSE monitoring, RTC calendar overflow, and ST manufacturer readout.
Each internal and external tamper has an enable control bit. By default internal tampers are enabled and external

tampers are disabled.

By default, all tamper detection events will erase the backup registers. External tamper events can be configured to not erase the backup registers.

Note that the backup registers are not reset by system reset or when the device wakes up from Standby mode.

Backup registers can be reset when a tamper detection event occurs or when the readout protection of the flash is changed from level 1 to level 0.

Tamper detection

Ultra-low power anti-tamper circuitry
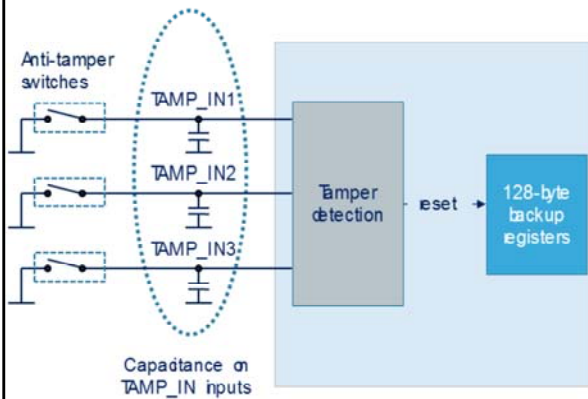
- 3 tamper pins and events, available in VBAT mode
- Configurable active edge or level for each event
- Reset of backup registers when an external tamper event is detected
  - May be disabled for external tampers
- Tamper can generate a timestamp event

The TAMP embeds ultra-low-power tamper detection circuitry.
The purpose is to detect physical tampering in a secure application, and to automatically erase sensitive data in case of intrusion.
3 tamper pins and events are supported, and are functional in all low-power modes and in VBAT mode.
The detection can be edge- or level-triggered, and the active edge or level is configurable for each event.
A pre-charge time is determined by the TAMPRECH bits, in order to support large capacitances on the TAMP_Inx inputs.
A tamper event can generate a timestamp event, which can be used to record the date of the intrusion attempt.
The capacitors shown in the figure perform filtering.
If no external capacitors are explicitly connected to a Tamper input, they provide a model of the trace capacity.
Note that an external pull-up is required in Edge Detection mode.
In Level Detection mode, the internal pull-up is used, as explained in the next slides.

Safe and ultra-low-power tamper detection with filtering

- Configurable use of I/O pull-up resistor to detect anti-tamper switch open state

- Configurable pre-charging pulse to support different capacitance values
  - 1, 2, 4 or 8 cycles

- Configurable filter
  - Sampling rate: 128, 64, 32, 16, 8, 4, 2, or 1 Hz
  - Number of consecutive identical events before issuing an interrupt to wake up the microcontroller: 1, 2, 4, or 8

The tamper detection circuit includes an ultra-low power digital filter.
The internal I/O pull-up can be used to detect the anti-tamper switch state.
The I/O pull-up is applied only during the pre-charging pulse in order to avoid any consumption if the tamper pin is at a low level.
The pre-charging pulse duration is configurable to support different capacitance values, and can be 1, 2, 4 or 8 TAMP clock cycles.
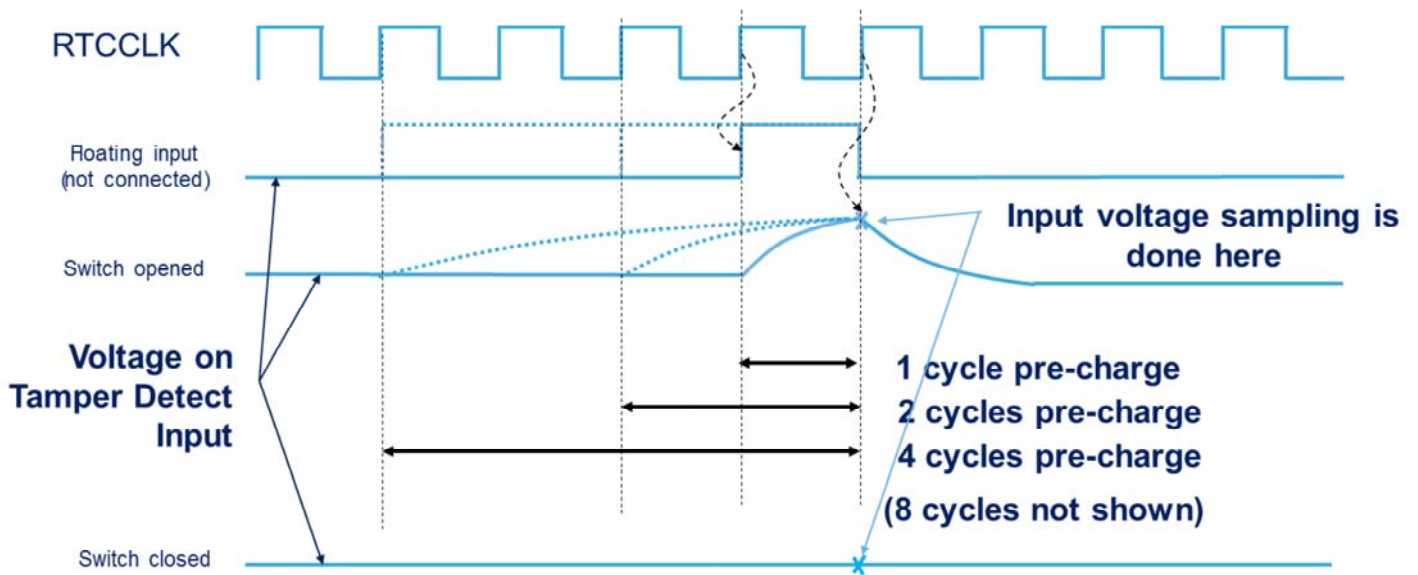The pin level is sampled at the end of the pre-charging pulse.
A filter can be applied to the tamper pins.
It consists of detecting a given number of consecutive identical events before issuing an interrupt to wake up the device.
This number is configurable and can be 1, 2, 4 or 8 events, at a programmable sampling rate from 1 to 128 Hz.
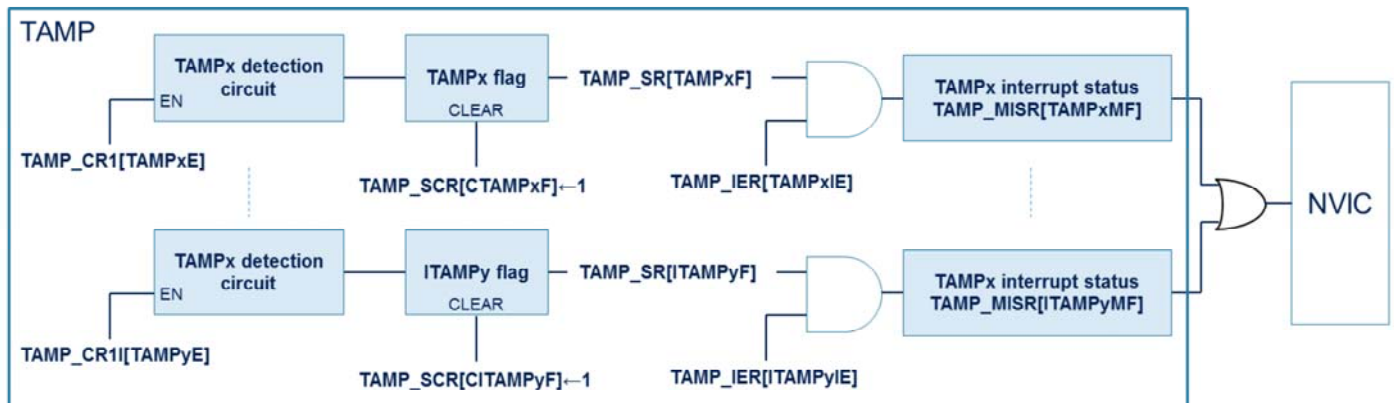
Tamper detection - signals

This figure illustrates tamper detection using the internal pull-up.
The internal pull-up can be applied for 1, 2, 4 or 8 cycles.
If the switch is opened, the level is pulled-up by the resistor.
If the switch is closed, the level remains low.
The input voltage is sampled at the end of the pre-charge pulse.

- Tamper detection can generate interrupts or trigger events, and can benefit from digital filtering
    - Interrupts can be enabled/disabled for each event
    - Backup registers erase is configurable for each external event
    - Hardware trigger to the low-power timer is configurable for each external event

The tamper detection circuitry can also be used to generate interrupts or trigger events.
Each tamper interrupt can be individually enabled or disabled.
Each external tamper event can be individually configured to erase the backup registers or not.
Each external tamper event can be individually configured to generate a hardware trigger to low-power timer.
This takes advantage of the digital filtering present on these I/Os for interrupt or trigger generation.

Interrupt event	Description
TAMPx	Set when a tamper event is detected on TAMP_INx
ITAMPy	Set when an internal tamper event is detected on ITAMP_INy

All interrupts can wake the processor up from all low-power modes. The detection on all tamper pins and internal tamper sources can generate an interrupt.

Any tamper detection circuit can be enabled or disabled by programming the TAMP_CR1 register.

If it is enabled and a tamper event is detected, the corresponding flag is set in the TAMP_SR register.

Then TAMP_IER register masks or enables the tamper event interrupt.

The interrupt service routine can easily determine which tamper event has occurred by reading the TAMP_MISR register which contains flags identifying the source of the tamper event interrupt.

The nested vectored interrupt controller (or NVIC) has a unique input related to RTC and TAMP modules.

Mode	Description
Run	Active
Sleep	Active ➤ TAMP interrupts cause the device to exit Sleep mode.
Low-power run	Active
Low-power sleep	Active ➤ TAMP interrupts cause the device to exit Low-power sleep mode
Stop 0/Stop 1	Level detection with filtering is active only when clocked by LSE or LSI ➤ TAMP interrupts cause the device to exit Stop 0/Stop 1 mode
Standby	Level detection with filtering is active only when clocked by LSE or LSI ➤ TAMP interrupts cause the device to exit Standby mode
Shutdown	Level detection with filtering is active only when clocked by LSE ➤ TAMP interrupts cause the device to exit Shutdown mode

The TAMP peripheral is active in all low-power modes and the TAMP interrupts cause the device to exit the low-power mode.
In Stop 0, Stop 1, and Standby modes, only the LSE or LSI clocks can be used to clock the TAMP.
Only the LSE is functional in Shutdown mode.

- Refer to these peripheral trainings linked to the TAMP
  - Real-time clock (RTC)
  - Reset and clock control (RCC)
  - Nested vectored interrupt controller (NVIC)

This is a list of peripherals related to the real-time clock. Please refer to these peripheral trainings for more information if needed.
- Real-time clock,
- Reset and clock control,
- Nested vectored interrupt controller.