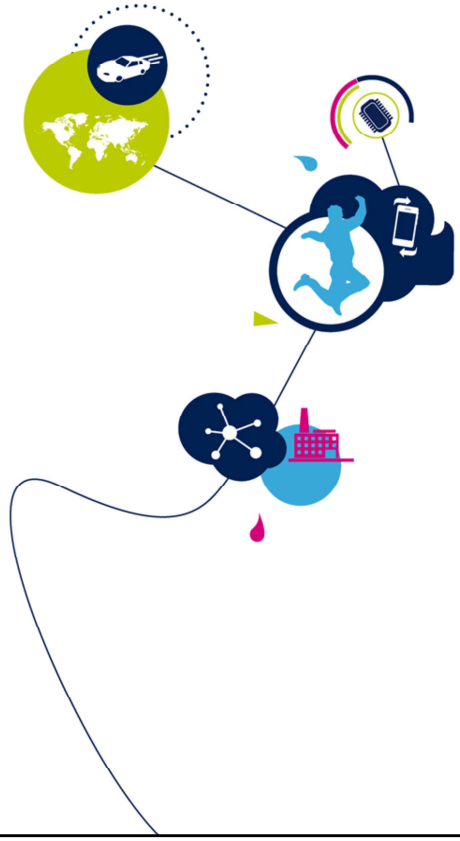
STM32H7- DLYB

Delay Block

Revision 1.0



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Hello, and welcome to this presentation of this Delay Block Module.

Overview

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- Generates a delayed sample clock for the SDMMC and QSPI communication interfaces.
- Input clock frequency ranges from 25 to 208 MHz.
- Firmware controlled
- No compensation for voltage and temperature drift.

Application benefits

- Supports SDMMC cards with variable delay.
- Improves timing margin for SDMMC and QSPI.

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The Delay Block module integrated inside STM32H7 microcontrollers is used to tune the receive data sampling clock for the SD/SDIO/MMC card host interfaces (SDMMC) and Quad-SPI memory interface (QSPI). It is mandatory for use with SDMMC Ultra-High-Speed (UHS-I) interface cards having a variable delay.

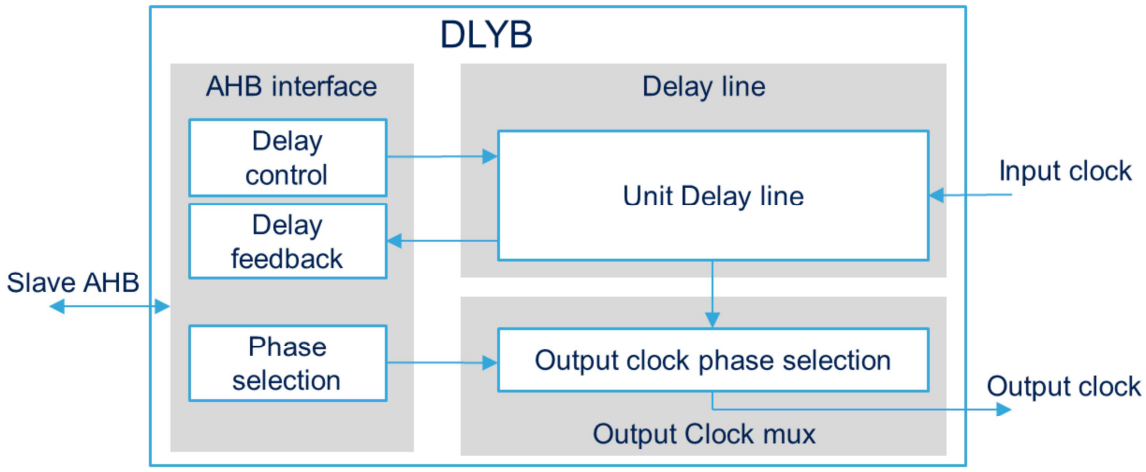
A wide input clock frequency range from 25 up to 208 MHz is supported.

The delay on the output clock is controlled by the firmware and may require retuning due to voltage or temperature drift.

Applications benefit from being able to support SDMMC UHS-I cards having variable delay, and easier integration of the high-speed SDMMC and QSPI interfaces.

In the STM32H7, a Delay Block is available with the SDMMC1, SDMMC2, and the QUADSPI modules.

Block diagram



Located on the AHB bus, the Delay Block module consists of an "AHB interface“ containing the delay line control, feedback information and output clock selection registers with the “Delay line” and “output clock multiplexer” parameter values.

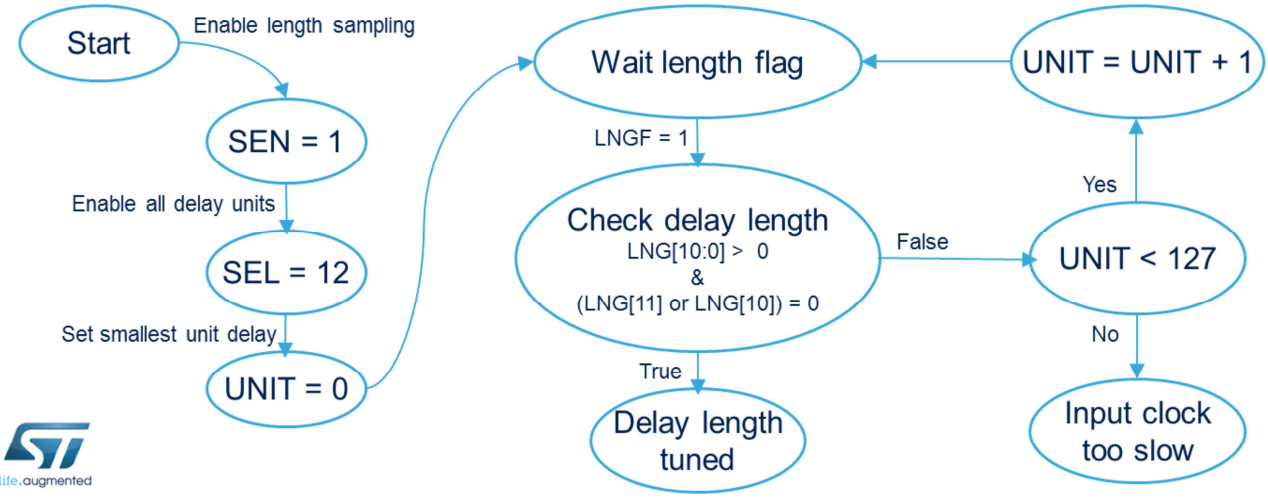
The Delay Block module consists of 12 delay units with programmable unit delays. The delay line feedback information is used to tune the delay line to one period of the input clock.

The output clock phase is selected by the Phase Selection register.

Delay Block procedure

Delay line tuning

- Before selecting the output clock phase, the delay line length must be tuned to one period of the input clock.



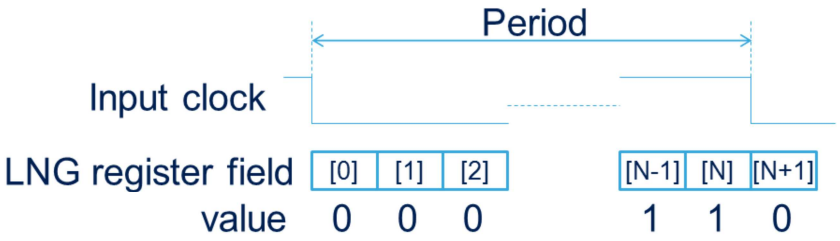
Before selecting an output clock phase, the delay line must be tuned to span one input clock period. To do this, set the SEN bit to '1' to enable the delay length sampling. (This will at the same time disable the output clock).
Then set SEL[3:0] to ‘1100’ to enable all delay units.
Select the smallest unit delay by setting UNIT[6:0] to '0'.
Writing the register UNIT field will trigger the delay line sampling.
Once the sampling over one input clock period is completed, the LNGF flag is set.
Firmware must poll this bit before checking the delay line length feedback in LNG[11:0].
When the LNG field is not 0 and either LNG bit 11 or bit 10 is ‘0’, the delay line spans one input clock period and the delay line length tuning process is finished.
Otherwise, the unit delay is increased and a new check is performed.

When the maximum delay unit is reached and the check is still false, the input clock is too slow to fit one complete period in the delay line.

Delay Block procedure

Delay length detection

- Once the delay length has been tuned, the number of delay cells spanning one input clock period has to be determined.
- The first msb bit of LNG[11:0] being '1' determines the number of delay units that span one input clock period.

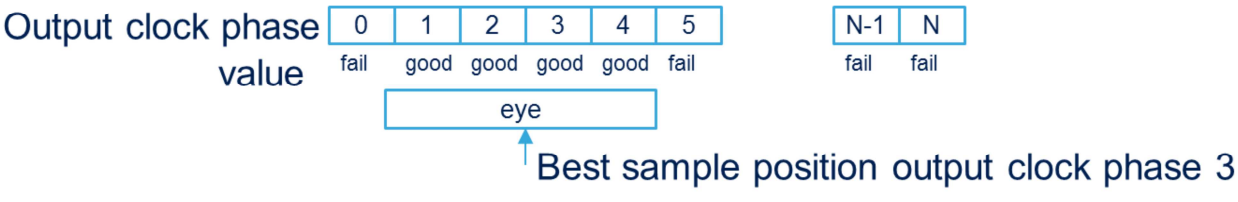


Once the delay line is tuned, you can determine how many delay units span one input clock period.
Starting from the LNG[11:0] most significant bit downwards, the first bit set to '1' determines the number of delay units that span one input clock period.
Number of delay units = bit index + 1.
That is, if the first LNG bit set to '1' is bit number [10], then 11 delay units [0:10] span one input clock period.

Delay Block procedure

Output clock phase selection

- To determine the best output clock in the associated peripheral, a receive data eye diagram must be constructed based on all sample positions.
- Using this eye diagram, the best sample position can be determined.
- A new output phase can only be selected when the output clock is disabled.
- The SD standard provides a tuning block for this purpose.



To determine the eye diagram, all peripheral interface data must be received and verified for all selectable output clock phases. From this a pattern with good and failing output clock phases will be obtained.
Subsequently, the best phase among the good ones is selected.
To select a new output clock phase, first set the SEN bit to ‘1’ to disable the output clock. Once the output clock phase is selected via bits SEL[3:0], the output clock can be re-enabled by resetting the SEN bit to ‘0’.
The SD specification provides a special tuning block to tune the receive data sample point.

Polling bits

Polling bit	Description
LNGF	Delay line sampling ready flag

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Following a unit delay update in UNIT, the LNGF flag informs the firmware that the delay line sampling has finished, and the delay length feedback can be read from bits LNG[11:0].

Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral registers content is kept. Clock input and output delay functional.
Stop	Active. Peripheral registers content is kept. Clock input and output delay functional.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

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Here is an overview of the peripheral status in specific low-power configuration modes. The Delay Block module is not able to change state in Sleep mode and lower. However the input to output clock delay is functional down to and including Stop mode. In Standby mode, the Delay Block module is powered down.

Related peripherals

- Refer to these peripherals trainings linked to this peripheral, if any
  - Reset and clock controller (RCC)
  - General-purpose input/outputs (GPIOs)
  - SD/SDIO/MMC card host interfaces (SDMMC)
  - Quad-SPI memory interface (QSPI)

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Here is a list of peripherals related to the Delay Block module. Users should be familiar with all the relationships between these peripherals to correctly configure and use the Delay Block module.