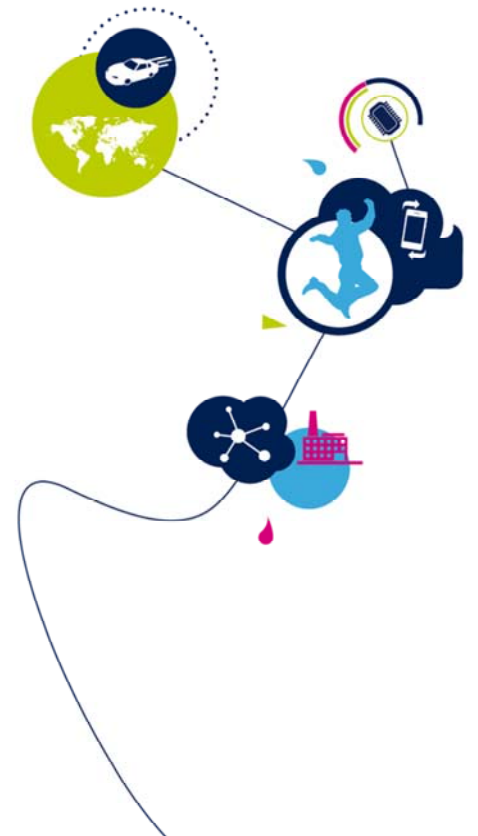
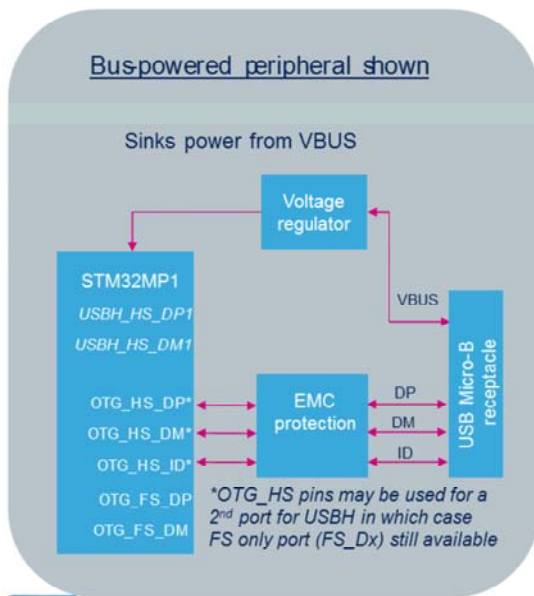


STM32MP1 - OTG

USB High Speed interfaces
Revision 1.0



Hello, and welcome to this presentation of the STM32MP1 USB Full Speed and High Speed interfaces. It covers all the features of these interfaces, which are widely used to connect either a PC or a USB device to the microcontroller.



- Provides USB 2.0 High Speed and Full Speed interfaces
- Supports “On-the-Go” products

Application benefits

- High Speed integrated PHY
- Low-power implementation
- Quicker charging via Battery Charger Detection



This figure shows the connections between a STM32MP1 microcontroller and a USB connector. The STM32MP1 features a USB High Speed communication interface, allowing the microcontroller to communicate typically with a PC or a USB storage device. The simplest implementation is a USB peripheral device but the STM32MP1 microcontroller also supports the USB “On-the-go” functionality. The above diagram connects the High Speed pins, but the Full Speed pins can also be used when both High Speed ports are used for USB host ports (see other module USBH).

- USB 2.0 High Speed (480 Mbits/s)
 - Integrated High Speed PHY (main port, statically shared with USBH EHCI host controller)
 - Integrated Full Speed PHY (second port)
 - Supports Link Power Management (LPM)
 - Device support, but also supports OTG specification (targeted hosts)
 - “On-the-Go” products and embedded hosts
 - Allows a device to have a limited host behavior as an “embedded host”
 - Latest specification, OTG 2.0 supported
 - Includes battery charger detection hardware
 - Latest specification, BC 1.2 supported (implementation requires software)
 - By using this specification assisted by hardware, more current (up to 1.5 A) can be safely drawn from BC 1.2 compliant chargers hence decreasing battery recharge time



Let's look at some of the key features of this USB high speed interface, which is a USB specification 2.0 compliant interface that operates at a 480 Megabits per second bit rate.

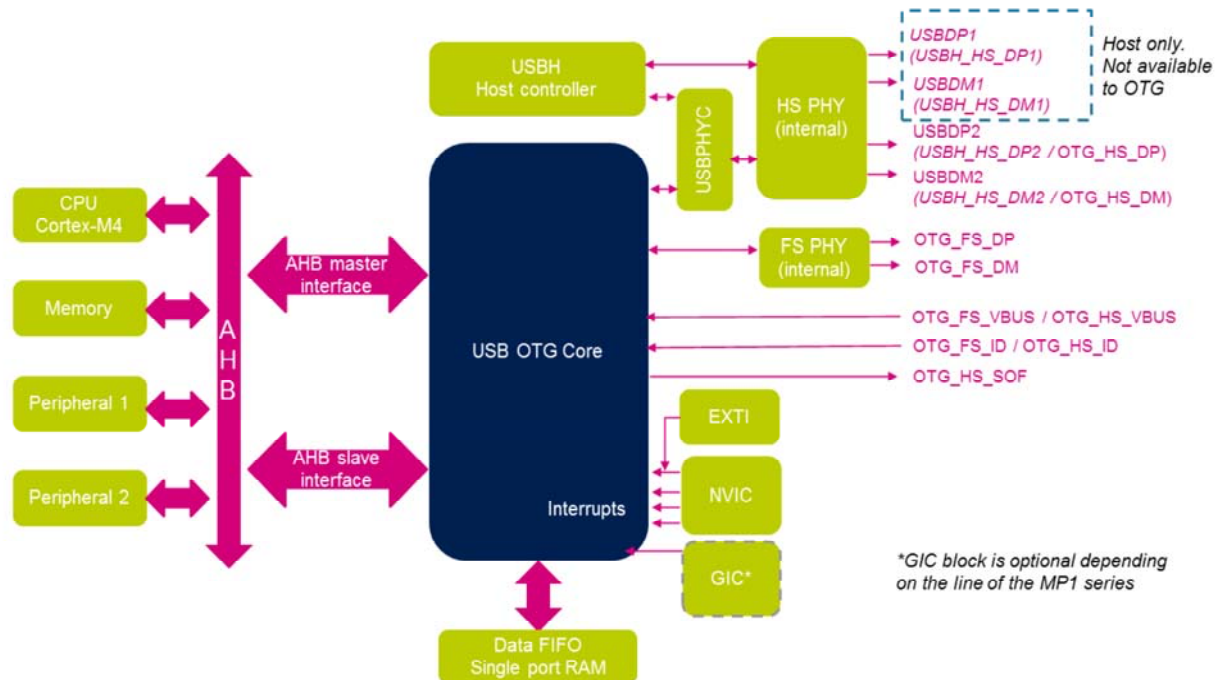
In the simplest form, a USB FS device can be implemented. Built-in support for Link Power Management adds enhanced power modes on top of the USB 2.0 specification.

In addition, the On-The-Go or “OTG” functionality enables implementation of an OTG product or an embedded host, both of which have the capacity to behave as a targeted host.

The battery charger detection function allows for increased current to be drawn from BC1.2-compliant chargers up to 1.5A.

USB 2.0 High Speed is also available via the ULPI interface. The same modes of operation are possible when coupling with an external ULPI transceiver.

Block diagram (OTG; USBH; USBPHYC)



In this block diagram, the USB OTG High Speed controller core is shown in the center with its data FIFOs below. It can either be used in conjunction with the second port of the HS (high speed) PHY or the FS (full speed) PHY. These PHYs on its right side handle the analog signal levels including many specific level detections relating to On-The-Go and Battery Charger detection functions. The USB interrupt goes to the Cortex-M4 processor to signal various USB events. The AHB slave interface enables read/write access of the controller registers and the Power & Clock control block. Transfers to and from memory are handled by a DMA engine inside the controller via the AHB master interface.

- Peripheral (device) mode function:
 - For a regular (i.e. non-OTG) device
 - For an OTG device when operating in Peripheral mode
- Targeted Host mode function:
 - For an embedded host
 - For an OTG device when operating in Embedded Host mode



At any given time, one of the two operating modes will be functional:

Peripheral mode, which will be used for a regular device or an OTG device when operating in Peripheral mode.

Targeted host mode, which will be used for an embedded host or an OTG device when operating in Host mode.

Interrupt event	Description
Resume/remote wakeup	Wakeup interrupt during suspend(L2) or LPM(L1) state.
Session request/ new session detected	Host mode: Session request is detected from the device. Device mode: VBUS in the valid range for B-peripheral device.
Disconnect detected	Asserted when a device disconnect is detected.
Connector ID status change	Change in connector ID status
LPM interrupt	Device: receives LPM transaction, responds with non-ERRORed response. Host: device responds to LPM transaction with non-ERRORed response or when host core has completed LPM transactions for programmed number of times.
Periodic Tx FIFO empty	When the periodic transmit FIFO is either half or completely empty and there is space for at least one entry to be written in the periodic request queue.
Host channels interrupt	Interrupt pending on one of the channels of the core (in Host mode).
Host port interrupt	Indicates a change in port status of one of the OTG_FS(/HS) controller ports in Host mode.
Reset detected	In device mode, this interrupt is asserted when a reset is detected on the USB in partial power-down mode when the device is in Suspend mode.



Interrupts from this USB block can be triggered by a large number of events or state changes.

This slide and the following three slides show all the events that can trigger an interrupt. As can be seen, these interrupt sources are diverse; they range from events related to low power management and OTG, to events related to normal host behavior and regular USB reset and disconnect events.

Interrupts (continued)

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Interrupt event	Description
Incomplete periodic transfer	Host: when there are incomplete periodic transactions still pending. Device: at least one isochronous OUT endpoint on which the transfer not completed.
Incomplete isochronous N transfer	At least one isochronous N endpoint on which the transfer is not completed in the current frame.
OUT endpoint interrupt	Interrupt is pending on one of the OUT endpoints of the core (in Device mode).
N endpoint interrupt	Indicates that an interrupt is pending on one of the N endpoints of the core (in Device mode).
End of periodic frame interrupt	Period specified in the periodic frame interval field has been reached in the current frame.
Isochronous OUT packet dropped interrupt	Failed to write an isochronous OUT packet into the Rx FIFO because the Rx FIFO does not have enough space to accommodate a maximum size packet for the isochronous OUT endpoint.
Enumeration done	Speed enumeration is complete.
USB reset	Device mode: A reset is detected on the USB (N.B. when not in partial Power-down mode).



In this second slide showing interrupts, another diverse set of sources is described.

Interrupts (continued)

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Interrupt event	Description
USB suspend	Suspend was detected on the USB.
Early suspend	Idle state has been detected on the USB for 3 ms.
Global OUT NAK effective	Set global OUT NAK bit, set by the application, has taken effect in the core.
Global N non-periodic NAK effective	Set global non-periodic N NAK bit, set by the application, has taken effect in the core.
Non-periodic Tx FIFO empty	Non-periodic Tx FIFO is either half or completely empty.
Rx FIFO non-empty	At least one packet pending to be read from the Rx FIFO.
Start of frame	Host mode: core sets this bit to indicate that an SOF (FS), or Keep-Alive (LS) is transmitted on the USB. Device mode: core sets this bit to indicate that an SOF token has been received on the USB.
OTG interrupt	OTG protocol event.
Mode mismatch interrupt	Host mode register access, when the core is operating in Device mode (and vice versa).

In this third slide describing interrupt sources, many SUSPEND, OTG functions and FIFO status events are listed as well as a general register access error.

Low-power modes (OTG)

Mode	Description
Suspend: Gate HCLK	Most of the system dock domain internal to the OTG high-speed core is switched off by dock gating.
Suspend: USB system stop	Application may decide to drastically reduce the overall power consumption by a complete shut down of all the dock sources in the system.



Low-power modes for the High Speed core are available when USB suspend is active in device mode. Refer also to the next slide.

MPU mode	Description	USB availability
Run	MCU fully active.	Required until USB enters Suspend mode.
Sleep	Peripheral interrupts cause the device to exit Sleep mode. Peripheral registers content is kept.	Available while USB device is in Suspend mode.
Stop/ LP Stop	Peripheral interrupts cause the device to exit Stop mode. Peripheral registers content is kept.	Available while USB device is in Suspend mode. Offers optimal power reduction.
LP LV Stop	Lower voltage stop mode.	Not compatible with USB applications (no wakeup from Suspend possible).
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.	Not compatible with USB applications.



The USB OTG peripheral is fully active in Run mode. During USB suspend, Sleep, Stop and LP Stop modes may be used.

- A few dedicated bits are implemented to assist debugging of
 - USB receive data FIFO status/contents (both host and device modes)
 - Host mode: periodic queue scheduling

Debug bit	Description
OTG Receive status debug read / OTG status read and pop registers	Special read FIFO access for debug.
Top of the periodic transmit request queue	Indicates the entry in the periodic Tx request queue that is currently being processed by the MAC.



Within the USB module, certain dedicated bits are implemented to allow debug functionality in a USB application.

They relate to FIFO status and contents and the scheduling of periodic queues in Host mode.

Additional details of these debug bits are listed in this table.

- USBPHYC is needed in order to use the two port High Speed (HS) UTMI PHY that is integrated in the STM32MP1 microcontroller
- USBPHYC functions
 - controls the PLL associated with the HS PHY
 - controls the UTMI switch on the shared PHY port #2, enabling the OTG to use that port
 - enables fine tuning of the HS PHY transmitter and receiver, necessary for optimal performance

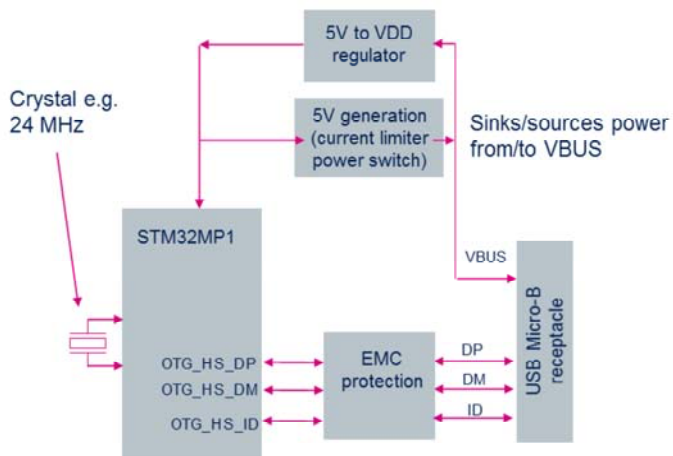


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USBPHYC is a small controller needed whenever the High Speed PHY will be used. It is to be used for controlling the PLL inside the High Speed PHY and enabling OTG controller access to its second port. Fine tuning of the High Speed PHY should also be done by using USBPHYC, this is necessary to get notably a well-adjusted eye diagram.

Application: OTG “On-The-Go” application

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- The schematic shows an example of a design for an “OTG” application
- In this example, the device is bus powered, drawing power only from USB VBUS
- A single 24 MHz crystal oscillator can be used



Here is an application example of an USB OTG or “On-The-Go” application.

Power can be drawn directly from the USB VBUS signal when in device mode.

The VBUS should be generated locally when in host mode. A single crystal oscillator (for example 24 MHz) is needed outside.

- For more details, please refer to the following source pages:
 - www.usb.org : [Document library page](#)
 - “[USB2 specification](#)” => a ZIP file containing:
 - USB2.0 specification
 - On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification (USB2), latest version 1.1a
 - USB 2.0 ECN: Link Power Management Addendum
 - “[Battery Charger v1.2](#)” specification
 - [ST Microelectronics MPU Wiki pages](#)



For complete USB specification documents, please refer to USB.org.

USB2.0 document home page has a ZIP file containing the USB2.0 and OTG2.0 specifications and an ECN for LPM . Please refer also to the MPU wiki pages.