Welcome to the presentation of the STM32 direct memory access controller (DMA). It covers the main features of this module, which is widely used to handle the STM32 peripheral data transfers.
The Direct memory access (DMA) embedded on the STM32H7 series is used to provide high-speed data transfers between peripherals and the memory and between memory and memory. Data can be quickly moved by the DMA without any CPU action. This keeps CPU resources free for other operations.

The DMA controller combines a powerful dual AHB master bus architecture with an independent FIFO to optimize the system’s bandwidth, based on a complex bus matrix architecture.

**Overview**

- **DMA1/2 features**
  - Dual AHB master bus
  - Flexible configuration
  - Hardware and software priority management
  - Configurable data transfer modes
    - Peripheral-to-Memory, Memory-to-Peripheral, and Memory-to-Memory modes

**Application benefits**

- DMA support for timers, ADC, and communication peripherals in D2 domain
- Offloads CPU from data transfer management
- Simple integration
The two DMA controllers (DMA1 and DMA2) have 16 streams in total, each dedicated to managing memory access requests from many peripherals. Each stream has flexible hardware requests and support for software triggers. The stream software priority is programmable and a hardware priority is used in case of equality. Streams are independently configurable. Each stream has its own data format, increment type and data address for both source and destination.

A four-word FIFO per stream allows performing data packing/unpacking and burst transfers. Independent stream interrupt flags allow triggering half transfer, transfer complete, and transfer error events. In case of a transfer error, the faulty stream is automatically disabled without any impact on the other active DMA streams.
For each stream, the source and destination data size format is independently configurable for 8-, 16- or 32-bit packets. The transfer type for the source and the destination can be independently programmed in single mode or burst mode. The source and destination addresses and pointer increment are also independently configurable. The transfer data size can be pre-programmed up to 65535. Circular buffer mode is available to support a continuous flow of data. The source and the destination addresses and the number of data to be transferred are automatically reloaded after the complete transfer. Double Buffer mode allows the switching between two memory buffers to be managed by hardware.
Memory-to-memory mode allows transfers from one address location to another without a hardware request. Once the stream is configured and enabled, the transfer starts immediately. When data is transferred to or from a peripheral, the hardware request coming from the selected peripheral is used to trigger the data transfer on the DMA Peripheral port. Once the transfer is completed, the request is acknowledged.
When FIFO mode is enabled (Direct mode disabled) the DMA controller manages the data format difference between source and destination (data packing and unpacking). Thanks to its internal FIFO, the DMA stream can reduce software overhead and the number of transactions over the AHB Bus.
In Single or Burst mode, the FIFO threshold level determines when the data in the FIFO should be transferred to/from memory.

There are four configurable threshold levels per stream starting from “one quarter FIFO Full” to “FIFO Full”.

Depending on the transfer direction on the memory port, when the FIFO threshold is reached, the FIFO is filled from or flushed to the memory location.

Burst mode is only available when FIFO mode is enabled. When setting Burst mode, the FIFO threshold should be compatible with burst size. It allows the DMA streams to have the burst data available in the FIFO to carry out a burst transfer.
DMA controllers support Circular mode allowing to configure the number of data items to transfer once, and automatically restart the transfer after a Transfer Complete event. Double buffer mode is only available in Circular mode. It allows to switch automatically by hardware between two memory addresses each time a Transfer Complete event occurs. In Double buffer mode, a status flag and control bit (CT) is available to monitor which destination is being used for data transfers.
The DMA controller provides access to 8 streams with up to 115 channels (requests) per stream. Each of the 8 streams are connected to dedicated hardware DMA channels (requests).
The priorities between the DMA stream requests are software-programmable (4 levels consisting of very high, high, medium, and low) or hardware in case of equality (request 0 has priority over request 1, etc.).
Each DMA controller stream request can be connected to DMA requests from up to 115 possible peripherals by the DMA request router (DMAMUX). This selection is software-configurable and allows a great number of peripherals to initiate DMA requests.
Each stream also supports software trigger for memory-to-memory transfers.
Each DMA stream is designed with this group of interrupt events. The Half Transfer interrupt flag is set when half the data has been transferred; the Transfer Complete flag is set when the transfer is complete; the Transfer Error flag is set when an error occurs during the data transfer; the FIFO Error flag is set whenever a DMA FIFO underrun/overrun condition or Threshold-burst size incompatibility; the Direct Mode Error flag is set in Peripheral-to-Memory mode, in Direct mode, when Memory Incrementation is disabled. It indicates that new data is being transferred to a memory location whereas the previous transfer is not complete yet.
You can refer to training slides related to the DMA request multiplexer (DMAMUX) and master direct memory access (MDMA) peripherals for additional information.