Hello, and welcome to this presentation of the STM32H7 System overview.
This block diagram summarizes the key features of the new STM32H743 Single-core line which integrates the Cortex®-M7 core (with single- and double-precision floating point units) running up to 480 MHz, with 32 Kbytes of Cache, up to 2 Mbytes of Dual-bank Flash memory (with ECC and Read-While-Write capability), 1 Mbyte of SRAM with a scattered architecture: 192 Kbytes of TCM (Tightly-Coupled Memory) RAM including 64 Kbytes of ITCM (Instruction TCM) RAM and 128 Kbytes of DTCM (Data TCM) RAM for time-critical routines and data, 512 Kbytes, 288 Kbytes and 64 Kbytes of user SRAM, and 4 Kbytes of SRAM in the backup domain to keep data in the lowest power modes. This line also includes up to 35 communication peripherals in addition to the new LCD-TFT controller interface with dual-layer support taking advantage of the Chrom-ART Accelerator™. This graphics accelerator creates content.
twice as fast as the core alone.
The STM32H7x3 Single-core line embeds also 11 enhanced analog functions including low-power 14-bit ADCs running at up to 2 Msamples/s, 12-bit DACs and op-amps, as well as 22 timers, which include a high-resolution timer running at 480 MHz.
The STM32H7x3 Single-core line is pin-to-pin compatible with the STM32F7 series for common packages, and compatible with most of the common packages of the STM32F4 series.
In addition to the Single-core line, the STM32H7 series offers two new Dual-core lines: STM32H745 and STM32H747 which are based on high-performance ARM® Cortex®-M7 and Cortex®-M4 32-bit RISC cores. Running at up to 240 MHz, the ARM® Cortex®-M4 processor features a dedicated hardware adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state code execution from Flash memory.

STM32H743 and STM32H747 devices operate in the –40 to +85 °C temperature range and STM32H745 devices can operate in the –40 to 125 °C extended temperature range. All lines operate from a 1.62 to 3.6 V power supply.
The STM32H7 series features a total of 1 Mbyte of RAM: 192 Kbytes of TCM RAM (including 64 Kbytes of ITCM RAM + 128 Kbytes of DTCM RAM for time-critical routines), 864 Kbytes of user SRAM, and 4 Kbytes of SRAM in the Backup domain.

The Flash memory interface manages the CPU AXI accesses to the Flash memory. It implements the erase and program Flash memory operations and the read and write protection mechanisms.

The Flash memory is organized as follows:
Two main memory blocks divided into sectors and an information block containing:
- The System memory location from which the device boots in System memory boot mode
- The Option bytes to configure read and write protection, BOR level, watchdog software/hardware and reset when the device is in Standby or Stop mode.
The embedded system SRAM is divided into up to five blocks:

- **AXI SRAM (D1 domain)** accessible through the D1 domain’s AXI bus matrix:
  - AXI SRAM (512 Kbytes) mapped at address 0x2400 0000
  - Supports byte, half-word, full-word or double-word accesses

- **AHB SRAM (D2 domain)** accessible through the D2 domain’s AHB matrix:
  - AHB SRAM1 (128 Kbytes) mapped at address 0x3000 0000
  - AHB SRAM2 (128 Kbytes) mapped at address 0x3002 0000
  - AHB SRAM3 (32 Kbytes) mapped at address 0x3004 0000
  - Supports byte, half-word or full-word accesses

- **AHB SRAM (D3 domain)** accessible through the D3 domain’s AHB matrix:
  - AHB SRAM4 (64 Kbytes) mapped at address 0x3800 0000 and accessible by most system masters
  - Supports up to 32-bit width accesses

The system AHB SRAM can be accessed as bytes, half-words (16-bit units) or words (32-bit units), while the system AXI SRAM can be accessed as bytes, half-words, words or
double-words (64-bit units). These memories can be addressed at maximum system clock frequency without wait state.
The AHB SRAMs of the D2 domain are also aliased to maintain the Cortex®-M4 Harvard architecture:

- AHB SRAM1 also mapped at address 0x1000 0000 and accessible by all the system masters through the D2 domain AHB matrix
- AHB SRAM2 also mapped at address 0x1002 0000 and accessible by all the system masters through the D2 domain AHB matrix
- AHB SRAM3 also mapped at address 0x1004 0000 and accessible by all the system masters through the D2 domain AHB matrix.
The TCM (Tightly-Coupled Memory) SRAMs are dedicated to the Cortex®-M7 CPU:
- **DTCM-RAM** on the TCM interface is mapped at the address 0x2000 0000 and is accessible by the Cortex®-M7 CPU, and by the MDMA through the AHBS slave bus of the Cortex®-M7 CPU.
- **ITCM-RAM** on the TCM interface is mapped at the address 0x0000 0000 and is accessible by the Cortex®-M7 CPU, and by the MDMA through the AHBS slave bus of the Cortex®-M7 CPU.

- These memories can be addressed at maximum CPU clock frequency without wait state.

The TCM (Tightly-Coupled Memory) SRAMs are dedicated to the Cortex®-M7 CPU:
- **DTCM-RAM** on the TCM interface is mapped at the address 0x2000 0000
- **ITCM-RAM** on the TCM interface is mapped at the address 0x0000 0000

ITCM-RAM and DTCM-RAM are accessible by the Cortex®-M7 CPU, and by the MDMA (Master Direct Memory Access) through the AHBS slave bus of the Cortex®-M7 CPU.
At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:
- All Flash memory address space
- All RAM address space: ITCM, DTCM RAMs and SRAMs
- The System memory bootloader

The values on the BOOT pin are latched on the 4th rising edge of SYSCLK after reset release. It is up to the user to set the BOOT pin after reset.
If the programmed boot memory address is out of the memory mapped area or in a reserved area, the default boot fetch address is programmed as follows:

- **Cortex®-M7 Boot address 0:** Flash memory at 0x0800 0000
- **Cortex®-M7 Boot address 1:** System bootloader at 0x1FF0 0000
- **Cortex®-M4 Boot address 0:** Flash memory at 0x0810 0000
- **Cortex®-M4 Boot address 1:** SRAM1 at 0x1000 0000

When Flash Level 2 protection is enabled:

- Only boot from Flash memory or the system bootloader will be available. If boot address is out of the memory range or RAM address, the default fetch will be forced from the Flash memory at address 0x0800 0000 for the Cortex®-M7 core and the Flash memory at address 0x0810 0000 for the Cortex®-M4 core.
For STM32H7x5 and STM32H7x7 lines, boot codes are executed simultaneously but it is also possible to boot from one core while clock gating the other according to the option bytes:

<table>
<thead>
<tr>
<th>BCM7</th>
<th>BCM4</th>
<th>Boot order</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Cortex®-M7 is booting and Cortex®-M4 clock is gated</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Cortex®-M7 clock is gated and Cortex®-M4 is booting</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Cortex®-M7 is booting and Cortex®-M4 clock is gated</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Both Cortex®-M7 and Cortex®-M4 are booting</td>
</tr>
</tbody>
</table>

The enabled CPU is defined as the master, it is responsible for system initialization. The other CPU performs specific initialization operations.

Allows to implement safe booting and ensure proper initialization on power-up.

In the STM32H7x5/x7 lines, the two cores can boot individually or at the same time according to the option bytes as shown in this table. This allows implementation of safe booting and ensures proper initialization on power-up. The enabled CPU is defined as the master, it is responsible for system initialization. The other CPU performs specific initialization operations.